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Fast Implementation of Lifting Based DWT Architecture for Image Compression

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Fast Implementation of Lifting Based DWT Architecture for Image Compression

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Abstract - Technological growth in semiconductor industry have led to unprecedented demand for faster, area efficient and low power VLSI circuits for complex image processing applications. DWT-IDWT is one of the most popular IP that is used for image transformation. In this work, a high speed, low power DWT/IDWT architecture is designed and implemented on ASIC using 130nm Technology. 2D DWT architecture based on lifting scheme architecture uses multipliers and adders, thus consuming power. This paper addresses power reduction in multiplier by proposing a modified algorithm for BZFAD multiplier. The proposed BZFAD multiplier is 65% faster and occupies 44% less area compared with the generic multipliers. The DWT architecture designed based on modified BZFAD multiplier achieves 35% less power reduction and operates at frequency of 200MHz with latency of 1536 clock cycles for 512x512 image. The developed DWT can be used as an IP for VLSI implementation.

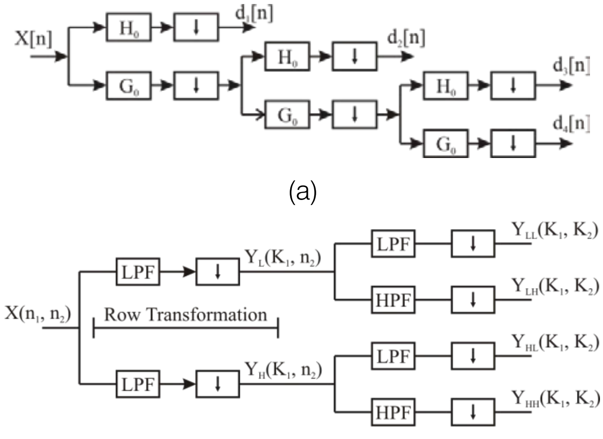
Keywords : DWT, Image compression, BZFAD multiplier, FPGA, Lifting scheme.

I. Introduction

The wavelet transformation is a widely used technique for image processing applications. Unlike traditional transforms such as the Fast Fourier Transform (FFT) and Discrete Cosine Transform (DCT), the Discrete Wavelet Transform (DWT) holds both time and frequency information, based on a multi-resolution analysis framework. This facilitates improved quality of reconstructed picture for the same compression than is possible by other transforms. In order to implement real time Codecs based on DWT, it needs to be targeted on a fast device. Field Programmable Gate Array (FPGA) implementation of DWT results in higher processing speed and lower costs when compared to other implementations such as PCs, ARM processors, DSPs etc. The Discrete wavelet transform is therefore increasingly used for image coding [1-4]. This is because the DWT can decompose the signals into different sub-bands with both time and frequency information and facilitate to arrive a high compression ratio [5]. It supports features like progressive image transmission (by quality, by resolution), ease of compressed image manipulation, region of interest coding, etc. The JPEG 2000 incorporates the DWT into its standard [6]. Recently several VLSI architectures have been proposed to realize single chip designs for DWT [7-10]. Traditionally, such algorithms were implemented using programmable DSP chips for low-rate applications or VLSI application specific integrated circuits (ASICs) for higher rates. To perform the convolution, we require a fast multiplier which is crucial in making the operations efficient.

II. Lifting Based DWT Scheme

Fig. 1a and Fig. 1b represent the top level architecture for 1D DWT. Input X is decomposed into multiple sub bands of low frequency and high frequency components to extract the detailed parameters from X using multiple stages of low pass and high pass filters. The sub band filters are symmetric and satisfy orthogonal property. For an input being image, the two 1D DWT computations are carried out in the horizontal and vertical directions to compute the two level decomposition. The inverse DWT process combines the decomposed image sub bands to original signal; the reconstructions is possible due to the symmetric property and inverse property of low pass and high pass filter coefficients.



(a)

(b)

a 1D b 2D

Figure 1 : Image Decomposition

Input x (n_1, n_2) is decomposed to four sub-components Y_{LL}, Y_{LH}, Y_{HL} and Y_{HH}. This results in a one level decomposition. The Y_{LL} sub-band component is further processed and is decomposed to another four sub-band components thus forming two level

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decomposition. This process is continued as per the design requirements till the requisite quality is obtained. Every stage of DWT requires LPF and HPF filters with down sampling by 2. Lifting based DWT computation is widely being adopted for image decomposition. In this work, we propose a modified architecture based on BZFAD [11] multiplier to realize the lifting based DWT.

Lifting scheme is one of the techniques that is used to realize DWT architecture. Lifting scheme is used in order to reduce the no of operations to be performed to half and filters can be decomposed into steps in lifting scheme. The memory required and also computation is less in case of lifting scheme. The implementation of the algorithm is fast and inverse transform is also simple in this method. The Fig. 2.shows the block diagram for lifting scheme [12].

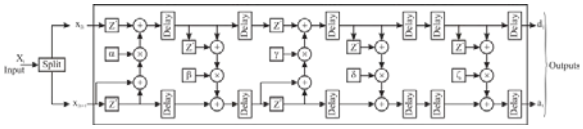

Figure 2 : Lifting scheme for 1D-DWT 9/7 filter

The z^{-1} blocks are for delay, α, β, γ, δ, ζ are the lifting coefficients and the shaded blocks are registers.9/7 filter has been used for implementation which requires four steps for lifting and one step for scaling. The input signal is x_i is split into two parts even part x_{2i} and odd part x_{2i+1} then the first step of lifting is performed given by the equations [13]:

$$d_i^1 = \alpha\,(x_{2i} + x_{2i+2}) + x_{2i+1} \qquad (1)$$

$$a_i^1 = \beta\,(d_i^1 + d_{i-1}^1) + x_{2i} \qquad (2)$$

The first equation is predict P1 and second equation is update U1.Then the second lifting step is performed which gives [13]:

$$d_i^2 = \gamma\,(a_i^1 + a_{i+1}^1) + d_i^1 \qquad (3)$$

$$a_i^2 = \delta\,(d_i^2 + d_{i-1}^2) + a_i^1 \qquad (4)$$

The third equation is predict P2 and fourth equation is update U2.Then scaling is performed and the following equations are obtained [13]:

$$a_i = \zeta\, a_i^2 = G_1 \qquad (5)$$

$$d_i = d_i^2/\zeta = G_2 \qquad (6)$$

The equations 5 and 6 are scale G_1 and G_2 respectively. The predict step helps determine the correlation between the sets of data and predicts even data samples from odd. These samples are used in the update step for updating the present phase. Some of the properties of the original input data can be maintained in the reduced set also by construction of a new operator using the update step. The lifting coefficients have constant values of -1.58613, -0.0529, 0.882911, 0.44350, -1.1496 for α, β, γ, δ, ζ respectively. By observation of the above equations, computing the final coefficients requires 6 steps. Data travels in sequence from stage 1 to stage 6, this introduces a delay of 6 stages. To speed up the process of computation, modified lifting scheme is proposed and realized.

III. Arithmetic Building Blocks for Lifting Scheme Implementation

High–speed multiplication has always been a fundamental requirement of high performance systems. Multiplier structure is one of the processing element consumes the maximum area and power and also constitutes delay. Therefore there is a need for high-speed architectures for N-bit multipliers with optimized area, speed and power. Multipliers are made up of adders, to reduce the Partial Product Reduction logic delay and regularize the layout. To improve regularity and compact layout, regularly structured tree with recurring blocks and rectangular-styled tree by folding are proposed at the expense of more complicated interconnects[14]. The present work focuses on multiplier design for low power applications such as DWT by rapidly reducing the partial product rows by identifying the critical paths and signal races in the multiplier. In other words, the goals have been to optimize the speed, area and power of the multiplier that form the major block in lifting based DWT.

a) Shift and Add Multiplier

In shift and add based multiplier logic, the multiplicand (A) is multiplied by multiplier (B). If the register A and B storing multiplicand and multiplier respectively is of N bit, the shift and add multiplier logic requires two N bit registers, and an N bit adder and N+1 accumulator. It also requires a N- bit counter to control the number of addition operation. In shift and add logic, the LSB bit of multiplier is checked for 1 or 0, if the LSB bit is 0, then the accumulator is shifted right by 1-position. If the LSB bit is 1 then the multiplicand is added with the accumulator content and the accumulator is shifted right by one bit position. The counter is decremented for every operation; the addition is performed until the counter is set to zero, which is indicated by the signal Ready. The multiplied product available in the accumulator of N clock cycles is the final output. Figure 3 below shows the top level block diagram of shift and add logic.

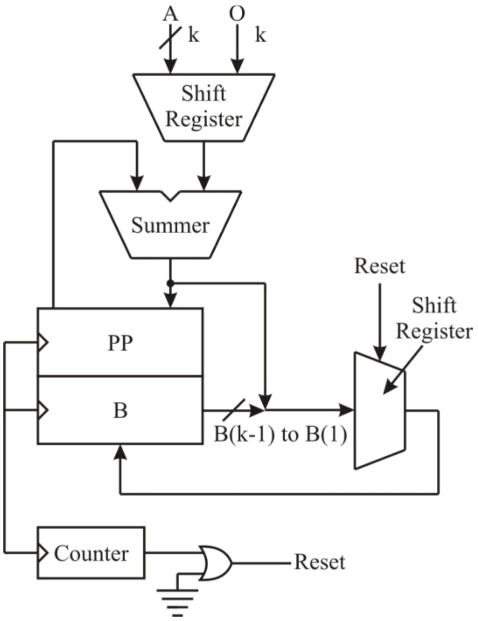

Fig. 3 : The Architecture of the Conventional Shift-and-Add Multiplier

IV. Bz-Fad Multiplier

As discussed in shift and add logic, if the LSB position is 1 then the accumulator is added with the multiplicand. If the accumulator contains more number of 1s, the adder has to add the 1 and this triggers the Full adder block within the adder. As we know that the power dissipation is due to switching activity of input lines, when ever the input or output changes, the power is switched from Vdd to Vss, thus contributing power dissipation. In order to reduce power dissipation, it is requried to reduce switching activity in the I/O lines. BZ-FAD [23] logic based multiplier reduces the switching activity and thus reduces power dissipation. In shift and logic for every operation the counter keeps track of number of cycles and thus controls the multiplication operation. In a binary counter, we know that the output bit change occurs in more than one bit, for example if the counter output is 2 and is changing to 3, there are two bit change occurring. This causes switching activity, and thus can be reduced by replacing the binary counter by ring counter. In a ring counter, at any given point of time only one bit change occurs, thus reducing switching activity and power dissipation. Another major source of power dissipation in shift and add logic is, for every bit 0 of the multiplier a shift operation is performed, thus all the bits in the accumulator are shifted by one bit position, this also introduces switching and thus power dissipation. In BZ-FAD logic, if the LSB bit is 0, then the shift operation is bypassed and a zero is introduced at the MSB, thus there is no shifting of accumulator content. In other words, if the LSB is zero, the accumulator is directly fed into the adder and there is no addition, but a zero is introduced by the control logic which is like right shift operation. The architecture of this multiplier is shown in Figure 4.

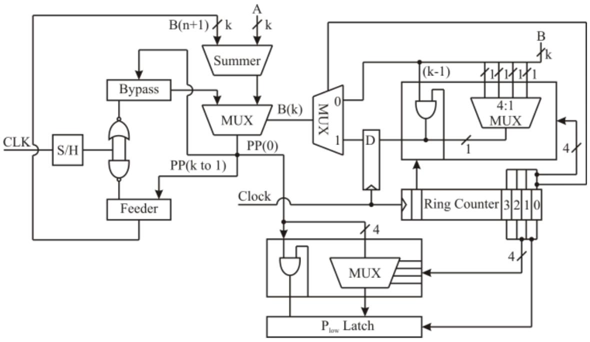

Fig. 4 : Low power multiplier architecture [16]

As the BZFAD, the control activity of ring counter, latch and bypass logic is realized using NMOS transistors, this introduces delay. The parasitic capacitance of NMOS transistors also increases the load capacitance and thus increases power dissipation. In order to reduce power dissipation we have replaced the transistor logic by MUX logic that have been designed to have ideal fanin and fanout capacitances. With MUX based logic the control signals can be suitably controlled to reduces switching activity as they are enabled only when required, based on the inputs derived from ring counter. However, the design requires more number of transistors and thus increases the chip area. We have also used the ripple carry adder which has the least average transition per addition among the look ahead, carry skip, carry-select and conditional sum adders to reduce power dissipation. Various multipliers are modeled in HDL and are analyzed for their performances and the results are tabulated for comparison. Next section discusses the comparison results of multiplier algorithms.

a) Comparison of Results

In this section, comparison of power, area for different types of multiplier with modified multiplier (BZ-FAD) is discussed. The results reveal that the modified BZ-FAD multiplier may be considered as a very low-power, yet highly area efficient multiplier.

b) Power Comparison

Table 1 : Power comparison of proposed multiplier with other multipliers

Multipliers	Total Dynamic power (w)	Cell Internal Power (µw)	Net Switching Power	Cell Leakage power (µw)
Modified BZ-FAD Multiplier	126	91.02	21.2	13.78
Shift and Add Multiplier	194	166.9	15.2	11.9
Booth Multiplier	379.12	295.62	62.2	21.3
Array Multiplier	231.5	145.4	66.3	19.8
Wallace Tree Multiplier	289.9	195.9	76.9	17.1

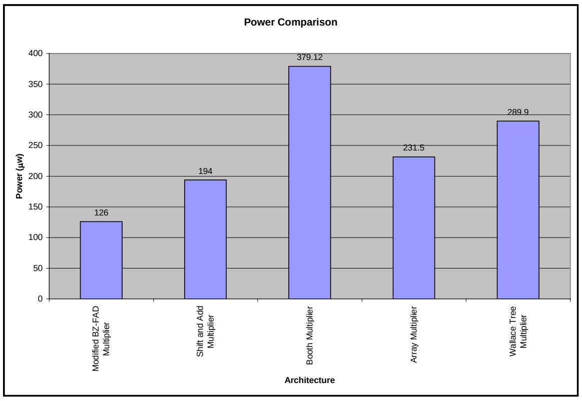

Fig. 5 : Power comparison of multipliers

As comparison, the power consumption of the multipliers for normally distributed input data are reported in Table 4.. As seen in Fig 5, the BZ-FAD multiplier consumes 33% lower power compared to the conventional multiplier. Finally, The results reveal that the BZ-FAD multiplier may be considered as a very low-power, yet highly area efficient multiplier.

c) Area Comparison

Table 2 : Area comparison of proposed multiplier with other multipliers [17,19]

Multipliers	Total Cell Area (µm2)	Number of Ports	Number of nets	Number of cells	Number of References
BZ-FAD Multiplier	2479.90	35	133	74	43
Shift and Add Multiplier	1726.25	35	99	43	12
Booth Multiplier	4459.06	34	233	163	32
Array Multiplier	3213.27	34	228	156	66
Wallace Tree Multiplier	3476.27	34	241	160	67

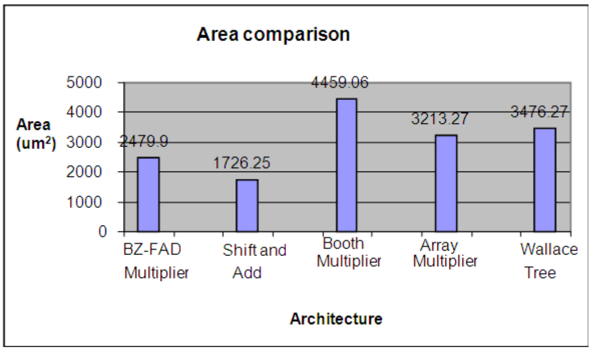

Fig. 6 : Area comparison of multipliers

In terms of the area, the proposed technique has some area overhead compared to the conventional shift-and-add multiplier as shown in Fig 6 and Table 2. Comparison between Fig 4 and Fig 3 reveals that M1, M2 and the ring counter are responsible for additional area in the proposed architecture. The area overheads of the ring counter and multiplexers *M1* and *M2* scale up linearly with the input data width. This leads to a small increase in the leakage power which, as the results reveal, is less than the overall power reduction. The leakage power of the 8-bit BZFAD architecture is about 11% more than that of the conventional architecture but the contribution of the leakage power in these multipliers is less than 3% of the total power for the technology used in this work. Finally, note that since the critical paths for both architectures are the same neither of the two architectures has a speed advantage over the other.

V. Discrete Wavelet Transform and Inverse Discrete Wavelet Transform Implementation

The discrete wavelet transform (DWT) is being increasingly used for image coding. This is due to the fact that DWT supports features like progressive image transmission (by quality, by resolution), ease of compressed image manipulation, region of interest coding, etc. DWT has traditionally been implemented by convolution. Such an implementation demands both a large number of computations and a large storage features that are not desirable for either high-speed or low-power applications. Recently, a lifting-based scheme that often requires far fewer computations has been proposed for the DWT [20, 21, 22]. The main feature of the lifting based DWT scheme is to break up the high pass and low pass filters into a sequence of upper and lower triangular matrices and convert the filter implementation into banded matrix multiplications. Such a scheme has several advantages, including “in-place” computation of the DWT, integer-to-integer wavelet transform (IWT), symmetric forward and inverse transform, etc. Therefore, it comes as no surprise that lifting has been chosen in the upcoming.

The proposed architecture computes multilevel DWT for both the forward and the inverse transforms one level at a time, in a row-column fashion. There are two row processors to compute along the rows and two column processors to compute along the columns. While this arrangement is suitable or filters that require two banded-matrix multiplications filters that require four banded-matrix multiplications require all four processors to compute along the rows or along the columns. The outputs generated by the row and column processors (that are used for further computations) are stored in memory modules.

The memory modules are divided into multiple banks to accommodate high computational bandwidth requirements. The proposed architecture is an extension of the architecture for the forward transform that was presented. A number of architectures have been proposed for calculation of the convolution-based DWT. The architectures are mostly folded and can be broadly classified into serial architectures (where the inputs are supplied to the filters in a serial manner) and parallel architectures (where the inputs are supplied to the filters in a parallel manner).

Recently, a methodology for implementing lifting-based DWT thatreduces the memoryrequirements and communication between the processors, when the image isbroken up into blocks. For a system that consists of the lifting-based DWT transform followed by an embedded zero-tree algorithm, a new interleaving scheme that reduces the number of memory accesses has been proposed. Finally, a lifting-based DWT architecture capable of performing filters with one lifting step, i.e., one predict and one update step. The outputs are generated in an interleaved fashion.

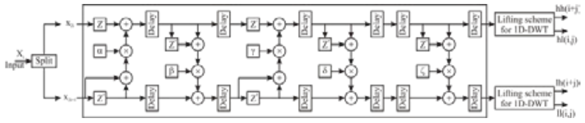

Figure 2.4 : 2-D Lifting-based DWT

The equations of the 1-D DWT based on lifting scheme is represented as

$$h(i) = x(2i+1)+\alpha(x(2i)+x(2i+2)) \quad (7)$$

$$l(i) = x(2i)+\beta(h(i)+h(i\text{-}1)) \quad (8)$$

The 2-D DWT is a multilevel decomposition technique, that decomposes into four sub bands such as *hh*, *hl*, *lh* and *ll*. The mathematical formulas of 2-D DWT are defined as follows:

$$hh(i,j) = h(2i+1,j) + \alpha\,(h(2i,j) + h(2i+2,j)) \quad (9)$$

$$hl(i,j) = h(2i,j) + \beta\,(hh(i,j) + hh(i-1,j)) \quad (10)$$

$$lh(i,j) = l(2i+1,j) + \alpha\,(l(2i,j) + l(2i+2,j)) \quad (11)$$

$$ll(i,j) = l(2i,j) + \beta\,(lh(i,j) + lh(i-1,j)) \quad (12)$$

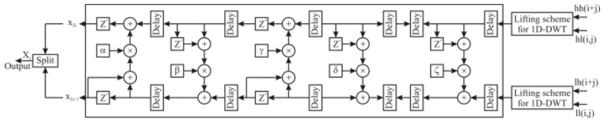

Figure 2.5 : 2-D Lifting based IDWT

The mathematical formulas of 2-D IDWT as defined as follows

$$l(2i,j)= ll(i,j)\text{-}\beta(lh(i,j)+lh(i\text{-}1,j)) \quad (13)$$

$$l(2i+1,j)= lh(i,j)\text{-}\alpha(L(2i,j)+l(2i+2,j)) \quad (14)$$

$$h(2i,j)= hl(i,j)\text{-}\beta(hh(i,j)+hh(i\text{-}1,j)) \quad (15)$$

$$h(2i+1,j)= hh(i,j)\text{-}\alpha(h(2i,j)+h(2i+2,j)) \quad (16)$$

$$x(i,2j) = l(i,j)\text{-}\beta(h(i,j)+h(i,j\text{-}1)) \quad (17)$$

$$x(i,2j+1) = h(i,j)\text{-}\alpha(x(i,2j)+x(i,2j+2)) \quad (18)$$

Different Values at different stages of DWT Synthesis

Report	Without BZ-FAD (Shift and add multiplier)	With BZ-FAD multiplier
Area (sq.mm)	20654	21984
Power (μw)	572	367

The Discrete wavelet transforms and inverse discrete wavelet transform operates at a maximum clock frequency of 200MHz. the discrete wavelet transforms and inverse discrete wavelet transform is synthesized by using design compiler. The design of DWT and IDWT is checked design for testability. Every time checked timing reports and the power report is taken from the primetime. The architectures for DWT and IDWT perform compression and decompression in $(4N^2\ (1-4-j)+9N)/6$ computation time. The total power consumption of the DWT/IDWT processor is ~0.367mW. The area of the designed architecture in 0.13 micron technology is 112 X 114 um square, and the frequency of operation is 200 MHz for discrete wavelet transform.

VI. Conclusion

In this work low-power architecture for shift-and-add multipliers is proposed and implemented. The conventional architecture has been modified by removing the shift operation of the *B* register (in *A* × *B*), direct feeding of *A* to the adder, bypassing the adder whenever possible, use of a ring counter instead of the binary counter, and removal of the partial product shifter. The BZ-FAD multiplier is further modified using multiplexers and XOR gates, the modified multiplier is modeled and implemented using 130nm technology. The modified multiplier is used in constructing lifting based DWT/IDWT architecture. The DWT/IDWT architecture is modeled and synthesized using TSMC libraries. The BZ-FAD multiplier based DWT/IDWT architecture reduces power dissipation by 30% and operates at 200 MHz. The adders in the lifting based DWT/IDWT can be further improved by replacing the adders by low power adders.

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