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By Prachi Agarwal, Dr. Anil Kumar Sharma & Adesh Kumar
University of Petroleum & Energy Studies, India

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Synthesis Approach of 2D Mesh Network Inter Communication (2D-2D) using Network on Chip

Prachi Agarwal [α], Dr. Anil Kumar Sharma [σ] & Adesh Kumar [ρ]

Abstract - The solution for the multiprocessor system architecture is Application specific Network on Chip (NOC) architectures which are emerging as a leading technology. Modeling and simulation of multilevel network structure and synthesis for custom NOC can beneficial in addressing several requirements such as bandwidth, inter process communication, multitasking application use, deadlock avoidance, router structures and port bandwidth. The paper emphasizes on the network on chip modeling and synthesis of 2D network and intercommunication among multilevel 2D networks. NOC synthesis environment provides transaction level network modeling and address all the requirements together in an integrated chip. In the paper consideration is done for 2D, 8 x 8 network and similar networks are considered which are identified by their specific network address. NOC chip is developed using VHDL programming language. Design is implemented in Xilinx 14.2 VHDL software, functional simulation is carried out in Modelsim 10.1 b, student edition and synthesis process is carried out on Digilent Sparten -3E FPGA.

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I. Introduction

Network on Chip (NoC) [1] [2] [3] is the latest approach to overcome the limitation of bus based communication network. NoC is a set of routers employed in a network, in which different nodes are inter connected with their cores can communicate with each others. In a network data comes in packets and sent to the destination with IP via routers and links [4] . When a packet reaches its destination address, it means it is switched [5] to the IP attached to the router. On-chip communications among different networks is possible using interconnection network topology [5] [6], switching, routing, queuing .flow control [11] and scheduling. Research can be done for n- dimensional topological structures network on chip design. The idea of NoC is derived from distributed computing and large scale computer networks. There are different routing techniques used in NOC design considerations to meet high throughput and cover time to market. Due to big constraints on hardware and memory resources utilization, the routing methods for NoC should be very simple.

According to the need of processors, NoC technology gives chip designer's flexibility in choosing the network topology, according to University of Bologna professor Luca Benini, founder of and scientific advisor for iNoCs, a start-up provider of on-chip interconnection technology. High degree of parallelism and pipelining increases [8] [12] the performance of the system because all the links in the network works simultaneously on different data packets [13]. As the complexity of the system is increasing, NOC is the solution to enhance system performance in comparison to the previous technological architectures such as dedicated, wires, point to point, bridges and shared buses. The scalability of system and throughput [17] [20] will increase because algorithms are designed in such a way that it offers higher degree of parallelism. For example, a mesh NoC topology [18] can function with parallelism and thus is well-suited for multiprocessor SoCs, whose cores must run in parallel. Prototype NoCs by the Electronics and Information Technology Laboratory of the French Atomic Energy Commission's Faust, the Swedish Royal Institute of Technology's Nostrum, and the Technion-Israel Institute of Technology's QNoC work with a mesh topology.

a) Tools Utilized

Design and implementation of mesh network is carried out using Project Navigator ISE 14.2, Xilinx company. It is a tool used to design the IC and to view their RTL (Register Transfer Logic) schematic. Model Sim EE 10.1b student's edition is a tool of Mentor Graphics Company used for simulation and debugging the functionality. The chip implementation is done using VHDL programming language.

The paper is organized as follows: Section I presents the introduction and the tools utilized. Section II describes intercommunication among 2D (8 x 8) mesh networks. Section III describes the FPGA synthesis environment. Section IV describes the Result and Performance Evaluation. Section V presents the Device utilization and timing summary. Conclusion is presented in Section VI.

Author α : M.Tech Scholar, Department of Electronics, Institute of Engineering & Technology, Alwar, Rajasthan India.
E-mail : prachiagarwal_05@yahoo.co.in
Author σ : Professor, Department of Electronics, Institute of Engineering & Technology, Alwar, Rajasthan India. E-mail : aks_826@yahoo.co.in
Author ρ : Assistant Professor, Department of Electronics Engineering, University of Petroleum & Energy Studies, Dehradun India.
E-mail : adeshmanav@gmail.com

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II. Intercommunication among 2D Mesh Networks

Intercommunication among 2D NOC networks can be understood using arbitration logic selection of networks [12]. First understanding, how a 2D networks behaves, then focusing on the intercommunication among 2D networks. 2D NOC [12] follows the cross link which allows addressing any node at any time [11]. A 2D mesh network is connecting multiple inputs to multiple outputs in a matrix form. The 2D NOC architecture is a m × n mesh of switches [10] and resources are placed on the slots formed by the switches. For an m x n architecture there are m nodes on X axis and n nodes on Y axis respectively. Considering an 8 x 8 structure in which 64 nodes can perform intra communication. Node identification is based on the row address and column address [1]. For example, if row address = 000 and column address = 101, node 6 (N_6) is identified. Similarly there is the possibility of identifying any node. Table 1 list the possible node address generation scheme for 2D 8 x 8 structure.

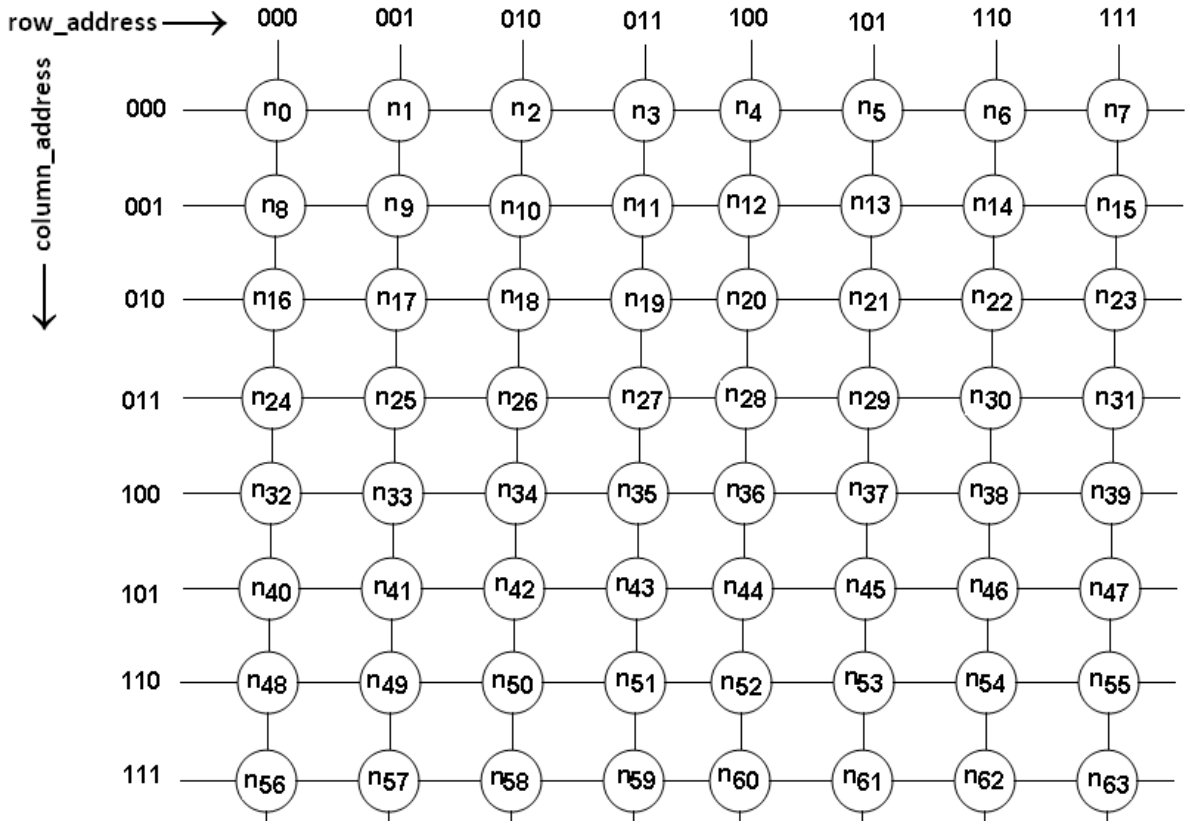

Figure 1 : Two dimensional (2D) cross point topological (8 × 8) structure [12]

Table 1 : Node address generation scheme in 2D structure

Row Address	Column Address							
	000	001	010	011	100	101	110	111
000	n_1	N_2	N_3	N_4	N_5	N_6	N_7	N_8
001	N_9	N_{10}	N_{11}	N_{12}	N_{13}	N_{14}	N_{15}	N_{16}
010	N_{17}	N_{18}	N_{19}	N_{20}	N_{21}	N_{22}	N_{23}	N_{24}
011	N_{25}	N_{26}	N_{27}	N_{28}	N_{29}	N_{30}	N_{31}	N_{32}
100	N_{33}	N_{34}	N_{35}	N_{36}	N_{37}	N_{38}	N_{39}	N_{40}
101	N_{41}	N_{42}	N_{43}	N_{44}	N_{45}	N_{46}	N_{47}	N_{48}
110	N_{49}	N_{50}	N_{51}	N_{52}	N_{53}	N_{54}	N_{55}	N_{56}
111	N_{57}	N_{58}	N_{59}	N_{60}	N_{61}	N_{62}	N_{63}	N_{64}

Considering a architecture in which four 2D (8 x 8) can configured in such a way that they can communicate each other. Each network is identified using its network_address. If network_address is 00 Network 1, network_address is 01 Network 2, network_address is 10 Network 3, and network_address is 11 Network 4 is identified. It is also illustrated using figure 3 and table 2.

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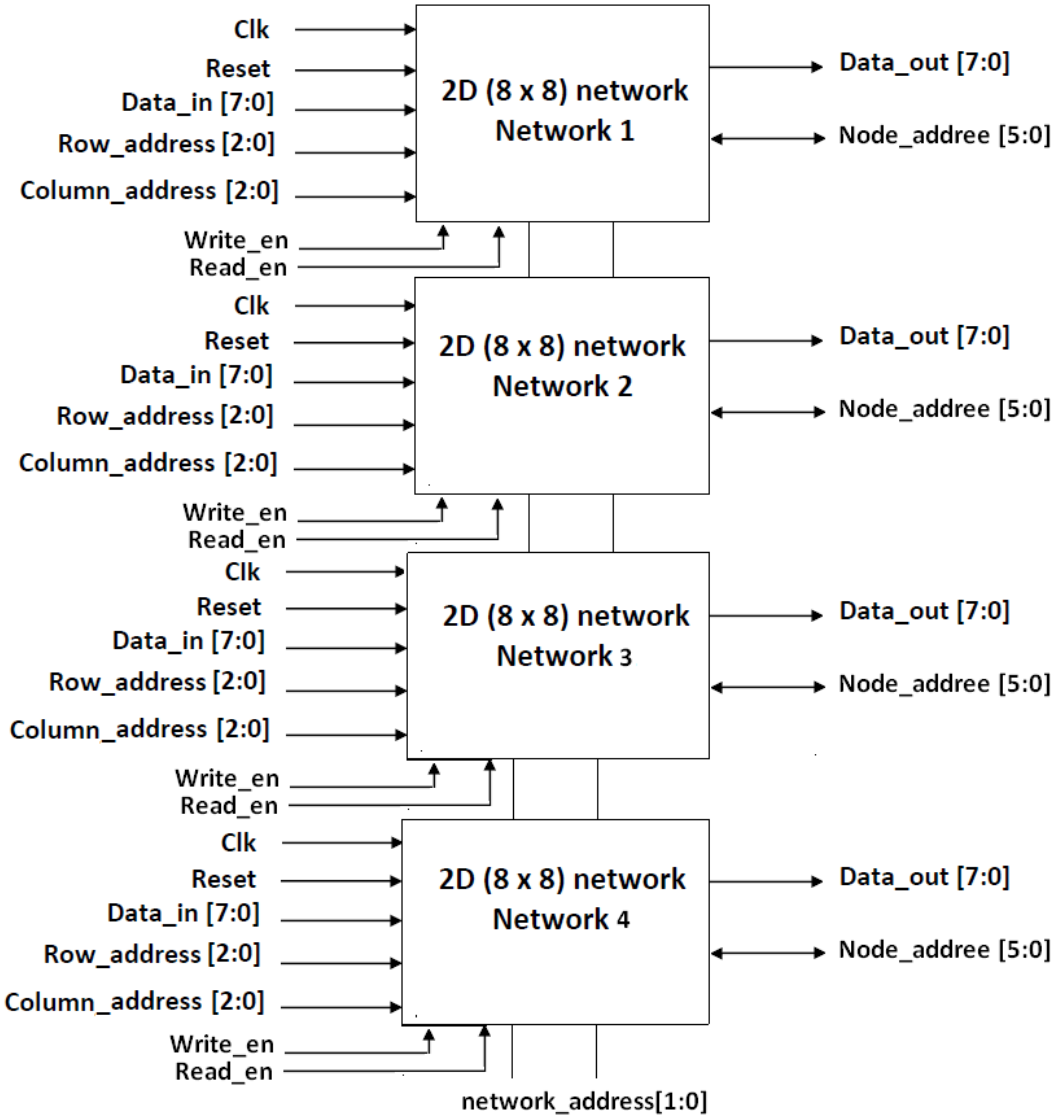

Figure 2 : Intercommunication Mesh Network

Table 2 : Network Selection

Network_Address	Selection Logic
00	Network 1 is selected
01	Network 2 is selected
10	Network 3 is selected
11	Network 4 is selected

III. Result & Performance Evaluation

Figure 3 shows the simulated result for the 8 x 8 intercommunication architecture, which shows 8 bit data transfer for network 1 to network 4. The functional simulation depends on the steps and Modelsim output is extracted after completion of these steps.

a) Simulation Process Sequence

Step 1: reset = 1, clk is used for synchronization and then run.

Step 2: reset = 0, same *clk* is used for synchronization and provide rising edge.

Step 3: Select the address of destination node *Node_address [5:0]* of 6 bits for 8 x 8 structure.

Step 4: Force the value of *row_address* and *column_address* of destination node. For 8 x 8 NOC *row_address[2:0]* and *column_address[2:0]* are of 3 bits.

Step 5: Force the value of *network address [1:0]* of destination network. *network_address [1:0] = "00"* for network 1, *network_address [1:0] = "01"* for network 2, *network_address [1:0] = "10"* for network 2 and *network_address [1:0] = "11"* for network 3.

Step 6: Give the eight bit value of data_in. Force write_en =1 and read_en =0 and then run.

Step 7: Write_en =0 and read_en =1 and run. Desired output on destination is achieved.

When write_en =1 and read_en =0, the data is written in temp variable from the source node, when write_en =0 and read_en =1, the data is read from the temp variable to destination node. Clk is applied at the

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positive edge clock pulse and reset is kept at 1 for the initial state. The Register transfer level (RTL) view of chip is shown yin the figure 4 and the details of each pin is listed in table 3.

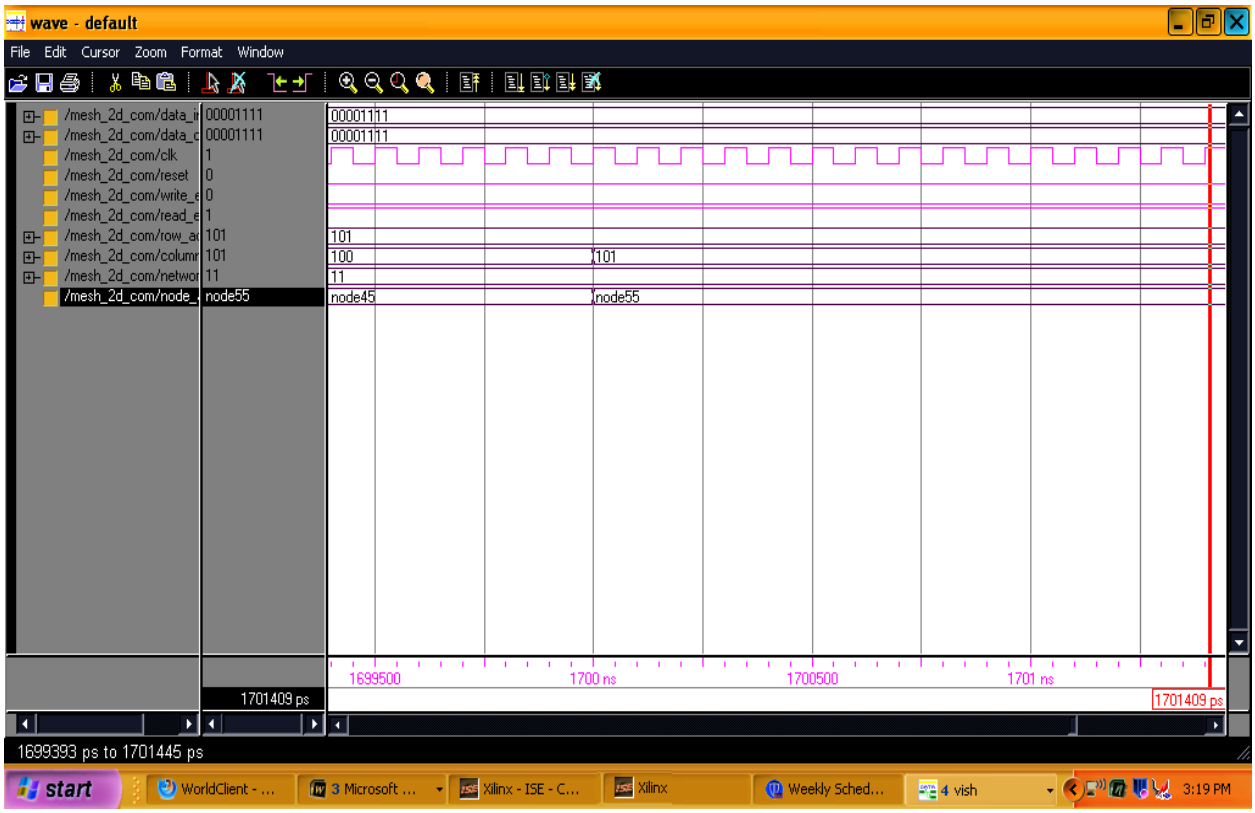

Figure 3 : Modelsim Output of Mesh Intercommunication Network (2D-2D) (8 x 8)

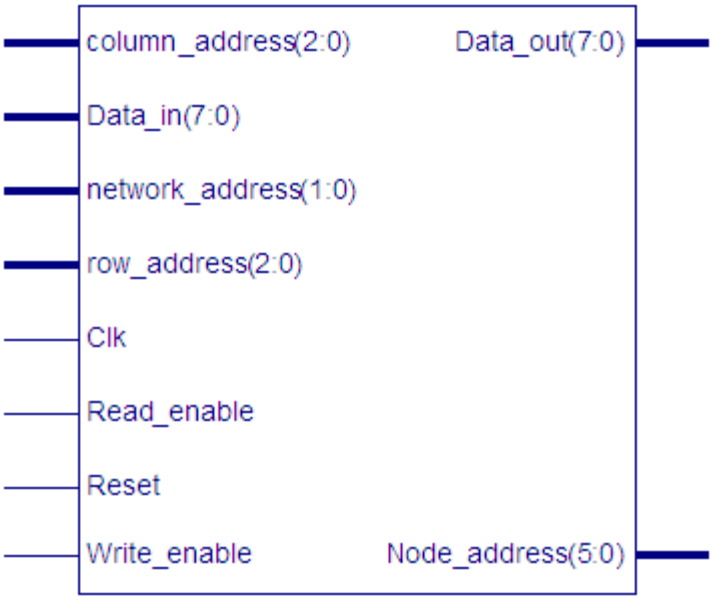

Figure 4 : RTL view of 2D-2D chip

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Table 3 : Design pins and their functional description for (8 x 8) NOC

Pins	Functional Description
reset	used for synchronization of the components by using clk
clk	Provide rising edge of clock pulse
node_address [5:0]	Address of the source and destination node of 6 bits
row_address [2:0]	represents address of the nodes in x direction (3 bits)
column_address [2:0]	represents address of the nodes in y direction (3 bits)
read_en	control signal to read data (1 bit)
write_en	control signal to write data (1 bit)
network_address [1:0]	Selection logic for the network (2 bits)
data_in[7:0]	represents input data in the network (8 bits)
data_out[7:0]	represents 8 bit output data of the destination node (8 bits)

IV. FPGA Synthesis

The Spartan-3E starter kit [21] [22] provides easy way to test the various programs in the FPGA itself, by dumping the 'bit' file of the designed program in Xilinx software into the FPGA and then observing the output .The Spartan 3E FPGA board [8] comes built in with many peripherals that help in the proper working of the board and also in interfacing the various signals to the board itself. Some of the peripherals included in the Spartan 3E FPGA board include: 2-line, 16-character LCD screen used for display the output, PS/2 mouse or keyboard port can be connected to the FPGA, VGA display port [21] used to display various encoded data on screen. The Sparten 3E kit is shown in the figure 5. Switches are the input for *clk, reset*, *row_addressn[2:0]*, *column_address [2:0]*, *network_address [1:0]*. Eight bits data *data_in[7:0]* is also given using switches. These switches are locked into FPGA using user constraint file (UCF). Figure 6 shows the flow of inputs given to FPGA device. Four slide switches and four push-button switches are used to give the inputs to the FPGA board. They can also act as the reset switches for the various program Kit also has four-output, SPI-based on board Digital-to-Analog Converter (DAC) on board which is to be interfaced to give the analog output to the digital data values. Two-input, SPI-based [7] [23] Analog-to-Digital Converter (ADC) with programmable gain preamplifier converts the real world analog signals into digital values.' Image processing inputs are given by the switches of kit and functionally tested on the corresponding LED's output.T he output data is flashed on LEDs. These LEDs are also locked in UCF file [16]. The bit file of the program is burn out in The EPROM of FPGA and corresponding result is shown by blinking LEDs. The output can be shown on Digital storage oscilloscope (DSO). As shown in figure 7. The input data is 10101010, when reset switch = 0, no output is display on DSO. When reset switch =1, output data is 10101010.

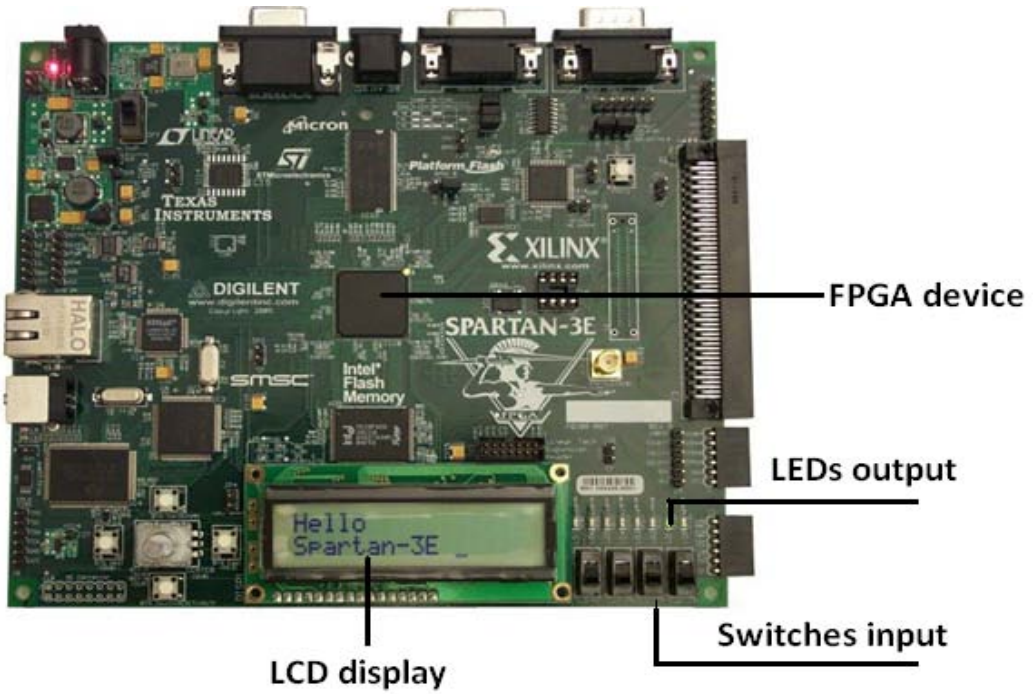

Figure 6 : Sparten-3 FPGA view [21]

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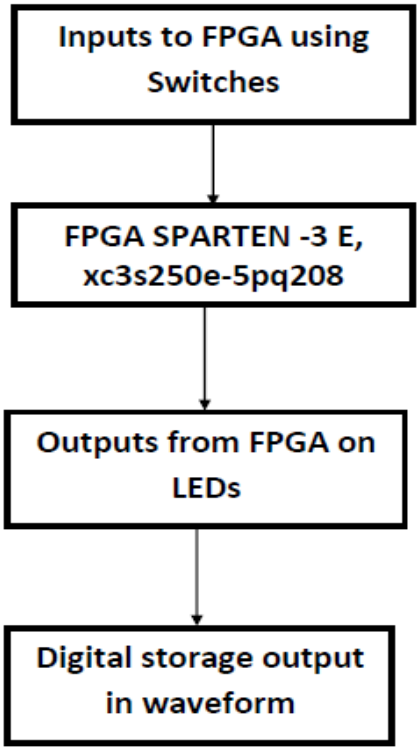

Figure 7 : FPGA syntheis flow on Sparten -3E

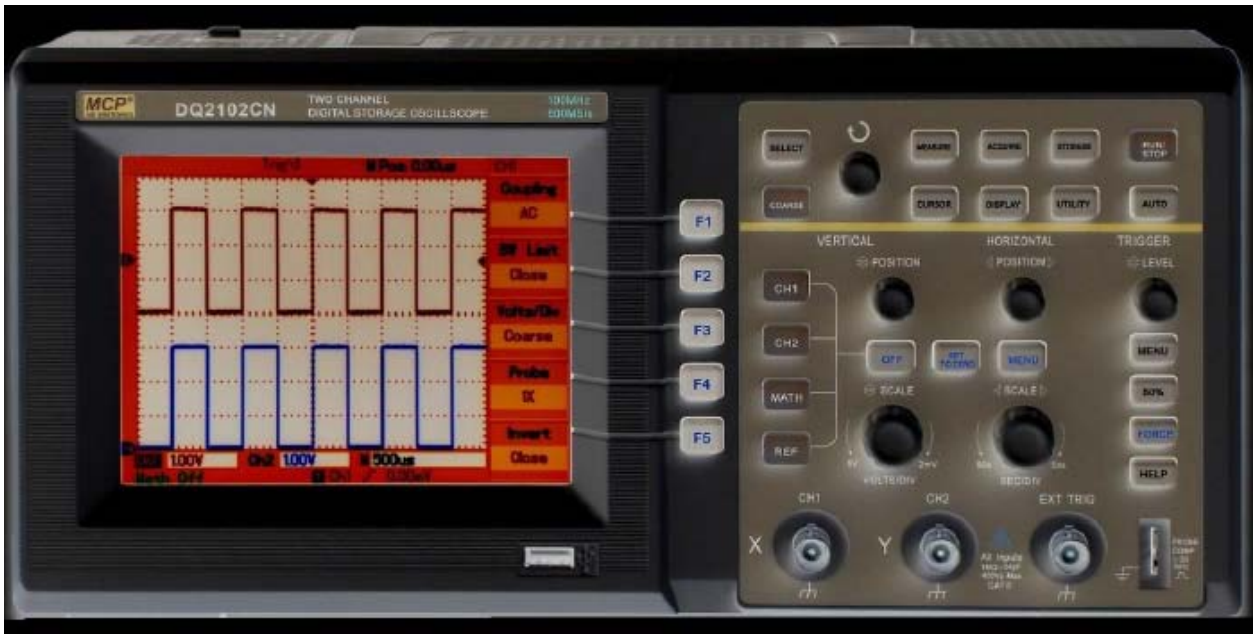

Figure 8 : Synthesis Output on DSO

V. Device Utilization and Timing Summary for 2D NOC

Device utilization report gives the percentage utilization of device hardware for the chip implementation. Timing report generates minimum and maximum time [1] [12] to reach the output. Synthesis report [21] extracted from the Xilinx shows the complete details of device utilization and timing summary.

Selected Device: xc3s250e-5pq208, this device is targeted for FPGA. Device utilization summary for 8 x 8 2D Mesh NOC is shown in table 5 and 6 respectively.

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Table 5 : Device utilization in (2D-2D) Mesh structure

Logic Utilization	Used	Available	Utilization
Number of Slices	335	2448	13 %
Number of Slice Flip Flops	80	4896	1 %
Number of 4 input LUTs	653	4896	13 %
Number of bonded IOBs	31	158	19 %
Number of GCLKs	2	24	8 %

a) Timing Summary for 8 x 8 NOC

Timing details provides the information of delay, minimum period, minimum input arrival time before clock and maximum output required time after clock [1].
Speed Grade: - 5
Minimum Period : 4.937 ns (Maximum Frequency: 202.536 MHz).
Mininput arrival time before clock : 9.977 ns.
Max output required time after clock : 4.368 6ns.
Total memory usage is 127274 kilobytes.

VI. Conclusion

The hardware chip for 2D-2D intercommunication network is modeled and simulated in Xilinx 14.2 successfully. The network size is considered 8 x 8 in which 8 nodes can communication among each other in duplex mode. The data communication from one network to another network is tested for different test cases. The network structure is synthesized in Xilinx supporting Digilent Sparten-3E FPGA kit. Device utilization summary shows Slices utilization 13 %, Number of Slice Flip Flops 1 %, Number of 4 input LUTs 13 %, Number of bonded IOBs 19 % and Number of GCLKs 2 %. Memory utilization is 127274 kB and maximum frequency 202.536 MHz. These parameters are optimized parameters. The proposed architecture is applicable for inter and intra communication among networks. In future we can enhance the data size, and number of nodes supporting to the networks.

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