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The Implementation of DMA Controller on Navigation baseband SoC

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The Implementation of DMA Controller on Navigation baseband SoC

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Abstract- This article discusses the architecture design of DMA controller on high performance GPS receiver based on RTEMS. We achieve the optimal integration of DMA IP and navigation baseband system. We designed the hardware architecture of DMA IP and make full use of hardware performance with the idea of multiplexing. We use register and FIFO buffer to achieve read-write control. And we design the DMA controller with Verilog HDL. Finally we verify the design on Altera Cyclone4 FPGA. The result demonstrates that DMA controller can ease the CPU's burden and shorten the acquisition & tracking time thus improving the performance of the whole system.

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I. Introduction

DMA controller is the core component of the SoC. Through controlling the data transfer from memory to peripheral independently, it can greatly alleviate the CPU's burden and improve the efficiency of data processing. Therefore the design of DMA controller directly affects the overall performance of SoC chip. Similar to the design of other integrated circuit IP, DMA design should also consider the reusability of DMA IP and balance the operation speed and circuit area, at the same time achieving good integration with SoC. According to the design goal, the domestic and foreign scholars have conducted in-depth research. Literature [2] designs a configurable multi-channel DMA controller, but it doesn't consider the size of FIFO BUFFER, which may causes the waste of resources. The design in literature [3] can alleviate the CPU's burden and improve the data transmission rate between peripherals, but it is only a single channel structure thus lack of generality. Literature [4] designs a specific data path for DMA data transfer. Although it avoids the limitation of AHB bus, achieving parallel transmission of multi-path data, but making the internal SoC bus timing complicated and consideration must be given to the arbitration of memory R/W between bus and special data bus. In this paper, according to the large amount of data of high real-time navigation applications, we design the DMA controller implementation in navigation baseband SoC. The design shortens the first positioning time of the chip and improves its whole performance.

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Our Navigation Baseband SoC chooses LEON3 processor from Aeroflex Gaisler Corporation and it's based on SPARC V8 architecture. The on-chip bus is the AMBA2.0 of ARM Corporation, which ensuring the data transmission flowing. In order to realize the fast acquisition and tracking of navigation signal, the chip has 2 built-in acquisition and tracking module. The chip uses the on-chip SRAM controller to realize the real-time data storage. We use RTEMS 4.10 as the operation system, making the system with good real-time performance. At the same time, the driver program of RTEMS relative to LINUX and other embedded operating system is simpler.

II. Design of the System Architecture

The whole system architecture uses classical SoC architecture based on AMBA bus, as Figure 1 shows. AMBA2.0 AHB bus connects on-chip CPU, memory and other high-speed devices. It achieves W/R operation between SRAM, SDRAM and FLASH ROM through memory controller. Acquisition and tracking module are connected to the DMA controller, and they store the generated data to RAM through DMA module.

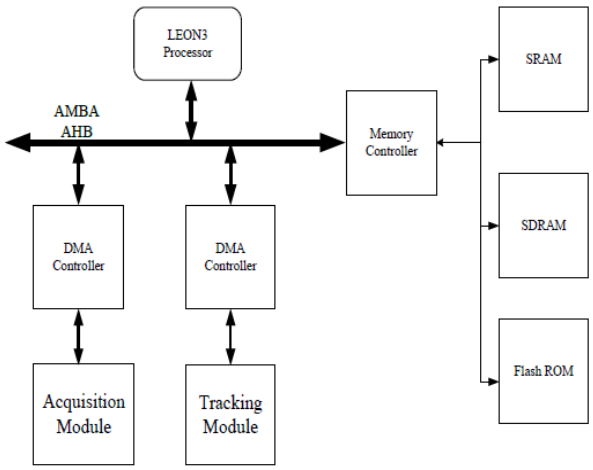

Fig.1 : Navigation Baseband Architecture

III. Design of the System Architecture

As Figure 2 shows, DMA module is mainly made of buffer, interrupt generating logic module, register, arbitration module, bus W/R module and corresponding interfaces. Acquisition and tracking module connects into DMA module through parallel data interfaces, and store the generating data to each

FIFO buffer. The size of the buffer is fixed and connects to a interrupt generating circuit. When any of the buffers is full, it generates corresponding interrupt signal and requires interrupt through the AMBA bus.

The DMA controller has three groups of control registers. Each group includes a 32 bit control register, source address register, destination address register and data register. It achieves memory W/R operation through Memory Mapping by AHB bus and AMBA bus controller. Each signal generated by control register is sent to fixed priority arbitrator for arbitration first, the arbiter controls a mux to generate corresponding control signal.

Bus R/W module is made of AMBA writing module and AMBA reading module. It transfers corresponding address data through AMBA bus timing specification.

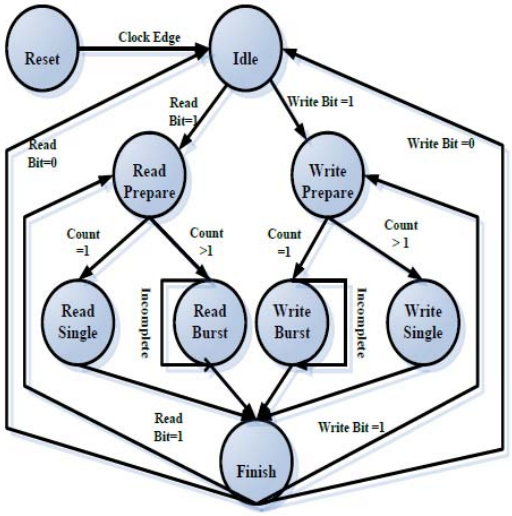

Fig. 2 : DMA Controller Architecture

IV. Design of the fifo Module

Since the The data generation rate of acquisition and tracking module is much slower than the bus read and write clock, In order to speed up the data transmission rate of DMA, we consider the use of two way asynchronous FIFO as a buffer.

The structure of the FIFO is shown as Figure 3. Because it uses different clocks to read and write, so we use Dual-port RAM as memory module. The word length and depth of storage of dual port RAM is according to the AD parameter RF front-end sampling. In order to solve the problem of metastable clock domain data transmission, FIFO read and write pointer is encoded with the gray code. Through the multi-level register transfer DMA controller can reduce the probability of metastable.

The comparison algorithm of full/empty of FIFO pointer references Clifford E. Cummings' paper. That is to construct a pointer which width is N+1, depth is 2^N bytes. Read and write pointer is represented with the gray code. The first two bits are not the same. When the FIFO is full the two LSB gets the same. When the pointer is exactly equal, FIFO is empty.

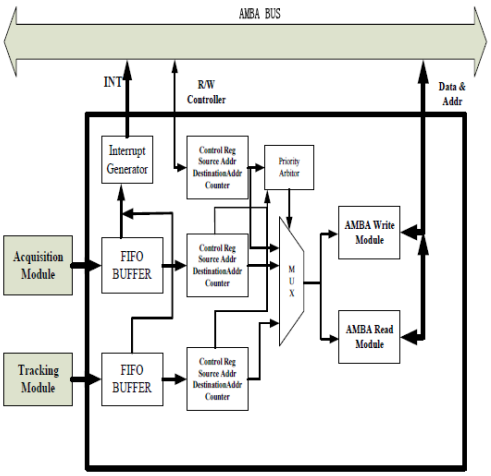

Fig.3 : FIFO module architecture

V. The Workflow of dma Controller

Initially, the bus is idle, waiting for the DMA transmission request. When the control register Read or Write bit is 1, the DMA controller goes into corresponding reading or writing ready state. According to the setting value of the counter, DMA then decided to adopt the single or burst mode to read and write bus. After read and write data process the controller goes into finish state. Finally it determines whether goes into the read and write cycle according to the value of control register. The workflow is shown as Figure4.

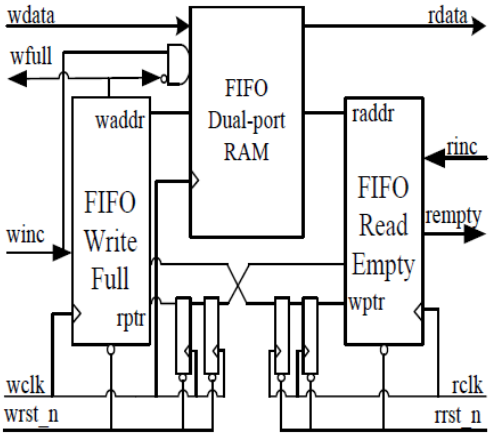

Fig. 4 : FSM Diagram

VI. The Software and Hardware Co-Verification of dma ip

We use Verilog HDL to build the DMA controller, and Altera QuartusII for integrated debugging. After downloading the design to Altera Cyclone4 EP4C115F2 9C7 FPGA, we can get the correct gate level netlist. The DMA controller consumes totally 6348 LE after

synthesize. We simulate the data transmission process by software interruption on RTEMS. Figure 5 shows the real-time read-burst mode waveform through Altera's Signal Tap on FPGA. We can see that DMA module successfully achieves data R/W in burst mode.

Fig. 5 : read burst module verification waveform

VII. Application

In order to investigate the effect of DMA solution brings, in this paper, we research in DMA and non DMA (FIFO interrupt) two cases the first positioning time (TTFF) baseband SoC requires. Through the test to different S/N ratio of the received signal and the dynamic condition, we can get the experiment data and conclusion.

a) Experiment Design

The first positioning time of navigation baseband SoC is also called cold start time. The system powers on and initialize without any historical information under a cold start condition. And then it attempts to locate and lock the satellite. Because of the lack of prior information, it will take a long time. System uses a method similar to the polling, locking the signals from all the satellites.

The system performs four steps from power on to the output of position data: system initialization – acquisition – tracking – position calculation. At the same time it interact with the user. In the four step, the processor is mainly responsible for initializing the operating system, position solution and human-computer interactive task. The DMA controller can be used instead of the processor, responsible for store the data generated by acquisition and tracking module into RAM. Therefore the processor can focus on the position solution and human-computer interactive task and the first positioning time (TTFF) is shortened.

In order to comprehensively study the performance of the system, the test experiment selects three different IF GPS signal as signal source. The GPS S/N ratio is 42db-Hz under the first condition. The system acceleration is 0g. The GPS S/N ratio is 42db-Hz under the first condition. But the system acceleration is 20g. The GPS S/N ratio is 34db-Hz under the first condition. The system acceleration is 0g. The test results is shown in Table 1 and Table 2.

Table 1: Non-DMA Mode TTFF statistics

GPS S/N dB/Hz	system acceleration / m/s^2	TTFF / s
42	0	26.4
42	20	30.2
34	0	28.6

Table 2 : DMA Mode TTFF statistics

GPS S /N dB/Hz	system acceleration / m/s^2	TTFF / s
42	0	25.3
42	20	28.1
34	0	26.8

b) Data analysis

We can draw from Table 1 and Table 2 that: Under the first condition, the system is under a low dynamic environment with high signal-to-noise ratio, since that the TTFF both in DMA and non-DMA mode is relatively short. And the DMA mode takes 1.1 s less time than non-DMA mode. So, DMA controller sets CPU free from busy data transforming task, making it to have more free time to perform other tasks and shortening the TTFF.

Under the second condition, the system is under a high dynamic extreme environment, which greatly increases the acquisition and tracking difficulty. Here the DMA mode takes 2.1 s less time than non-DMA mode. Compared to the first condition, Using DMA method to shorten the TTFF effect is more obvious.

Under the third condition, the system is under a environment with low signal-to-noise ratio, which also increases the acquisition and tracking difficulty. TTFF in DMA mode is 28.6s, in non-DMA mode is 26.8s, which is both longer than the first condition. Here the DMA mode takes 1.8 s less time than non-DMA mode. Implementing DMA also has the obvious effect on reducing TTFF.

The experiment proofs that: The DMA controller can effectively reduce navigation baseband SoC CPU's load, shorten TTFF.

VIII. Conclusion

SoC technology has developed rapidly in recent years, represent the future development trend of IC. As a complex system composed by multiple IP, the single component design of GPS baseband SoC must fully consider the overall system hardware and software

integration in order to play the best performance of the whole system. In this paper, the DMA IP from the system view, it uses FIFO BUFFER and interrupting mechanism to realize the good combination of acquisition and tracking module. With the control register group developer can easily program the DMA controller under the RTMES real-time operating system. The FPGA Experiments show that this design can realize the data read and write control based on AMBA bus, reduce the burden of CPU.

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