Design and Analysis of Low Run-Time Leakage in a 13 Transistors Full Adder in 45nm Technology

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GJCST-A Classification: G.4, B.3.2

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Abstract- In this paper a new full adder is proposed. The number of Transistors used in the proposed full adder is 13. Average leakage is 62% of conventional 28 transistor CMOS full adder. The leakage power reduction results in overall power reduction. The proposed full adder is evaluated by virtuoso simulation software using 45 nm technology of cadence tools.

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I. INTRODUCTION

In this paper various 1-bit full adders are considered for leakage analysis. A 13 Transistor Full adder is designed and analysed for low leakage. Full adders considered for analysis in this paper are Complimentary MOS implementation of full adder[29], Mirror full adder[29], Transmission gate full adder[29], Manchester full adder[29], Complimentary pass transistor logic full adder, Low power Full adder, Lean integration with pass transistor full adder, 20 Transistor Transmission gate full adder, Improved 14 transistor Full adder, SERF Full adder, GDI XOR full adder, Low power Full adder, Lean integration with pass transistor full adder, 20 Transistor Transmission gate full adder, Improved 14 transistor Full adder, SERF Full adder, GDI XOR full adder, 10 transistor full adder, 9A full adder, 9B full adder, 13A full adder, 8 transistor full adder and proposed 13 transistor full adder.

CMOS 28 Transistor Full Adder: Conventional CMOS Full Adder consists of 28 transistors as shown in fig.1. From the following equations one can design CMOS 28 Transistor full adder circuit[29].

\[ C_0 = AB + [A + B]C \] (1)
\[ S = ABC_i + C_0(A + B + C_i) \] (2)

Mirror Adder: The fig.2. shows Mirror Adder. An improved adder circuit, also called as "Mirror Adder"[2]. This is a clever implementation of the propagate/generate/delete function when either D or G is high, C0 is set VDD of Gnd, respectively. When the conditions for propagate are valid (or P is 1), the incoming carry is propagated to CO.

Transmission Gate Full Adder: A full adder can be designed to use MUX and XOR. While this impractical in a complementary CMOS implementation, it becomes attractive when MUX and XORs are implemented as transmission gates[4]. The Transmission Gates Full Adder is as shown in fig.3.

Manchester Full Adder: The main idea of designing this adder is to optimize carry chain till some extent in TG full adder by adding generate and delete signals[5]. The propagate path is unchanged, and it passes Cin to the Cout output if the propagate signal is true. If the propagation condition is not satisfied, the output is either pulled low by Di signal or pull up by Gi. Manchester Full adder[29] as shown in fig.4.

Complimentary pass transistor logic: The CPL Full Adder has 18 transistors[33] and is based on NMOS passtransistor logic as shown in fig.5 and fig.6.

Low Power Full Adder: This novel adder [43] cell has 16 transistors. It is based on the 4-transistor implementations.

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LEAP Full Adder: The pass transistor based cell library and synthesis tool are constructed to clarify the potential of top down pass transistor logic. The entire scheme is called LEAP [43] (Lean Integration with Pass-transistor). The LEAP Full adder is as shown in Fig. 8.

20 Transistor Transmission Gate Full Adder: Transmission gate approach [36] which is another widely used CMOS design style to implement digital function has been discussed. Transmission gate based implementation is similar to pass transistor with the difference that transmission gate logic uses NMOS and PMOS transistors whereas pass transistor logic uses only one type of transistor i.e. either NMOS or PMOS. 20 Transistor Transmission Gate Full adder is as shown in Fig. 9.

Improved 14 Transistor Full Adder: The 14T full adder [40] contains a 4T PTL XOR gate an inverter and two transmission gates based multiplexer designs for Sum and Carry signals as shown in Fig. 10. The circuit is simpler than the conventional adder. This circuit has 4 transistor XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously...
to generate Sum and Cout. 14 Transistor full adder is as shown in fig.10.

![Figure 10: 14T Full Adder][40]

**SER Full Adder:** SERF adder[11] reuses charge by the energy recovering logic and hence consumes less power than non-energy recovering logic. SERF adder has no direct path to the ground, therefore power dissipation is reduced. The charge stored at the load capacitance is reapplied to the control gates. The joint effect of these two things makes the SERF adder an energy efficient design. SERF Full adder as shown in fig.11.

![Figure 11: Static Energy Recovery Full Adder][11]

**GDI XOR Full Adder:** GDI[39] technique is implemented to design a high performance and low power full adder. GDI cell contains three inputs- G (common state input of NMOS and PMOS), N (input to the source or drain of NMOS) and P (input to the source or drain of PMOS). GDI XOR Full adder as shown in fig.12.

![Figure 12: Gate diffusion XOR Full Adder][39]

**10 Transistor Full Adder:** Full adder using 10T uses more than one logic style for the implementation and it is called as Hybrid logic design style. The number of transistors count is 10. 10 Transistor Full adder[41] is as shown in fig.14.

![Figure 14: 10T Full Adder][41]

**9A Full Adder:** The 9A Full adder[38] shown in below figure implemented using four transistor static energy recovery XNOR, four transistor ground less XNOR and 2:1 multiplexer. 9A Full adder as shown in fig.15.

![Figure 15: 9A Full Adder][38]

XOR gate has no power supply, it is called Powerless XOR, or PXOR. A new XNOR gate is named as Groundless XNOR or GB.
Cout is designed using multiplexer. 13A Full adder is as shown in fig. 17.

**Figure 16: 9B Full Adder[38]**

**Figure 17: 13A Full Adder[11]**

**8 Transistor Full Adder**: It is built using three multiplexers and one inverter[42]. The inverter in the circuit speeds up propagation of Cout and also provides complemented Cout signal required for generation of Sum. The xor gate is replaced by xnor gate. So the need for inverter is avoided. This reduces the transistor count to 8. The transistor level implementation of the eight transistor full adder is shown in fig.18.

**Figure 18: 8T Full Adder[42]**

**Proposed 13 Transistors Full Adder**: After having detail analysis we started to work by undertaking different approach so that we can reduce leakage till some extent along with increase in swing and reduce in average power. Then initially we started on investigating on output swing and came to know that by replacing A, B it is possible to increase the swing as well as decrease in leakage along with average power. It differs from complementary CMOS in that the source side of the MOS transistor is connected to an input line instead of being connected to power lines. Another important difference is that only one PTL network (either NMOS or PMOS) is sufficient to perform the logic operation. In this circuit sum is calculated from output carry. This proposed full adder resulted low leakage as well as low power as comparing with existed full adder.

**Figure 19: Proposed 13T Full Adder**
II. SIMULATION RESULTS

Simulation results are presented in Table I for the analysis. The table shows the comparison of average leakage power, peak leakage power, average power and peak power in 28 Transistor full adder, Mirror, TG, Manchester, CPL, LEAP, 20T, 14T, SERF, GDI XOR, GDI XNOR, 10T, 9A, 9B, 13A, 8T and proposed 13 Transistors full adders.

<table>
<thead>
<tr>
<th>Full Adders</th>
<th>Average Leakage</th>
<th>Peak Leakage</th>
<th>Average Power</th>
<th>Peak Power</th>
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<tr>
<td>28T</td>
<td>313.2nW</td>
<td>34.83uW</td>
<td>351.1nW</td>
<td>36.26uW</td>
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<tr>
<td>Mirror</td>
<td>288.3nW</td>
<td>37.48uW</td>
<td>317.0nW</td>
<td>28.75uW</td>
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<td>TG</td>
<td>8.9uW</td>
<td>53.80uW</td>
<td>41.96uW</td>
<td>69.14uW</td>
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<td>Manchester</td>
<td>9.013uW</td>
<td>72.52uW</td>
<td>42.32uW</td>
<td>115.32uW</td>
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<td>CPL</td>
<td>9.13uW</td>
<td>44.14uW</td>
<td>39.83uW</td>
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<td>LP</td>
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<td>73.88uW</td>
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<td>LEAP</td>
<td>11.91uW</td>
<td>44.62uW</td>
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<td>20T</td>
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<td>720nW</td>
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<td>14T</td>
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<td>44.14uW</td>
<td>39.83uW</td>
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<td>SERF</td>
<td>158nW</td>
<td>10.90uW</td>
<td>252nW</td>
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<td>GDI XOR</td>
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<td>15.53uW</td>
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<tr>
<td>GDI XNOR</td>
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<td>31.97uW</td>
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<tr>
<td>10T</td>
<td>8.85uW</td>
<td>33.95uW</td>
<td>12.45uW</td>
<td>27.39uW</td>
</tr>
<tr>
<td>9A</td>
<td>8.85uW</td>
<td>33.95uW</td>
<td>19.07uW</td>
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<tr>
<td>9B</td>
<td>15.76uW</td>
<td>34.95uW</td>
<td>20.36uW</td>
<td>32.70uW</td>
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<tr>
<td>Proposed 13T</td>
<td>196.4nW</td>
<td>17.10uW</td>
<td>12.67uW</td>
<td>52.70uW</td>
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</table>

III. CONCLUSION

Below 70 nm technologies run-time leakage power dominates the dynamic power. So one should come up with new full adder which consumes less leakage power compared to dynamic power one such attempt is discussed in this paper.

IV. ACKNOWLEDGMENT

My sincere thanks to my guides Dr. K. Manjunathachari and Dr. K. Lalkishore for their valuable support and encouragement.

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