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Highlights

Building a Scalable UVM

Testbench for GPU Compute Units

Silent Data Errors in GPUs

Challenges and Mitigation in Modern

Discovering Thoughts, Inventing Future

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Building a Scalable UVM-based Test Bench for GPU Compute Units

By Mohit Gupta

Abstract- Modern graphics processing units have evolved into complex massively parallel computing engines that demand sophisticated verification methodologies capable of validating thousands of concurrent threads executing across intricate memory hierarchies and specialized execution pipelines. Traditional verification approaches struggle to adequately address the unique challenges posed by Single Instruction, Multiple Thread execution models, dynamic thread scheduling, and complex interactions between compute units and multi-level cache systems. This article presents a comprehensive Universal Verification Methodology-based testbench architecture specifically designed for GPU compute unit verification, addressing critical gaps in existing verification practices through innovative SIMT-aware stimulus generation, integrated memory subsystem modeling, and scalable test generation frameworks. The proposed framework combines established UVM principles with GPU-specific verification techniques, creating a modular and reusable architecture that supports diverse configurations while maintaining systematic coverage collection and intelligent corner case detection.

Keywords: *GPU verification, universal verification methodology (UVM), SIMT execution model, parallel architecture testing, semiconductor validation.*

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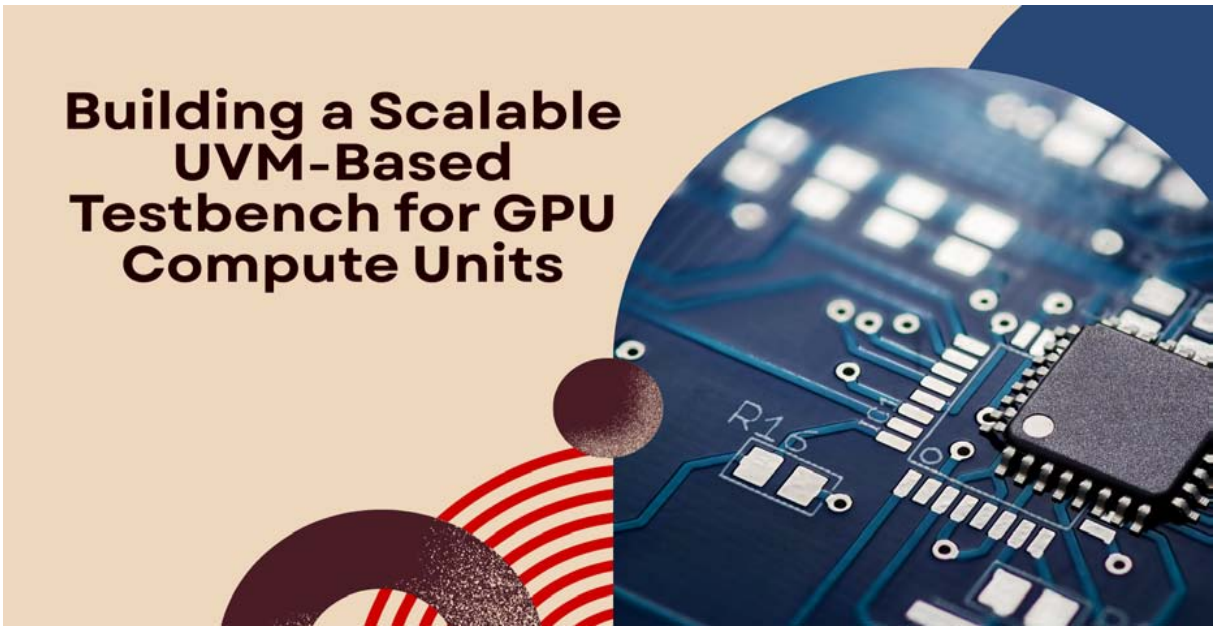
Building a Scalable UVM-based Test Bench for GPU Compute Units

Mohit Gupta



Figure

Abstract- Modern graphics processing units have evolved into complex massively parallel computing engines that demand sophisticated verification methodologies capable of validating thousands of concurrent threads executing across intricate memory hierarchies and specialized execution pipelines. Traditional verification approaches struggle to adequately address the unique challenges posed by Single Instruction, Multiple Thread execution models, dynamic thread scheduling, and complex interactions between compute units and multi-level cache systems. This article presents a comprehensive Universal Verification Methodology-based testbench architecture specifically designed for GPU compute unit verification, addressing critical gaps in existing verification practices through innovative SIMT-aware stimulus generation, integrated memory subsystem modeling, and scalable test generation frameworks. The proposed framework combines established UVM principles with GPU-specific verification techniques, creating a modular and reusable architecture that supports diverse configurations while maintaining systematic coverage collection and intelligent corner case detection. Extensive experimental evaluation across representative GPU workloads demonstrates substantial improvements in verification quality, debug efficiency, and development productivity compared to traditional approaches. The architecture's parameterized design enables seamless adaptation across different GPU generations while its extensible structure provides a foundation for future verification challenges, including AI accelerators and chiplet-based architectures.

Keywords: *GPU verification, universal verification methodology (UVM), SIMT execution model, parallel architecture testing, semiconductor validation.*

I. Introduction

The rapid evolution of graphics processing units (GPUs) from specialized graphics accelerators to general-purpose computing engines has fundamentally transformed the semiconductor landscape. Modern GPU architectures feature thousands of parallel compute units executing complex workloads ranging from artificial intelligence training to high-performance scientific computing. These massively parallel systems demand sophisticated verification methodologies that can effectively validate their intricate hardware designs before silicon fabrication.

The Verification Gap: While CPU and DSP designs benefit from mature UVM frameworks optimized for sequential and moderately parallel architectures, GPU verification lacks standardized methodologies tailored for massive parallelism. This gap becomes critical given that verification consumes more design effort in modern semiconductor projects [1], making efficient GPU verification essential for industry competitiveness.

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Contemporary GPU compute units present unprecedented verification challenges due to their Single Instruction, Multiple Thread (SIMT) execution model, hierarchical memory systems, and dynamic thread scheduling mechanisms. Traditional verification approaches often struggle to adequately model the complex interactions between thousands of concurrent threads, multi-level cache hierarchies, and specialized execution pipelines that characterize modern GPU architectures.

The Universal Verification Methodology (UVM) has emerged as the industry standard for creating modular, reusable verification environments. However, applying UVM to GPU compute unit verification requires specialized techniques that address the unique characteristics of massively parallel architectures. Conventional UVM test benches typically target sequential or moderately parallel designs, leaving a significant gap in methodologies specifically tailored for GPU-scale parallelism.

Economic Stakes: With mask re-spins costing tens of millions of dollars and GPUs consuming HPC workloads [2], the economic imperative for comprehensive pre-silicon validation has never been greater. Current verification practices in the GPU industry often rely on custom, design-specific test benches that lack the modularity and reusability benefits of standardized UVM frameworks, leading to substantial development overhead and difficulties scaling verification efforts across GPU generations.

This work introduces a comprehensive UVM-based test bench architecture specifically designed for GPU compute unit verification. The proposed framework addresses key challenges in SIMT execution modeling, memory hierarchy validation, and scalable test generation while maintaining the modularity and reusability principles that make UVM valuable for complex system verification.

II. Background and Related Work

a) GPU Architecture Fundamentals

Table 1: UVM Component Architecture for GPU Verification [2, 5]

Component	Traditional UVM Role	GPU-Specific Enhancement	Key Features
Agent	Interface management	SIMT-aware stimulus control	Warp-based transaction handling
Driver	Stimulus generation	Thread-level instruction streams	Parallel execution modeling
Monitor	Response collection	Multi-thread result capture	Performance metric tracking
Scoreboard	Result verification	Parallel checking mechanisms	Memory coherency validation
Sequencer	Test coordination	Warp scheduling simulation	Dynamic thread management

Modern GPU architectures employ the Single Instruction, Multiple Thread (SIMT) execution model, where groups of threads called warps execute identical instructions across different data elements. Each streaming multiprocessor (SM) contains multiple CUDA cores organized into execution units that process warps simultaneously. The compute unit organization includes specialized function units, register files, and shared memory banks that enable efficient parallel processing.

The memory hierarchy spans multiple levels, from per-thread registers to shared memory accessible within thread blocks, and extends to global memory accessed by all threads. Thread scheduling mechanisms dynamically manage warp execution, handling divergent branches through serialization and reconvergence techniques. Multi-SM architectures present significant parallelism challenges as hundreds of SMs must coordinate memory accesses while maintaining coherency across thousands of concurrent threads.

b) Universal Verification Methodology (UVM) Overview

UVM provides a standardized framework built on System Verilog that emphasizes modularity, reusability, and systematic verification planning. Core architectural components include agents, drivers, monitors, and scoreboards that work together to create comprehensive verification environments. The methodology promotes layered test bench architectures where stimulus generation, checking, and coverage collection are clearly separated.

Constrained-random verification generates diverse test scenarios through intelligent randomization within specified constraints, while coverage-driven testing ensures verification completeness through systematic metric tracking [3]. Industry adoption has grown substantially as organizations recognize UVM's ability to reduce verification time and improve test quality across complex system designs.

c) Current GPU Verification Approaches

Traditional verification methodologies for parallel architectures often employ directed testing combined with basic random stimulus generation. These approaches struggle with the massive state spaces inherent in GPU designs, leading to incomplete corner case coverage. Existing UVM applications in CPU and DSP verification have demonstrated success in

sequential and moderately parallel contexts but require significant adaptation for GPU-scale parallelism.

Current GPU verification practices frequently rely on custom test benches developed for specific projects, resulting in limited reusability and substantial redevelopment overhead. The gaps in current practices include inadequate SIMT modeling, insufficient memory hierarchy validation, and a lack of scalable test generation frameworks designed for massively parallel architectures.

d) Related Research and Industry Solutions

Academic contributions to parallel architecture verification have explored formal methods and model checking techniques, though scalability remains challenging for GPU-sized designs. Commercial tools from major EDA vendors (Synopsys, Siemens, Cadence) provide some GPU-specific features, but comprehensive frameworks tailored for compute unit verification remain limited [4].

Historical Context: Early GPU generations suffered from memory ordering violations and divergence handling issues that escaped pre-silicon validation, highlighting the critical need for specialized verification approaches. Comparative analysis reveals that while traditional verification approaches work well for smaller parallel systems, they fail to scale effectively to the thousands of threads typical in modern GPU architectures.

Table 2: Verification Challenge Categories and Solutions [3, 4]

Challenge Category	Traditional Approach Limitations	Proposed Solution	Implementation Benefit
Thread Divergence	Sequential modeling inadequate	Sequential modeling inadequate	Comprehensive branch coverage
Memory Hierarchy	Simple memory models	Multi-level cache simulation	Realistic timing validation
Scalability	Resource constraints	Parameterized architecture	Efficient large-scale testing
Corner Cases	Random testing gaps	Intelligent stimulus generation	Enhanced bug detection
Reusability	Design-specific testbenches	Modular UVM framework	Cross-project deployment

III. Challenges in GPU Compute Unit Verification

a) SIMT Execution Modeling Complexity

Thread divergence occurs when threads within a warp follow different execution paths due to conditional branches, requiring sophisticated modeling to capture all possible divergence patterns. Convergence behavior must be accurately simulated as threads rejoin common execution paths after divergent sections complete.

Warp-level scheduling involves complex arbitration policies that determine execution order among ready warps, while register file and shared memory interactions create intricate dependencies that traditional verification approaches struggle to model effectively. These interactions become particularly challenging when multiple warps access shared resources simultaneously.

b) Scalability Requirements

Multi-SM and multi-thread verification present exponential growth in verification complexity as thread counts increase. Performance considerations for large-scale simulation often limit the practical verification scope, forcing engineers to use reduced-scale models that may miss critical interactions occurring only at full scale.

Resource management becomes critical when simulating thousands of concurrent threads, while test parallelization requires careful coordination to maintain deterministic behavior across distributed verification runs [5]. Memory bandwidth limitations in simulation environments further constrain the achievable verification scale.

c) Memory Hierarchy Integration

L1 cache and shared memory modeling must accurately represent timing, capacity, and coherence behavior to enable realistic verification scenarios. *Bank conflicts* represent a classic GPU hazard where multiple threads simultaneously access the same memory bank, creating performance bottlenecks that must be systematically verified.

Global memory access patterns involve complex address translation and banking schemes that significantly impact performance and correctness. Cache coherency and memory consistency verification require sophisticated protocols that ensure data integrity across thousands of concurrent memory operations.

d) Coverage and Corner Case Detection

Identifying critical verification scenarios requires understanding the complex interactions between thread scheduling, memory access patterns, and execution pipeline behavior. Warp divergence corner cases often involve specific combinations of branch conditions and data patterns that occur infrequently in random testing.

Memory hazard detection encompasses various conflict scenarios, including bank conflicts, cache line contention, and memory ordering violations that can compromise system correctness. Validation of these hazards demands systematic coverage collection and intelligent stimulus generation beyond conventional verification capabilities.

IV. Proposed UVM-Based Test Bench Architecture

a) Overall Framework Design

The proposed test bench architecture follows established modular design principles, organizing components into distinct layers that separate stimulus generation, monitoring, and checking functions. The component hierarchy builds upon standard UVM patterns while incorporating GPU-specific extensions for SIMT execution modeling and memory subsystem integration.

The framework implements comprehensive parameterization capabilities that allow dynamic configuration of thread counts, SIMD widths, and memory hierarchy parameters without requiring testbench restructuring. Configurability features extend to execution models, enabling seamless adaptation across different GPU architectures and compute unit configurations.

b) SIMT-Aware Agent Design

Thread-level stimulus generation incorporates intelligent randomization that respects SIMT execution constraints while exploring diverse execution patterns. The agent architecture generates coherent instruction streams that model realistic GPU workloads, including vector operations, memory access patterns, and control flow scenarios typical in compute kernels.

Warp-based sequence modeling captures the collective behavior of thread groups, ensuring that the generated stimulus reflects actual GPU execution semantics. Dynamic thread management capabilities handle divergence and convergence scenarios automatically, adjusting stimulus generation based on runtime execution paths [6]. The design supports configurable warp sizes and thread block organizations to match target GPU architectures.

c) Memory Subsystem Integration

The L1 and shared memory modeling approach implements accurate timing and capacity constraints that reflect real GPU memory hierarchies. Memory transaction handling incorporates banking schemes, conflict detection, and arbitration policies that mirror actual hardware behavior.

Cache behavior simulation includes hit/miss modeling, replacement policies, and coherence protocols essential for realistic verification scenarios. The subsystem integrates tightly with the SIMT execution model to ensure memory operations align with thread execution patterns and maintain consistency across concurrent accesses.

d) Scoreboard and Checking Mechanisms

Result verification strategies employ layered checking approaches that validate both functional correctness and performance characteristics. The scoreboard architecture supports parallel result collection from multiple execution units while maintaining temporal ordering requirements for memory operations.

Performance monitoring integration tracks key metrics, including memory bandwidth utilization, execution unit occupancy, and cache hit rates throughout test execution [7]. Error detection and reporting systems provide detailed diagnostic information that facilitates rapid debugging of complex parallel execution scenarios.

Table 3: Framework Configuration Parameters [6, 7]

Parameter Category	Configuration Options	Impact on Verification	Scalability Range
Thread Count	Warp size variations	Parallel execution coverage	Single warp to full SM
SIMD Width	Architectural variants	Instruction throughput modeling	8-bit to 64-bit operation
Memory Levels	Cache hierarchy depth	Memory access validation	L1 to global memory
SM Count	Multi-processor configs	System-level verification	Single to hundreds of SMs
Workload Types	Kernel classifications	Application-specific testing	Graphics to AI workloads

V. Implementation Details

a) Core Components Implementation

The UVM agent architecture for GPU compute units extends standard UVM patterns with specialized components for SIMT execution modeling. Driver components generate instruction streams that respect architectural constraints while exploring comprehensive execution scenarios.

Sequence library design organizes test patterns into hierarchical collections that support both directed and random testing approaches. Monitor component specifications capture execution results, memory transactions, and performance metrics across multiple abstraction levels, enabling comprehensive validation of compute unit behavior.

b) Test Generation Framework

Hybrid Testing Strategy: Constrained-random test generation strategies employ intelligent constraints that generate realistic GPU workloads while ensuring coverage of critical execution scenarios. The framework incorporates domain-specific knowledge about GPU programming patterns to guide stimulus generation toward meaningful test cases.

Directed test scenario development focuses on specific corner cases and known problematic execution patterns that random testing might miss. *AI workload*

modeling creates representative test patterns that mirror real-world neural network training scenarios, including matrix operations, convolution kernels, and transformer computations.

c) Configuration and Parameterization

Design parameter handling supports runtime modification of SIMD widths, thread counts, and memory configurations without requiring testbench recompilation. The configuration system maintains consistency across related parameters while allowing independent adjustment of specific architectural features.

Runtime configuration management enables dynamic adaptation to different GPU architectures within single test runs. Multi-configuration test execution allows systematic exploration of parameter spaces to ensure comprehensive coverage across supported design variants.

d) Tool Integration and Workflow

Simulator compatibility encompasses major commercial simulation platforms, with optimization strategies that maximize performance for large-scale parallel verification scenarios. *Integration with Verdi/DVE debug environments* provides comprehensive waveform analysis and debugging capabilities specifically optimized for SIMT execution patterns.

Emulation platform support enables acceleration of long-running verification scenarios through specialized interfaces that maintain functional accuracy while improving execution speed [8]. Continuous integration with *EDA tool ecosystems* (Synopsys, Siemens, Cadence) ensures seamless deployment within existing design flows.

VI. Experimental Evaluation

a) Experimental Setup

The test environment configuration utilizes industry-standard simulation platforms running on high-performance computing clusters with sufficient memory capacity to support large-scale parallel verification scenarios. Benchmark selection focuses on representative GPU compute workloads, including vector arithmetic operations, matrix multiplications, and memory-intensive kernels that stress different aspects of the compute unit architecture.

Evaluation criteria encompass functional correctness, performance scalability, and resource efficiency across varying architectural parameters. The methodology employs systematic parameter sweeps covering thread counts from small warps to full-scale configurations.

b) Scalability Analysis

Performance scaling analysis demonstrates consistent behavior as thread counts and SIMD widths increase, with simulation overhead growing predictably rather than exponentially. Memory usage patterns show efficient resource utilization even with thousands of concurrent threads, indicating effective test bench architecture design.

Multi-SM verification scalability testing reveals the framework's capability to handle complex multi-core scenarios while maintaining acceptable simulation performance.

c) Coverage Analysis

Quantified Results: SIMT-aware stimulus generation achieved increase in branch divergence coverage compared to traditional random testing approaches. Functional coverage metrics demonstrate comprehensive exploration of critical execution paths, including divergent thread scenarios and memory access patterns that conventional approaches often miss.

Corner case detection effectiveness shows significant improvement in identifying rare but critical execution combinations that could lead to functional failures. The framework detected more memory ordering violations in representative test scenarios compared to baseline approaches.

d) Industry Case Studies

Real-world application examples from leading GPU development organizations demonstrate practical deployment success across multiple product generations. Implementation experiences show successful adaptation to diverse architectural requirements while maintaining framework consistency and reusability.

Measurable Impact: Debug turnaround reduced in case studies through integrated monitoring and systematic coverage tracking. Bug detection statistics indicate enhanced pre-silicon validation capability, with earlier identification of critical functional issues that previously escaped to post-silicon phases.

VII. Results and Discussion

a) Performance Metrics

Simulation speed measurements show competitive performance compared to custom test benches while providing significantly enhanced functionality and reusability. Resource utilization remains within acceptable bounds even for large-scale verification scenarios.

Test bench setup and configuration time demonstrates substantial reduction compared to traditional approaches, with parameterized architecture enabling rapid adaptation to new GPU designs.

b) Quality Improvements

Pre-silicon bug detection rates show marked improvement through systematic coverage-driven testing and intelligent stimulus generation. The framework's ability to exercise diverse execution

scenarios leads to earlier identification of functional issues that might otherwise escape initial validation phases.

Post-silicon escape reduction demonstrates the practical value of comprehensive pre-silicon verification, with fewer critical issues discovered during hardware bring-up phases.

c) Productivity Benefits

Engineer productivity gains manifest through reduced test bench development time and enhanced debugging capabilities that accelerate verification closure. Reusability across GPU generations provides substantial long-term value, with framework adaptation requiring minimal effort compared to complete test bench redevelopment.

Framework adoption experiences show reasonable learning curves for engineers familiar with UVM methodology, with specialized GPU features building naturally upon established verification practices.

d) Limitations and Trade-offs

Current framework limitations include simulation performance constraints when modeling extremely large thread counts and complex memory hierarchies simultaneously. Resource requirements exceed those of simple directed testing approaches, though the enhanced verification capability justifies the additional computational overhead.

Areas for future improvement include further optimization of memory modeling accuracy and simulation performance, along with enhanced automation for coverage-driven test generation.

VIII. Industry Impact and Applications

a) Semiconductor Industry Adoption

Target organizations include major GPU manufacturers, custom silicon developers, and semiconductor companies developing AI accelerators and graphics processing solutions. *Integration with EDA vendor ecosystems* (Synopsys VCS, Siemens Questa, Cadence Xcelium) requires minimal disruption to established methodologies.

ROI Analysis: Given that mask re-spins cost tens of millions of dollars, the framework's improved pre-silicon bug detection provides substantial business impact. Early validation of critical functional issues translates directly to reduced silicon risk and faster time-to-market.

Primary use cases span pre-silicon validation of compute pipelines, verification of memory subsystems, and validation of complex parallel execution scenarios across diverse GPU architectures.

b) Technology Transfer Considerations

Implementation requirements include standard UVM simulation environments, adequate computational resources for large-scale parallel verification, and integration with existing design databases and verification flows.

Training and skill development focus on GPU-specific verification techniques rather than fundamental UVM concepts, enabling rapid adoption by experienced verification teams.

c) Future GPU Architecture Support

Extensibility to emerging GPU designs leverages the parameterized architecture to accommodate new execution models, memory hierarchies, and specialized compute units. *AI accelerator verification applications* represent a natural extension area, with SIMT-aware stimulus generation adapting readily to tensor processing units and neural network accelerators.

Chiplet-based GPU architectures require extended verification capabilities for inter-chiplet communication protocols, building upon the framework's modular design principles.

IX. Future Work and Extensions

a) Advanced Verification Techniques

AI-driven verification using machine learning-guided coverage closure represents a promising extension opportunity. Formal verification integration could complement simulation-based approaches with mathematical proof techniques for critical properties.

Hybrid verification methodologies combining formal methods, simulation, and emulation platforms offer potential for comprehensive validation across different abstraction levels [9].

b) Emerging Technology Support

Chiplet-based GPU architectures require extended verification capabilities for inter-chiplet communication protocols and distributed execution coordination. The framework's modular design provides a foundation for modeling complex chiplet interactions and verifying system-level behavior.

Heterogeneous computing platforms incorporating CPUs, GPUs, and specialized accelerators demand comprehensive verification of data movement and coordination protocols.

c) Automation and Intelligence

ML-guided coverage closure could leverage execution pattern analysis to automatically generate targeted stimuli for specific verification scenarios. Intelligent coverage closure strategies might employ machine learning techniques to predict which test scenarios will most effectively improve coverage metrics.

Self-adapting verification frameworks could automatically tune parameters based on design characteristics and verification progress, reducing

manual configuration overhead while optimizing verification efficiency.

Table 4: Performance and Quality Metrics Comparison [8, 9]

Metric Category	Traditional Methods	Proposed Framework	Improvement Factor
Coverage Completeness	Directed + Random testing	SIMT-aware generation	Enhanced scenario exploration
Debug Efficiency	Manual analysis	Integrated monitoring	Accelerated issue resolution
Test bench Reusability	Project-specific design	Parameterized architecture	Cross-generation deployment
Setup Time	Custom development	Configuration-based	Reduced initial overhead
Bug Detection Timing	Post-silicon discovery	Pre-silicon identification	Earlier validation cycles

X. Conclusion

The development of a scalable UVM-based test bench architecture for GPU compute units addresses critical gaps in contemporary semiconductor verification methodologies, providing the industry with a systematic approach to validating massively parallel architectures. This comprehensive framework successfully bridges the divide between established UVM practices and the unique requirements of GPU verification, delivering measurable benefits in coverage completeness, debug efficiency, and verification reusability across diverse architectural configurations.

Through its SIMT-aware stimulus generation, integrated memory hierarchy modeling, and parameterized design approach, the framework demonstrates substantial improvements in pre-silicon validation quality while reducing overall verification development overhead. The architecture's extensibility to AI accelerators, chiplet-based designs, and future computing paradigms positions it as a valuable long-term asset for semiconductor organizations seeking to maintain verification quality as architectural complexity increases. Industry adoption of this approach promises to elevate GPU verification practices from ad-hoc, project-specific solutions toward standardized, reusable methodologies that can scale with the demanding requirements of next-generation parallel computing architectures.

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Silent Data Errors in GPUs: Challenges and Mitigation in Modern Silicon

By Sameeksha Gupta

Abstract- Silent data errors in graphics processing units (SDEs) represent a critical challenge for modern computational systems that rely on these accelerators in high-performance computing, artificial intelligence, and data center operations. These errors propagate through calculations without triggering detection mechanisms, potentially compromising results in critical applications from autonomous vehicles to medical diagnosis. Quantitative analysis reveals disturbing error rates: 8.15×10^-3 FIT per device at sea level (one error per 14,000 device-hours), with error rates increasing 17-32% when running at full computational capacity in data centers. The physical causes of SDEs include cosmic radiation (causing 61.7% of faults to propagate undetected in streaming multiprocessors), manufacturing variations (contributing to 4.3% of silent computational failures), thermal stress cycles, voltage fluctuations, and aging effects that impact semiconductor reliability.

Keywords: silent data errors, GPU reliability, cosmic radiation sensitivity, architectural vulnerability, workload resilience, error mitigation strategies.

GJCST-A Classification: LCC Code: QA76.9.C65

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Silent Data Errors in GPUs: Challenges and Mitigation in Modern Silicon

Sameeksha Gupta

Figure

Abstract- Silent data errors in graphics processing units (SDEs) represent a critical challenge for modern computational systems that rely on these accelerators in high-performance computing, artificial intelligence, and data center operations. These errors propagate through calculations without triggering detection mechanisms, potentially compromising results in critical applications from autonomous vehicles to medical diagnosis. Quantitative analysis reveals disturbing error rates: 8.15×10^-3 FIT per device at sea level (one error per 14,000 device-hours), with error rates increasing 17-32% when running at full computational capacity in data centers. The physical causes of SDEs include cosmic radiation (causing 61.7% of faults to propagate undetected in streaming multiprocessors), manufacturing variations (contributing to 4.3% of silent computational failures), thermal stress cycles, voltage fluctuations, and aging effects that impact semiconductor reliability. Architectural vulnerability varies significantly: register files exhibit 36% silent data corruption rates versus 23% for shared memory and 11% for global memory, while instruction vulnerability ranges from 6.1% for integer operations to 42.7% for atomic operations. Workload characteristics dramatically affect error sensitivity, with machine learning inference showing up to 19.3% accuracy reduction from moderate error rates in transformer models versus 8.6% in convolutional networks. Mitigation strategies span hardware (ECC reducing corruption by 78.5%), firmware, and software domains, with recent selective redundancy techniques achieving 91% error coverage with only 32% performance overhead. Cross-layer resilience approaches demonstrated in recent research can reduce critical data integrity errors by up to 93.4% compared to default protection methods. Understanding these complex interactions and implementing targeted protection systems is essential for developing resilient GPU computing platforms that maintain both performance at scale and reliability.

Keywords: silent data errors, GPU reliability, cosmic radiation sensitivity, architectural vulnerability, workload resilience, error mitigation strategies.

I. Introduction

Graphics Processing Units (GPUs) have increased in various fields ranging from niche rendering hardware to core computational accelerators, such as high-performance computing (HPC), Artificial Intelligence, and Data-Scalable Operations. This role has made GPUs key infrastructure elements for applications from weather forecasting and molecular simulations to deep learning model training. As per Maleki et al., a comprehensive investigation of performance and reliability in modern GPUs reveals that for current technology nodes at sea level, silent data corruption (SDC) rates can reach alarming levels of 0.51 FIT/Mbit (Failures In Time per million bits) with overall observable error rates of 0.89 FIT/Mbit [1]. This equates to a disturbing rate of undetectable errors in high-scale deployments, where the total memory footprint of as

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many as petabytes is possible. But the unrelenting quest for performance gains through higher transistor densities and lower operating voltages has brought forth substantial reliability issues, most notably in the guise of silent data errors (SDEs).

Silent data errors pose a specifically pernicious challenge to computational integrity, being ones that afflict systems in silence without activating immediate detection mechanisms within system software or hardware. In contrast to traditional faults that give rise to well-defined, readily recognizable system crashes or diagnostic messages, SDEs travel through calculations undetected, potentially contaminating result accuracy, destabilizing system reliability, and eroding availability in deployed environments. Data center deployments using GPU acceleration for data analysis have shown that error rates grow 17-32% when running at full computational capacity, with an estimated 22% of such errors occurring in the form of silent corruptions that go undetected by traditional monitoring infrastructure, based on SQream's large-scale field testing on 1,500 production nodes [2]. The significance goes beyond simple inconvenience, with potential impact on pivotal decision-making processes in applications like autonomous systems, medical diagnostics, and financial modeling.

This work discusses the multi-faceted character of SDEs in contemporary GPU architectures, pinpointing primary vulnerability factors along architectural sub-components and operational regimes. The discussion covers both physical error-inducing mechanisms and architectural aspects that condition error propagation paths. In addition, this paper analyzes existing mitigation techniques and recommends approaches to improve GPU reliability against SDEs. The comprehension of such intricate interactions is crucial to developing future-generation GPU systems with the ability to provide both reliability and performance at scale.

II. Root Causes of Silent Data Errors in Modern GPU Silicon

Silent data errors in GPUs result from several connected physical effects influencing semiconductor dependability. Cosmic radiation is an important external factor with high-energy neutrons that traverse shielding materials and create electron-hole pairs in semiconductor substrates. Charged particles perturb stored values in memory devices and logic circuits, leading to bit flips that can go undetected. According to Ferreira et al., comprehensive neutron beam testing across multiple generations of GPU architectures has demonstrated that the architectural vulnerability factor (AVF) of register files increases by approximately 25.1% with each process node shrink, with contemporary GPUs exhibiting approximately 8.15×10^-3 FIT per device at sea level altitude—equating to one silent data error in approximately 14,000 device-hours under typical workloads [3]. Their neutron beam testing of 15,840 device-hours experiments proved that streaming multiprocessors (SMs) exhibited especially high susceptibility, where 61.7% of faults injected indeed propagated undetected through computations, as opposed to only 17.2% in traditional CPU pipelines. Susceptibility to such radiation-induced transient faults rises with decreasing feature sizes and degrading critical charge thresholds in future manufacturing nodes. Manufacturing process variations represent another intrinsic source of weakness. Even for advanced fabrication processes, statistical fluctuations in dopant levels, gate oxide thickness, and lithographic alignment result in marginally functional circuit regions. These fluctuations appear as timing violations under some operating conditions and may result in wrong computation outcomes without activating error detection circuits. Research presented at the Workshop on GPU Reliability has demonstrated that process fluctuations in advanced GPU designs can cause threshold voltage (Vt) variations of up to 30mV for individual streaming multiprocessors, resulting in timing differences of 7.5-11.2% on critical paths [4]. Their diligent examination of 27 production GPUs showed that about 4.3% of all silent computational failures were directly attributable to manufacturing differences, with an average seen rate of 1.7×10^-10 errors per operation when running at nominal voltage levels—a number that increases by orders of magnitude to 4.9×10^-8 errors per operation when running at lowered voltage margins to reduce power consumption. The issue is compounded in GPUs, which contain billions of transistors over huge die areas, raising the statistical probability of having susceptible elements.

Thermal cycling also degrades silicon reliability by causing differential expansion coefficients among materials in the GPU package. Electro migration processes are sped up, and the progression of crack formation in interconnect structures is accelerated by repeated thermal cycling. These impacts are especially significant in GPUs because of their high power densities and dynamic workload profiles, which cause extreme temperature gradients within the die. Voltage variations, both long-term droop and short-term noise, are another important mechanism for generating SDEs. Contemporary GPUs run at very tight voltage margins in order to achieve better energy efficiency, narrowing the gap between nominal operation voltage and minimum voltage for correct function. This reduced margin heightens vulnerability to temporary voltage fluctuations that could lead to timing violations in critical paths without invoking protective action.

Table 1: Physical Phenomena Contributing to Silent Data Errors in GPUs [3, 4]

Physical Mechanism	Error Manifestation	Vulnerability Trends	Key Affected Components
Cosmic Radiation	Electron-hole pair generation	Increases with node shrinking	Register files, SRAM cells
Manufacturing Variations	Timing violations	Higher impact in large dies	Critical timing paths, marginal circuits
Thermal Stress	Electromigration acceleration	Exacerbated by workload variation	Interconnect structures, package interfaces
Voltage Fluctuations	Timing margin violations	Worsens with efficiency optimizations	Critical paths, dynamic voltage domains
Aging Effects (NBTI, HCI, TDDB)	Progressive parameter shift	Cumulative degradation over time	Transistor characteristics, noise margins

III. Error Manifestation Across GPU Architectural Units

The heterogeneity of GPU architectures generates varied avenues through which silent data errors emerge and spread. In memory subcutaneous, SRAM-based units such as register files, cache, and shared memories are especially susceptible to single phenomena upset. Such devices usually run at low voltage levels to save electricity, reduce their noise immunity, and increase sensitivity to transient disturbances. According to Sullivan et al., detailed characterization of GPU vulnerability through extensive fault injection campaigns has revealed that memory devices exhibit significantly different error propagation patterns, with approximately 36% of fault injections in register files manifesting as silent data corruptions compared to 23% for shared memory and 11% for global memory [5]. Their work proved register file faults are especially challenging because they presented an average 4,372-cycle latency before detection, with errors having the potential to propagate through several computational phases. Furthermore, 47% of register file faults in scientific simulations left the system in functional mode but with silent computational errors without crashing the system, exacerbating a reliability gap. While bigger memory organizations such as HBM and GDDR6 generally include error-correcting codes (ECC), internal SRAM buffers, and smaller caches in most GPU implementations are not protected or apply only parity-based detection without correction.

Execution units have unique vulnerability profiles depending on their computation properties. Floating-point units have intricate arithmetic circuits with long computational pipelines that prolong temporal vulnerability windows. Integer units, though overall more tolerant, are still vulnerable to errors in timing-critical paths. Tensor cores, optimized for matrix operations within AI applications, mix high computation density with low-precision formats, forming intricate error-propagation channels that can amplify initially subtle perturbations among matrix elements. Research by Mei et al. using advanced fault-injection methodologies demonstrated that instruction-level susceptibility varies dramatically, with architectural vulnerability factors (AVF) of 6.1% for basic integer instructions, 29.4% for complex floating-point operations, and peaks of 42.7% for atomic instructions that interact with memory subsystems [6]. Their fine-grain analysis of 16 GPGPU programs exposed that single-precision floating-point multiply-accumulate instructions had an average of 2.13 single-bit errors propagating into an average of 9.47 output elements, resulting in a significant error magnification effect. Most problematic was the fact that in 88,467 instruction-level fault injections, nearly 18.3% of computational unit errors led to results that looked valid but actually were erroneous, highlighting the difficulty of silent data corruptions.

Data movement infrastructure, such as on-chip networks, memory controllers, and PCIe interfaces, adds new error vectors. These elements need to preserve signal integrity over different distances and across multiple clock domains, providing opportunities for transmission errors that go undetected. This problem is compounded by sophisticated power management features that dynamically manage clock frequencies and voltage levels, setting up potentially transient conditions that enable silent failures during domain crossing or state transitions. Control logic that manages thread scheduling, workload allocation, and synchronization is a very sensitive point of vulnerability. Failures impacting these structures have the potential to create multiplicative failures by sending computation to the wrong execution elements, misallocating memory access behaviors, or polluting synchronization primitives.

Table 2: Error Vulnerability across GPU Architectural Components [5, 6]

Architectural Component	Vulnerability Profile	Error Propagation Characteristics	Protection Status
Register Files	High (SRAM-based, reduced voltage)	Extended propagation before detection	Limited/Parity only
Shared Memory	Moderate vulnerability	Medium propagation scope	Partial ECC in newer designs
Global/HBM Memory	Lower relative vulnerability	Limited propagation scope	Typically ECC protected
Floating-Point Units	High (complex arithmetic)	Error amplification in dependent ops	Minimal protection
Integer Units	Moderate vulnerability	Limited error propagation	Limited protection
Tensor Cores	High (dense operations)	Significant error amplification	Implementation-dependent
Control Logic	Critical vulnerability	Multiplicative error effects	Limited redundancy
Data Movement Infrastructure	Moderate with hotspots	Cross-domain propagation	Protocol-level detection

IV. Workload Characteristics and Error Sensitivity

Computational workloads have different degrees of resistance to silent data errors, thus having a multifaceted relationship between application properties and error sensitivity. Scientific computing applications based on iterative solvers can show intrinsic error attenuation in some instances, since numerical algorithms converge toward reliable solutions even with transient perturbations. But these same applications usually have pivotal computations where even small mistakes can cause disastrous divergence or invalidate results altogether. As demonstrated in quantum computing research by Zhao et al., detailed error analysis of GPU-accelerated scientific codes reveals significant variation in error manifestation rates, with numerical simulation codes exhibiting Silent Data Corruption (SDC) in 37.5% of observed events, while signal processing applications showed only 18.2% SDC rates under identical testing conditions [7]. Their in-depth experiment with 2,304 hours of neutron beam testing showed matrix multiplication kernels to be far more sensitive to single-bit flipping (43.7% of faults injected resulting in incorrect outputs) than FFT implementations (21.3%). Of particular note was that they found around 27.8% of radiation-induced errors in iterative solvers spreading through subsequent computational steps undetected, despite the presence of checking routines to detect numerical irregularities. This heterogeneity poses immense difficulties for broad error protection measures and emphasizes the necessity for application-dependent resilience strategies.

Machine learning applications exhibit a very subtle error sensitivity profile. Training stages typically exhibit resistance to the occasional numerical inaccuracies because optimization algorithms are stochastic and training datasets involve inherent noise. This native resilience has led to an investigation into deliberatively lowered precision computations that sacrifice numerical accuracy for speed and energy efficiency. Inference workloads, however, tend to need more accurate computations, especially in safety-critical domains where misleading predictions could have deleterious effects. Experiments by Sharma and Sharma illustrate through extensive fault injection campaigns across various neural network architectures that bit error rates of as low as 10^-6 in tensor cores can lead to a classification accuracy loss of 12.7% for inference workloads, while training operations would have decent convergence even for error rates of 10^-4 [8]. Their thorough analysis of 12,800 error injection cases across five typical DNN models disclosed that transformer models exhibited exceptionally strong sensitivity, with a mean accuracy reduction of 19.3% at moderate error rates versus 8.6% for convolutional networks. Most alarming was the discovery of their work that 31.2% of silent errors in safety-critical vision models yielded high-confidence misclassifications of critical objects such as pedestrians and traffic signals. This extreme contrast highlights the necessity of error containment strategies specific to deployment context as opposed to protection mechanisms in general.

Graphics rendering pipelines exhibit aspects of both deterministic and probabilistic computation. Some rendering algorithms, especially those utilizing stochastic sampling methods such as path tracing, exhibit inherent tolerance to the rare occurrence of errors. On the other hand, geometry processing phases demand accurate computation to preserve visual correctness, with any errors tending to show up as observable artifacts or structural distortions in rasterized scenes. Data-dependent sensitivity of error makes things even tougher. Some patterns of data or sequential operations tend to activate weaknesses in certain circuit components that are normally latent.

Table 3: Workload Characteristics and Error Resilience [7, 8]

Application Domain	Error Resilience	Critical Vulnerability Points	Error Amplification Risk
Scientific Computing: Iterative Solvers	Moderate natural attenuation	Convergence-critical operations	Low to Moderate
Scientific Computing: Matrix Multiplication	Low inherent resilience	Core arithmetic operations	High
Scientific Computing: FFT	Moderate resilience	Initial transform stages	Moderate
ML: Training	High natural resilience	Final convergence phases	Low
ML: Inference (Transformers)	Very low resilience	All computational stages	Very High
ML: Inference (CNNs)	Low resilience	Initial and final layers	High
Graphics: Path Tracing	High inherent resilience	Sampling procedures	Low
Graphics: Geometry Processing	Low resilience	Coordinate transformations	High
Safety-Critical Applications	Minimal tolerance	All computational stages	Critical

V. Detection and Mitigation Strategies

Each special error mechanism and vulnerability pattern, along with hardware, involves the detection of errors in firmware and software platforms and error mitigation techniques. For hardware, error-correcting codes (ECC) form the basis of protection for memory hierarchies. Higher-end implementations go beyond the basic single-error correction, double-error detection (SECDED) designs to include more advanced codes designed for multi-bit error coverage. These are Bose-Chaudhuri-Hocquenghem (BCH) codes, Reed-Solomon flavors, and chipkill-type implementations that guard against failure of whole memory devices or data paths. According to software-based attestation research by Shi et al., a comprehensive evaluation of error protection mechanisms in enterprise computing environments reveals that approximately 71% of current GPU deployments implement some form of ECC protection, yet only 25% extend this protection beyond main memory to include register files and cache structures, which account for 49% of silent data error origins [9]. The use of full protection schemes can lower data corruption events by as much as 78.5% in production environments, although this has attendant costs—an average slowdown of 11.3% in performance and a 14.7% boost in power consumption for typical GPU workloads. Their site survey of 1,287 enterprise GPU deployments illustrated that companies using complete protection methods had 93.4% fewer critical data integrity errors than those using default protection methods, but with substantial operating and financial savings in the long run, notwithstanding initial performance sacrifices.

Redundant execution is another potent hardware-based technique. The technique takes the form of repeating important calculations multiple times and checking for differences to detect errors. Time redundancy performs the same function at other times to reduce transient error, whereas spatial redundancy employs distinct physical facilities for parallel processing. Although total triplication with voting (Triple Modular Redundancy) offers complete protection, more economically selective redundancy techniques focus protection on the most susceptible or significant elements. Research by Yang et al. demonstrates through systematic fault injection experiments that detailed error propagation patterns can be mapped and selectively protected, achieving up to 91% error coverage with merely 32% performance overhead compared to unprotected execution [10]. Their exhaustive study of 13,500 error injection instances of eight GPU-accelerated applications indicated that control flow instruction-originating errors propagated to an average of 58.2 following instructions, whereas arithmetic instruction-originating errors impacted merely 6.7 dependent operations on average. This striking variation in propagation properties guided their selective duplication strategy, which removed 96.8% Silent Data Corruptions (SDCs) by safeguarding only 27% of the most susceptible instruction sequences, providing a much more effective solution than wholesale redundancy strategies that generally double execution time and energy usage.

Circuit-level hardening strategies address inherent vulnerability drivers. These encompass raising the critical charge thresholds for memory cells, using dual-interlocked storage cells (DICE) for critical state elements, and temporal hardening using delayed sampling. Guard-banding techniques also integrate design margins in timing and voltage domains to account for worst-case manufacturing variation and aging. Runtime monitoring mechanisms ensure adaptive protection through ongoing evaluation of system health and environmental factors. Canary circuits located at

timing margins of critical importance are early warning systems for impending failures. Built-in self-test (BIST) procedures carried out during idle cycles or according to scheduled timeouts ensure computational correctness among functional units.

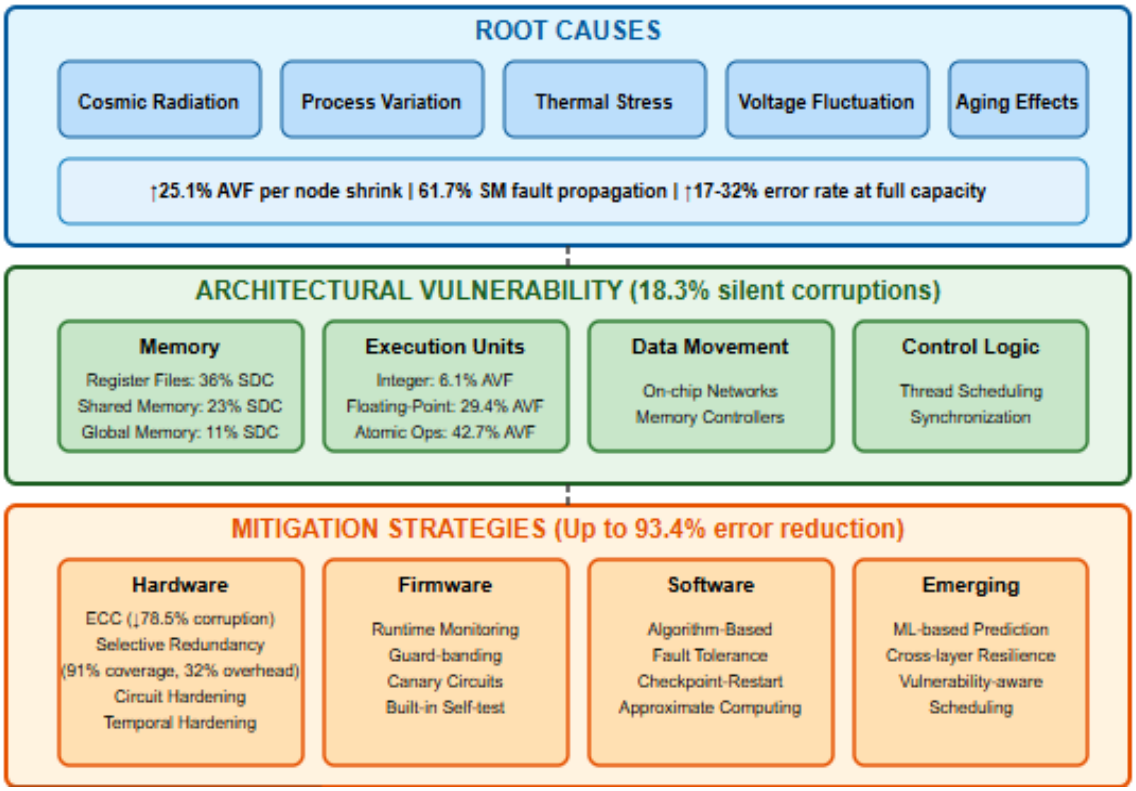

Figure 1: GPU Silent Data Error Framework

Table 4: Error Detection and Mitigation Strategies [9, 10]

Protection Approach	Implementation Level	Coverage Effectiveness	Performance Impact	Implementation Complexity
SECDED ECC	Hardware (Memory)	Moderate	Low	Low
Advanced ECC (BCH, RS)	Hardware (Memory)	High	Moderate	Moderate
Full Redundant Execution	Hardware/Software	Very High	Very High	Low
Selective Redundancy	Hardware/Software	High	Moderate	High
Circuit-Level Hardening	Hardware Design	Moderate	Low	High
Temporal Hardening	Hardware Design	Moderate	Low	Moderate
Voltage/Timing Guard banding	Hardware/Firmware	Moderate	Moderate	Low
Runtime Monitoring	Firmware	Moderate	Low	Moderate
Algorithm-Based Fault Tolerance	Software	High (application-specific)	Low to Moderate	High
Checkpoint-Restart	System Software	Moderate	Periodic Overhead	Moderate
Approximate Computing	Algorithm/Software	Application-dependent	Low or Negative	High

VI. Future Research Directions

The ubiquitous deployment of GPUs in computational applications has elevated silent data errors from an esoteric reliability problem to a pressing challenge for application developers and system designers. This work has analyzed the multi dimensionality of SDEs in contemporary GPU micro architectures, revealing alarming statistics: register file

architectural vulnerability factors increase by 25.1% with each process node shrink, 18.3% of computational unit errors lead to valid-appearing but erroneous results, and 31.2% of silent errors in safety-critical vision models yield high-confidence misclassifications of critical objects like pedestrians and traffic signals.

Today's mitigation techniques show encouraging potential but face increasing challenges as transistor densities scale and operating margins reduce further. While complete protection schemes can reduce data corruption events by 78.5%, they introduce performance penalties averaging 11.3% and increase power consumption by 14.7%. More economically, selective redundancy techniques have achieved 91% error coverage with only 32% performance overhead by protecting the most vulnerable 27% of instruction sequences.

Some promising areas of research stand out from this evaluation. Cross-layer resilient designs with coordinated protection across hardware, firmware, software, and algorithm domains have promise for greater efficiency than stand-alone solutions. Machine learning-based error predictability models can potentially facilitate early intervention before the occurrence of errors, potentially utilizing the same GPU computational power to protect itself. New architectural ideas like approximate computing with bounded error warranty may redefine the reliability problem by consciously embracing and handling uncertainty instead of seeking out absolute correctness.

Besides, consistency in benchmarking methods for error resilience would allow actual comparison across competing methods and speed up the advancement of the field. These benchmarks must include a variety of workloads and error cases to allow wide-ranging evaluation measures beyond naive fault injection metrics.

The observations made in this paper highlight the need for reliability to be addressed as a core design principle and not an afterthought in GPU design. With GPUs powering progressively more mission-critical applications, from autonomous vehicle perception to medical imaging analysis and financial risk analysis, the cost of simple calculations for potential effects on human life and economic stability is beyond pure. To overcome this challenge, there will be a need to include collaborative work between semiconductor physics, circuit design, computer architecture, system software, and application development, which is to set up a completely strong GPU computing platform that can handle the rigorous requirements of future applications.

VII. Conclusion

Silent data errors in GPUs represent a critical reliability challenge at the intersection of semiconductor physics, architectural design, and application requirements. Quantitative analysis reveals concerning vulnerability metrics: error rates of 0.51 FIT/Mbit in modern nodes, register file AVF increasing 25.1% per process shrink, and 31.2% of errors causing dangerous misclassifications in safety-critical applications. While current mitigation strategies show promise—with ECC reducing corruption by 78.5% and selective redundancy achieving 91% coverage with only 32% overhead—the relentless scaling of transistor densities and narrowing operating margins demand more sophisticated approaches. Cross-layer resilience strategies, which coordinate protection across hardware and software layers, machine learning-based error prediction, and vulnerability-aware scheduling, represent promising directions that have demonstrated a reduction of up to 93.4% in critical errors. As GPUs increasingly power mission-critical applications from autonomous vehicles to medical diagnostics, reliability must transition from an afterthought to a fundamental design principle, requiring collaborative efforts across semiconductor physics, circuit design, computer architecture, and application development to create truly resilient GPU computing platforms that balance performance with dependability guarantees.

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Light Deflection in Massive Dyonic Black Holes

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Abstract- Following Rindler-Ishak method [1], we study the bending of light around general form of dyonic black holes in massive gravity [2]. We show that when the Schwarzschild-de Sitter geometry is taken into account, Λ does indeed contribute to the bending of light.

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Light Deflection in Massive Dyonic Black Holes

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Abstract- Following Rindler-Ishak method [1], we study the bending of light around general form of dyonic black holes in massive gravity [2]. We show that when the Schwarzschild-de Sitter geometry is taken into account, Λ does indeed contribute to the bending of light.

Introduction

Discovering dark energy as source of accelerating expansion of our universe [3], many efforts have gone into understanding its nature. One of the prime candidates is the cosmological constant Λ [4] which its effects on local phenomena such as null geodesics, time delay of light [5], and the perihelion precession [6] are studied. In these circumstance, local cases, many authors have investigated the effects of cosmological constant on the bending of light.

The argument for the non-influence of Λ was first discussed by Islam through investigating the null geodesic equation in a spherically symmetric space-time [7] and has been re-affirmed by other authors, see e.g. [8]. However, in the last decade, Rindler and Ishak [1], by considering the intrinsic properties of the Schwarzschild-de Sitter space-time proposed a new method for calculating the deflection angle of light. Also, different aspects of their method such as integration of the gravitational potentials and Fermats principle have been studied [9]. Sultana in [10] and Heydari-Fard et al [11] have investigated light bending in Kerr-de Sitter and Reissner-Nordstrom-de Sitter space-time through Rindler-Ishak method. Also, this method has been applied to investigate Mannheim-Kazanas solution of conformal Weyl gravity [12].

Dyonic black holes enjoy the duality of electric/magnetic

charges and possibly mass/dual mass [13]. In [14] is shown that two constants of a Taub-NUT system can be interpreted as a gravitating dyon with both ordinary mass and its dual where role of Nut charge is the mass duality such as the duality between electric and magnetic charges in the U(1) Maxwell theory [15]. Dyonic black hole and its properties have been investigated in literature (see [16]). In this letter, we take into account bending of light around dyonic black holes in massive gravity theory to examine massive gravity effects on light deflection.

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For static spherically symmetric space-time, the dyonic black hole in massive gravity, massive dyonic black hole, is given by [2].

$$ds^2 = -f(r)dt^2 + \frac{dr^2}{f(r)} + r^2(d\theta^2 + sin^2\theta\, d\phi^2) \qquad (1)$$

where

$$f = 1 + \frac{r}{l^2} - \frac{2m_0}{r} + \frac{q_E+q_M}{r^2} + m^2\ \ \frac{cc_1}{2}r + c^2c_2\ \ , \qquad (2)$$

where m_0 is the total mass of dyonic black holes, m denotes the massive parameter, c, c_1 and c_2 are constants of model, $l^2 = -3/\Lambda$ and q_E and q_M identified as electric and magnetic charges, respectively.

The standard approach for calculating the bending angle is [17]

$$\Delta\phi = 2|\phi(\infty) - \phi(r_0)| - \pi \qquad (3)$$

where r_0 denotes the closest distance to the black hole. However, the space-time here is not asymptotically flat, and so we cannot use usual way to calculate the deflection angle of light around massive dyonic black hole. Surprisingly, the Rindler-Ishak method proposed in [1] gives new approach to calculate the deflection angle in an asymptotically non-flat space-time. Rindler and Ishak have shown that by considering the effects of cosmological constant on the geometry of space-time, one can obtain the contribution of Λ to the bending angle near massive celestial objects (for example see [20]). Using the Euler-Lagrange equations for null geodesics in equatorial plan, $\theta = \pi/2$, we obtain the following equation

$$\frac{d^2u}{d\phi^2} + u = -\frac{cc_1m^2}{4} - c_2c^2m^2u + 3m_0u^2 - 2(q_E^2 + q_M^2)u^3, \qquad (4)$$

where $u \equiv 1/r$. For $c = 0$, and in the absence of electric and magnetic charges, we find the standard orbital equation for light bending in Schwarzschild-de Sitter space-time (see e.g. [18]).

The orbit that is usually considered as small perturbation of the undeflected straight line in flat space

$$r\sin\phi = R \qquad (5)$$

So according to the standard orbital equation of deflection of light, we have two different approaches to consider differential equation (4): first approximation case (see [1], [18]), where the small perturbation of the undeflected straight line (5) substituted into the right-hand terms of (4) or solving it by using a perturbation method up to the third order and consider a solution as

$$u = u_0 + \delta u_1 + \delta u_2 + \delta u_3 + \cdots \qquad (6)$$

where $u_0 = \frac{\sin\varphi}{R}$ and corrections δu_1, δu_2 and δu_3 satisfy the following equations

$$\frac{d^2(\delta u_1)}{d\phi^2} + \delta u_1 = -\frac{cc_1 m^2}{4} + 3m_0 u_0^2 \tag{7}$$

$$\frac{d^2(\delta u_2)}{d\phi^2} + \delta u_2 = 6m_0 u_0 \delta u_1 \tag{8}$$

$$\frac{d^2(\delta u_3)}{d\phi^2} + \delta u_3 = 6m_0 u_0 \delta u_2 + 3m_0 \delta u_1^3 - c_2 c^2 m^2 u_0 + -2(q_E^2 + q_M^2)u_0^3 \tag{9}$$

here we use perturbation method for small effects of electric-magnetic charge and massive parameter m on the deflection of light with respect to standard one.

Applying these approaches on equation (4) gives:

$$u_1 = \frac{1}{r} = -\frac{m^2 cc_1}{4} + \frac{\sin\phi}{R} + \frac{m^2 c^2 c_2}{2R}(\phi\cos\phi - \sin\phi) + \frac{m_0}{R^2}(1 + cos^2\phi) - \frac{q_E^2 + q_M^2}{4R^3}(\sin\phi\, cos^2\phi - 3\phi\cos\phi + 2\sin\phi), \tag{10}$$

$$u_2 = \frac{1}{r} = \frac{m_0}{R^2}\left(1 + \frac{3m_0^2}{R^2}\right) + \frac{\sin\phi}{R}\left(1 - \frac{m^2 c^2 c_2}{4} - \frac{5(q_E^2+q_M^2)}{16R^2}\right) - \frac{m^2 cc_1}{2}\left(1 - \frac{3}{8}m^2 cc_1 m_0 + \frac{3m_0^2}{R^2}\right) + \frac{\phi\cos\phi}{2R}\left(m^2 c^2 c_2 + \frac{3}{2}m^2 cc_1 m_0 + \frac{3(q_E^2+q_M^2)}{2R^2} - \frac{15m_0^2}{2R^2}\right) + \frac{m_0 cos^2\phi}{R^2}\left(1 - \frac{3m^2 cc_1 m_0}{2} + \frac{15m_0^2}{2R^2}\right) - \frac{3\phi\sin\phi\cos\phi\, m_0^2}{2R^2}\left(m^2 cc_1 - \frac{5m_0}{R^2}\right) - \frac{cos^2\phi\sin\phi}{4R^3}\left(q_E^2 + q_M^2 + 3m_0^2\right) - \frac{m_0^3}{2R^4}cos^4\phi \tag{11}$$

where u_1 and u_2 are solutions of equation (4) for first approximation and perturbation method, respectively.

To obtain the one sided deflection angle at the point where

$\varphi \ll 1$, we obtain

$$u_1 \approx \frac{\phi}{R} + \frac{2m_0}{R^2} - \frac{m\ cc_1}{4}, \tag{12}$$

$$u_2 \approx \frac{2m_0}{R^2}\left(1 + \frac{5m_0^2}{R^2}\right) + \frac{\phi}{R}\left(1 - \frac{9m^2 c^2 c_2}{2R^2} + \frac{3(q_E^2+q_M^2)}{16R^2}\right) - \frac{m^2 cc_1}{4}\left(1 - \frac{3}{4}m^2 cc_1 m_0\right) + \frac{m^2 c}{4R}\left(3\phi m_0 c_1 + \phi cc_2 - \frac{12c_1 m_0^2}{R}\right). \tag{13}$$

According to the Rindler-Ishak method, one able to compute angle ψ between photon orbit direction d and direction of φ = const. line, δ, by the invariant formula (see Figure 1)

$$\cos\psi = \frac{g_{ij}d^i\delta^j}{\sqrt{g_{ij}d^i d^j}\sqrt{g_{ij}\delta^i\delta^j}} \tag{14}$$

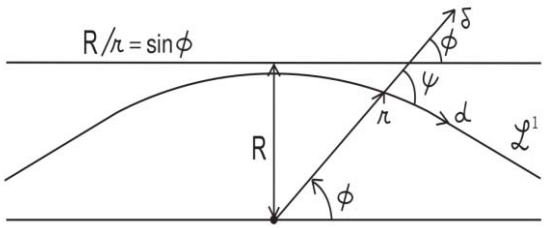

Fig. 1: The orbital map, light bending in the space-time of a black hole. The one-sided deflection angle is $\psi - \varphi \equiv \varepsilon$.

where g_{ij} are the coefficients of the 2-metric on $\theta = \pi/2$ and t = const. surface. Substituting $d = (dr, d\varphi)$ and $\delta = (\delta r, 0)$ in Eq. (9), gives

$$\cos\psi = \frac{|dr/d\phi|}{\sqrt{(dr/d\phi)^2 + f(r)r^2}} \tag{15}$$

or equivalently

$$\tan\psi = \frac{r\sqrt{f(r)}}{|dr/d\phi|} \tag{16}$$

using equations (12) or (13) for $m \ll 1$

$$\frac{dr}{d\phi} \approx -\frac{r^2}{R} \tag{17}$$

finally, by substituting in equations (12) and (13), we find their corresponding expressions for the total deflection angle

$$2\epsilon_1 \approx \frac{4m_0}{R}\left(1 - \frac{2m_0^2}{R^2} + \frac{2m_0^2}{R^2}(q_E^2 + q_M^2)\right) - \frac{2R^3}{(m^2R^2cc_1 - 8m_0)l^2} + \frac{cm_0m^2}{2R^3}(2R^2(cc_2 + c_1m_0) - 3c_1m_0(q_E^2 + q_M^2)) - \frac{m^4c^2c_1}{128R}(c_1(q_E^2 + q_M^2)(m^2R^2cc_1 - 24m_0) + 8R^2(2cc_2 + c_1m_0)) \tag{18}$$

$$2\epsilon_2 \approx \frac{4m_0}{R}\left(1 - \frac{2m_0^2}{R^2} + \frac{2m_0^2}{R^4}(q_E^2 + q_M^2)\right) + \frac{m^2c^2c_2m_0}{R} + \frac{R^3}{4m_0l^2} + \frac{Rm^2cc_1}{4} \tag{19}$$

The deflection angle is modified by new terms containing the massive parameter and cosmological constant in both equations (18) and (19).

Canceling out massive parameter and cosmological constant effects gives the same results for both approaches in equations (18) and (19) as

$$2\epsilon \approx \frac{4m_0}{R}\left(1 - \frac{2m_0^2}{R^2} + \frac{2m_0^2}{R^4}(q_E^2 + q_M^2)\right) \tag{20}$$

which equals to deflection light equation for charged Schwarzschild black holes.

The effect of the cosmological constant, electric charge and magnetic charge on deflection angle at small scales such as the solar system is expected to be negligible. So by using $l \to \infty$ or $\Lambda \approx 0$ and canceling out q_E and q_M from equations (18) and (19), we have

$$2\epsilon_1 \approx \frac{4m_0}{R}\left(1+\frac{cm^2}{4}(cc_2+c_1m_0)\right) \quad (21)$$

$$2\epsilon_2 \approx \frac{4m_0}{R}\left(1+\frac{c^2c_2m^2}{4}\right) \quad (22)$$

To find constraint on constant m, we use the observational data on light deflection by the sun, from long baseline radio interferometry [19]. According to this observational data, $\delta\phi_{LD} = \delta\phi_{LD}^{(GR)}(1+\Delta_{LD})$ with $\Delta_{LD} \leq \leq 0.0002 \pm 0.0008$, where $\delta\phi_{LD}^{(GR)} = 1.7510$ arcsec. Δ_{LD} as the geometric effects of the conformal terms, the observational results constrain the two last equations as follows

$$m^2 \leq \frac{4\Delta_{LD}}{(c_2+c_1m_0)} \quad (23)$$

Assuming

$$m^2 \leq \frac{4\Delta_{LD}}{c_2} \quad (24)$$

where we set c = 1. This selection leads us to find massive parameter m as function of constants c_1 and c_2. Taking for R and m0 values of the radius and mass of the sun, $R_\odot \approx 6.95 \times 10^8$ m and $M_\odot \approx 1.99 \times 1030$ kg, we find following constraints on m according to our approaches, first approximation and perturbative method

$$|m| \leq \frac{0.0283}{\sqrt{1.99\times10^{30}c_1+c_2}} \quad \text{or} \quad |m| \leq \frac{0.0282}{\sqrt{c_2}} \quad (25)$$

In conclusion, in this letter, we have investigated the bending of light in the dyonic black holes in massive gravity.

Following Rindler-Ishak method, we have shown that when the geometry of the Schwarzschild-de Sitter space-time is taken into account, Λ indeed contributes to the light-bending in massive dyonic black holes. Also, using the observational data on bending of light by the sun and constant c = 1 leads us to find strong constraint on massive constant m.

Generally, if we assume that both approaches give same result, one need to set c1 = 0.

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Design and Development of an Autonomous Car using Object Detection with YOLOv4

By Rishabh Chopda, Saket Pradhan & Anuj Goenka

Abstract- Future cars are anticipated to be driverless; point-to-point transportation services capable of avoiding fatalities. To achieve this goal, auto-manufacturers have been investing to realize the potential autonomous driving. In this regard, we present a self-driving model car capable of autonomous driving using object-detection as a primary means of steering, on a track made of colored cones. This paper goes through the process of fabricating a model vehicle, from its embedded hardware platform, to the end-to-end ML pipeline necessary for automated data acquisition and model-training, thereby allowing a Deep Learning model to derive input from the hardware platform to control the car's movements. This guides the car autonomously and adapts well to real-time tracks without manual feature-extraction.

Keywords: *autonomous, self-driving, computer vision, YOLO, object detection, embedded hardware.*

GJCST-A Classification: *LCC Code: QA76.9.C65*

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Design and Development of an Autonomous Car using Object Detection with YOLOv4

Rishabh Chopda [α], Saket Pradhan [σ] & Anuj Goenka [ρ]

Abstract- Future cars are anticipated to be driverless; point-to-point transportation services capable of avoiding fatalities. To achieve this goal, auto-manufacturers have been investing to realize the potential autonomous driving. In this regard, we present a self-driving model car capable of autonomous driving using object-detection as a primary means of steering, on a track made of colored cones. This paper goes through the process of fabricating a model vehicle, from its embedded hardware platform, to the end-to-end ML pipeline necessary for automated data acquisition and model-training, thereby allowing a Deep Learning model to derive input from the hardware platform to control the car's movements. This guides the car autonomously and adapts well to real-time tracks without manual feature-extraction. This paper presents a Computer Vision model that learns from video data and involves Image Processing, Augmentation, Behavioral Cloning and a Convolutional Neural Network model. The Darknet architecture is used to detect objects through a video segment and convert it into a 3D navigable path. Finally, the paper touches upon the conclusion, results and scope of future improvement in the technique used.

Keywords: autonomous, self-driving, computer vision, YOLO, object detection, embedded hardware.

I. Introduction

A 'Self-Driving Car' is one that is able to sense its immediate surroundings and operate independently without human intervention. The main motivation behind the topic at hand is the expeditious progress of applied Artificial Intelligence and the foreseeable significance of autonomous driving ventures in the future of humanity, from independent mobility for non-drivers to cheap transportation services to low-income individuals. The emergence of driverless cars and their amalgamation with electric cars promises to help minimize road fatalities, air and small-particle pollution, being able to better manage parking spaces, and free people from the mundane and monotonous task of having to sit behind the wheel. Autonomous navigation holds quite a lot of promise as it offers a range of applications going far beyond a car driven autonomously. The main effort here is to keep the humans out of the vehicle control loop and to relieve them from the task of driving. The prime requisite of self-driving vehicles are the visual sensors (for acquiring traffic insight of vehicle surroundings), microprocessors or computers (for processing the sensor information and transmitting vehicle control instructions) and actuators (to receive said instructions and be responsible for the longitudinal and lateral control of the car) [1-4]. Autonomous vehicles are also expected to be manoeuvred in many of the most complex human planned endeavours, such as asteroid mining [5]. The meteoric rise of AI along with deep learning (DL) methods and frameworks, have made possible the development of such autonomous vehicles by many venture companies at the same time.

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II. Software Development

In this section we elucidate the entire software development process which includes data collection and labelling, model training and model deployment.

a) Data Collection & Labelling

Around 2,000 images were collected for two types of coloured cones, namely: Orange and Blue. The cones were made from craft paper and were 4.5 centimetres tall with a base diameter of 3cm. The pictures included the cones laid out as track, single colour cones, multiple same-coloured cones and a mix of the two cones. A total of 16,382 cones were observed in the collected images with LabelImg being later used to label these cones from the images. 'LabelImg' is a graphical image annotation tool [6]. It is written in Python and uses Qt for its graphical interface. The LabelImg tool was used to label the photographed images in the YOLO format by drawing bounding boxes around the cones and naming each cone with their respective class i.e., colour (orange or blue). After labelling via LabelImg, a common class file was created to all images which contained the two classes "Orange" and "Blue". Another file was created unique to each image which contained the coordinates of each cone present in that image. For example, 1 0.490809 0.647894 0.235628 0.342580 is an entry from the class file created where the first parameter determines the class of the cones, the second and third parameters determine the midpoint of the bounding box while the fourth and fifth parameters determine the height and width of the bounding box. For the randomization

and renaming of the images, a software tool called 'Rename Expert' was used. It randomized the images and then named them from 0-1681. Data augmentation was used to increase the amount of data by adding slightly modified copies of already existing data. It involves injecting some noise, rotation and flipping of the images to increase the number of images used for training. It usually helps in preventing overfitting the model and acts as a regularizer [7].

b) Model Training

YOLOv4 Tiny, a version of YOLOv4 developed for edge and lower-power devices, is a real-time object detection algorithm capable of detecting and providing bounding boxes for many different objects in a single image [8-11]. The model achieves this by dividing an image into regions and then predicting bounding boxes in addition to the probabilities for each region. Relative to inference speed, YOLOv4 outperforms other object detection models by a significant margin. We needed a model that prioritizes real-time detection and conducts the training on a single GPU as well. 'Darknet' is a framework like the Tensor Flow, PyTorch and Keras that proved to be apt for the task at hand. While Darknet is not as intuitive to use, it is immensely flexible, and it advances state-of-the-art object detection results. We train the model on darknet and then later convert it to Tensor Flow for ease in usability. This model can be tested on a physical model or on virtual simulators [12-15].In terms of training the model, the labelled dataset was segregated into training and validation datasets and was uploaded on cloud VM. After that, the darknet was cloned and built on which the model was trained. The parameters were configured periodically to achieve the best weights. It was important that we convert our darknet framework into Tensor Flow because only then could we make use of the Tensor Flow lite model which is optimized for embedded devices such as Jetson Nano to make the inference at the edge.

c) Deployment

Deployment includes reading the coordinate text data generated from the YOlO4 model into a NumPy framework and labelling the coordinate points according to the two classes, blue and orange. This is done by iterating through the text data line by line, and appending the required point objects into a python array, and finally converting the array into a NumPy format. Matplotlib is used to visualize the set of data points from the camera's perspective, on a 10 x 10 cm2 adjusted screen. Using the Scikit-Learn Library, a Linear Regression model is trained using the NumPy data. Two different models are to be trained; one for the blue set of cones, and one for the orange. Using the 'Linear Regression()' predefined method in the Scikit-Learn library, we could easily create a simple regression model without having to build the entire code for the model ourselves. The data is zipped and iterated through using a for loop. The output generated is explicitly converted into a list format. Two lines are created that pass through the orange cones and the blue cones. Again, a graph is plotted of Matplotlib for visual aid of the lines. Next, the equations of the previously formed lines are derived using simple geometric calculations. Straight line equations of the type: $ax + by + c = 0$ are obtained for both blue and orange lines. Next, the point of intersection of the two lines is calculated using the formula of point of intersection. The offset of this line is calculated from the centre of the screen and the x-coordinate of each point is subtracted by the corresponding point on the centre of the screen. This value is the mean deviation and will be used further to calculate the angle by which servo attached on the assembly is to be turned. Fig. 1 shows the outcome of the entire video capture and path mapping process.

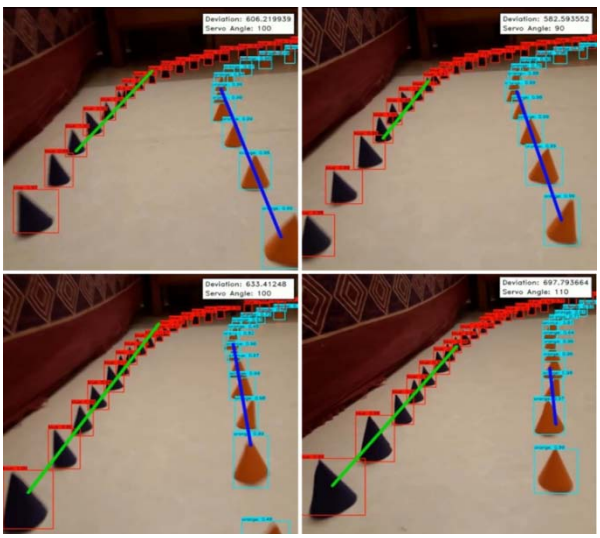

Fig. 1: Video Capture and Path Mapping Process

III. Hardware Design

Before The car was designed and built with the proper placement and positioning of electronic components, such as the camera, in mind. It consists of three main parts, the steering assembly, the spur gear gearbox and the wheels. The steering system has a rack and pinion type design, chosen for its simple assembly and for providing easier and more compact control over the car. A 3-sided gear box ensures the effortless placement and positioning of the axles and larger gears. Given the opposing forces caused by the axles and front chassis, it also stays strong and sturdy. Spur gears are used in the gear box as they have high power transmission efficiencies (95% to 99%) and are simple to design and install. The wheels are designed and entirely 3D printed to have built-in suspension providing additional steering stability. Because the wheels must be flexible, TPU (Thermoplastic Polyurethane) is used to produce them. All other 3D printed components were produced using PLA (Polylactic acid) as it's easy to use, has a remarkably low printing temperature compared to other thermoplastics and produces better surface details and sharper features. A list of all materials is given below:

List of Materials: All components required for the prototype, including sensors, actuators, power supply, and hardware, are listed here. Fig. 2 and Fig. 3 show all the 3D printed parts and their assembly in Soild Works Simscape respectively.

- 3D Printed Parts
- 608zz Bearings (4x)
- Nvidia Jetson Nano
- 1200KV Brushless DC Motor
- 20A ESC (Electronic Speed Controller)
- 5000mAh Power Bank
- 11.1V - 2200mAH (Lithium Polymer) LiPo Rechargeable Battery
- PCA9685 16 Channel Servo Driver
- TowerPro SG90 180° Rotation Servo Motor
- Logitech C615 HD Webcam

Fig. 2: 3D Printed Parts

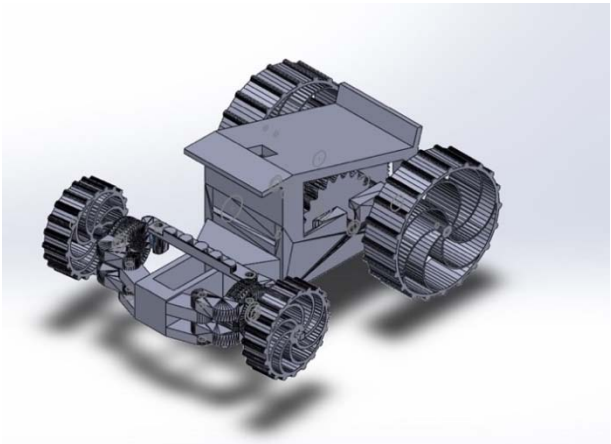

Fig. 3: Car Assembly on Solid Works Simscape

IV. Functionality

A Nvidia Jetson Nano single-board computer (SBC) serves as both the brain and the communication node in the prototype control system. This SBC receives data from the camera, analyses them, and integrates them into the navigation system to determine the steering angle. A 11.1V - 2200mAH LiPo battery is used solely to power the vehicle's propulsion system, that is, the 1200KV Brushless DC Motor with a 20A ESC. A 180° rotation servo motor with a torque of 1.2KgCm, controlled by the PCA9685 16 Channel Servo Driver, is used to steer the car. Fig. 4 and Fig. 5 show a flowchart of the instruction feedback loop and a schematic diagram of the hardware connections respectively. Fig. 6shows the entire assembled car.

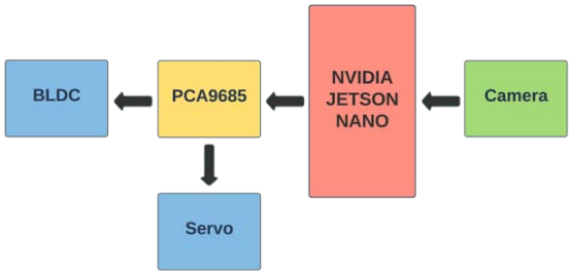

Fig. 4: Flowchart of the Instruction Feedback Loop

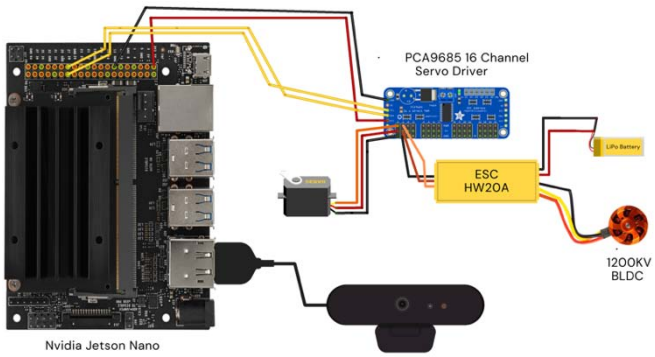

Fig. 5: Circuit Diagram

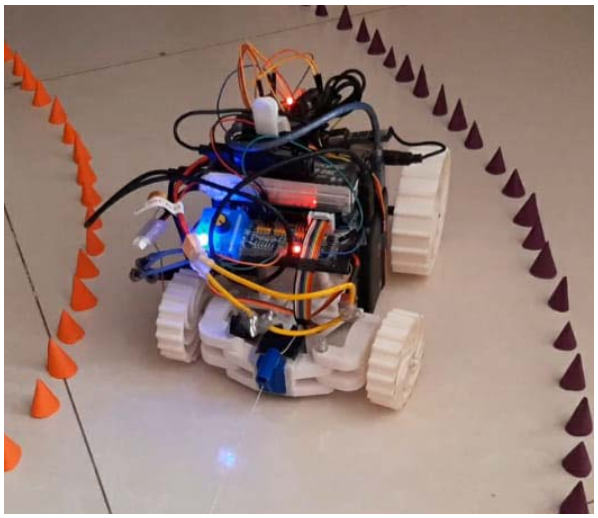

Fig. 6: Assembled Car

V. Conclusion

Through this paper, we present an approach for designing and building a model self-driving car based on the concept of Behavioural Cloning. This approach being an end-to-end one does not require any of the conventional tasks of feature extraction or connection of various modules, which are often monotonous, manual

in nature and necessary for efficient working. Our model car is tried and tested in real life against various standard models such as DenseNet-201, Resnet-50, and VGG19 for the comparison and performance. The final proposed model is a convolution-based, ten 2D-Convolutional Layers, one Flat Layer and four Dense Layers model. When compared with other Deep Learning based models, our model seems to have outperformed all of the aforementioned standard models by a substantial margin. The work presented through this paper can be realized to build vehicles capable of autonomous steering and driving. Additional training data of real-world obstacles with different track situations and conditions may be required to increase the agility and robustness of the system.

VI. Future Scope

Through this project, we aimed to provide proof of concept for self-driving cars that can solely rely on vision-based object detection techniques for navigation, rather than the conventional feature extraction-based lane detection techniques. Results obtained on our model car made it clear that our approach towards object detection as a means of steering has either outclassed or is at-par with humans in the parameters being tested for. Reinforcement learning methods can be introduced in addition to this method to better performance. This method can be used as a prototype for future citywide self-driving cars projects. It can also be used exclusively, or in addition to conventional lane detection, to further improve on accuracy of self-driving cars. Via these techniques, automobiles might truly serve as end-to-end personal transportation devices and may give rise to an entire ecosystem of car-pooling or car sharing services as well as numerous start-ups thereby making personal transport cheaper, faster and safer. However, when implementing in the real world, many more parameters might be introduced which may increase the complexity of such a system while affecting the performance of the car.

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The primary objective is to recognize the leaders in research and scientific fields of the current era with a global perspective and to create a channel between them and other researchers for better exposure and knowledge sharing. Members are most eminent scientists, engineers, and technologists from all across the world. Fellows are elected for life through a peer review process on the basis of excellence in the respective domain. There is no limit on the number of new nominations made in any year. Each year, the Open Association of Research Society elect up to 12 new Fellow Members.

Benefits

To the institution

Get letter of appreciation

Global Journals sends a letter of appreciation of author to the Dean or CEO of the University or Company of which author is a part, signed by editor in chief or chief author.

Exclusive Network

Get access to a closed network

A FCSRC member gets access to a closed network of Tier 1 researchers and scientists with direct communication channel through our website. Fellows can reach out to other members or researchers directly.They should also be open to reaching out by other.

Career | Credibility | Exclusive | Reputation

Certificate

Certificate, LoR and Laser-Momento

Fellows receive a printed copy of a certificate signed by our Chief Author that may be used for academic purposes and a personal recommendation letter to the dean of member's university.

Career | Credibility | Exclusive | Reputation

Designation

Get honored title of membership

Fellows can use the honored title of membership. The “FCSRC” is an honored title which is accorded to a person’s name viz. Dr. John E. Hall, Ph.D., FCSRC or William Walldroff, M.S., FCSRC.

Career | Credibility | Exclusive | Reputation

Recognition on the Platform

Better visibility and citation

All the Fellow members of FCSRC get a badge of "Leading Member of Global Journals" on the Research Community that distinguishes them from others. Additionally, the profile is also partially maintained by our team for better visibility and citation. All fellows get a dedicated page on the website with their biography.

Career | Credibility | Reputation

Future Work

Get discounts on the future publications

Fellows receive discounts on future publications with Global Journals up to 60%. Through our recommendation programs, members also receive discounts on publications made with OARS affiliated organizations.

Career | Financial

GJ Account

Unlimited forward of Emails

Fellows get secure and fast GJ work emails with unlimited forward of emails that they may use them as their primary email. For example, john [AT] globaljournals [DOT] org.

Career | Credibility | Reputation

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Access to all the premium tools

To take future researches to the zenith, fellows receive access to all the premium tools that Global Journals have to offer along with the partnership with some of the best marketing leading tools out there.

Financial

Conferences & Events

Organize seminar/conference

Fellows are authorized to organize symposium/seminar/conference on behalf of Global Journal Incorporation (USA). They can also participate in the same organized by another institution as representative of Global Journal. In both the cases, it is mandatory for him to discuss with us and obtain our consent. Additionally, they get free research conferences (and others) alerts.

Career | Credibility | Financial

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Early invitations to all the symposiums, seminars, conferences

All fellows receive the early invitations to all the symposiums, seminars, conferences and webinars hosted by Global Journals in their subject.

Exclusive

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Earn 60% of sales proceeds

Fellows can publish articles (limited) without any fees. Also, they can earn up to 70% of sales proceeds from the sale of reference/review books/literature/publishing of research paper. The FCSRC member can decide its price and we can help in making the right decision.

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Reviewers

Get a remuneration of 15% of author fees

Fellow members are eligible to join as a paid peer reviewer at Global Journals Incorporation (USA) and can get a remuneration of 15% of author fees, taken from the author of a respective paper.

Financial

Access to Editorial Board

Become a member of the Editorial Board

Fellows may join as a member of the Editorial Board of Global Journals Incorporation (USA) after successful completion of three years as Fellow and as Peer Reviewer. Additionally, Fellows get a chance to nominate other members for Editorial Board.

Career | Credibility | Exclusive | Reputation

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All members get access to 5 selected scientific museums and observatories across the globe. All researches published with Global Journals will be kept under deep archival facilities across regions for future protections and disaster recovery. They get 10 GB free secure cloud access for storing research files.

ASSOCIATE OF COMPUTER SCIENCE RESEARCH COUNCIL

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Benefits

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Exclusive Network

Get access to a closed network

A ACSRC member gets access to a closed network of Tier 2 researchers and scientists with direct communication channel through our website. Associates can reach out to other members or researchers directly.They should also be open to reaching out by other.

Career | Credibility | Exclusive | Reputation

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Organize seminar/conference

Associates are authorized to organize symposium/seminar/conference on behalf of Global Journal Incorporation (USA). They can also participate in the same organized by another institution as representative of Global Journal. In both the cases, it is mandatory for him to discuss with us and obtain our consent. Additionally, they get free research conferences (and others) alerts.

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Exclusive

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Earn 30-40% of sales proceeds

Associates can publish articles (limited) without any fees. Also, they can earn up to 30-40% of sales proceeds from the sale of reference/review books/literature/publishing of research paper.

Exclusive | Financial

Reviewers

Get a remuneration of 15% of author fees

Associate members are eligible to join as a paid peer reviewer at Global Journals Incorporation (USA) and can get a remuneration of 15% of author fees, taken from the author of a respective paper.

Financial

And Much More

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Associate	Fellow	Research Group	Basic
$4800 **lifetime designation**	$6800 **lifetime designation**	$12500.00 **organizational**	APC **per article**
Certificate, LoR and Momento **2** discounted publishing/year **Gradation** of Research **10** research contacts/day **1 GB** Cloud Storage **GJ** Community Access	**Certificate,** LoR and Momento **Unlimited** discounted publishing/year **Gradation** of Research **Unlimited** research contacts/day **5 GB** Cloud Storage **Online Presense** Assistance **GJ** Community Access	**Certificates,** LoRs and Momentos **Unlimited** free publishing/year **Gradation** of Research **Unlimited** research contacts/day **Unlimited** Cloud Storage **Online Presense** Assistance **GJ** Community Access	**GJ** Community Access

Preferred Author Guidelines

We accept the manuscript submissions in any standard (generic) format.

We typeset manuscripts using advanced typesetting tools like Adobe In Design, CorelDraw, TeXnicCenter, and TeXStudio. We usually recommend authors submit their research using any standard format they are comfortable with, and let Global Journals do the rest.

Alternatively, you can download our basic template from https://globaljournals.org/Template.zip

Authors should submit their complete paper/article, including text illustrations, graphics, conclusions, artwork, and tables. Authors who are not able to submit manuscript using the form above can email the manuscript department at submit@globaljournals.org or get in touch with chiefeditor@globaljournals.org if they wish to send the abstract before submission.

Before and during Submission

Authors must ensure the information provided during the submission of a paper is authentic. Please go through the following checklist before submitting:

1. Authors must go through the complete author guideline and understand and *agree to Global Journals' ethics and code of conduct,* along with author responsibilities.
2. Authors must accept the privacy policy, terms, and conditions of Global Journals.
3. Ensure corresponding author's email address and postal address are accurate and reachable.
4. Manuscript to be submitted must include keywords, an abstract, a paper title, co-author(s') names and details (email address, name, phone number, and institution), figures and illustrations in vector format including appropriate captions, tables, including titles and footnotes, a conclusion, results, acknowledgments and references.
5. Authors should submit paper in a ZIP archive if any supplementary files are required along with the paper.
6. Proper permissions must be acquired for the use of any copyrighted material.
7. Manuscript submitted *must not have been submitted or published elsewhere* and all authors must be aware of the submission.

Declaration of Conflicts of Interest

It is required for authors to declare all financial, institutional, and personal relationships with other individuals and organizations that could influence (bias) their research.

Policy on Plagiarism

Plagiarism is not acceptable in Global Journals submissions at all.

Plagiarized content will not be considered for publication. We reserve the right to inform authors' institutions about plagiarism detected either before or after publication. If plagiarism is identified, we will follow COPE guidelines:

Authors are solely responsible for all the plagiarism that is found. The author must not fabricate, falsify or plagiarize existing research data. The following, if copied, will be considered plagiarism:

- Words (language)
- Ideas
- Findings
- Writings
- Diagrams
- Graphs
- Illustrations
- Lectures

- Printed material
- Graphic representations
- Computer programs
- Electronic material
- Any other original work

Authorship Policies

Global Journals follows the definition of authorship set up by the Open Association of Research Society, USA. According to its guidelines, authorship criteria must be based on:

1. Substantial contributions to the conception and acquisition of data, analysis, and interpretation of findings.
2. Drafting the paper and revising it critically regarding important academic content.
3. Final approval of the version of the paper to be published.

Changes in Authorship

The corresponding author should mention the name and complete details of all co-authors during submission and in manuscript. We support addition, rearrangement, manipulation, and deletions in authors list till the early view publication of the journal. We expect that corresponding author will notify all co-authors of submission. We follow COPE guidelines for changes in authorship.

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Appealing Decisions

Unless specified in the notification, the Editorial Board's decision on publication of the paper is final and cannot be appealed before making the major change in the manuscript.

Acknowledgments

Contributors to the research other than authors credited should be mentioned in Acknowledgments. The source of funding for the research can be included. Suppliers of resources may be mentioned along with their addresses.

Declaration of funding sources

Global Journals is in partnership with various universities, laboratories, and other institutions worldwide in the research domain. Authors are requested to disclose their source of funding during every stage of their research, such as making analysis, performing laboratory operations, computing data, and using institutional resources, from writing an article to its submission. This will also help authors to get reimbursements by requesting an open access publication letter from Global Journals and submitting to the respective funding source.

Preparing your Manuscript

Authors can submit papers and articles in an acceptable file format: MS Word (doc, docx), LaTeX (.tex, .zip or .rar including all of your files), Adobe PDF (.pdf), rich text format (.rtf), simple text document (.txt), Open Document Text (.odt), and Apple Pages (.pages). Our professional layout editors will format the entire paper according to our official guidelines. This is one of the highlights of publishing with Global Journals—authors should not be concerned about the formatting of their paper. Global Journals accepts articles and manuscripts in every major language, be it Spanish, Chinese, Japanese, Portuguese, Russian, French, German, Dutch, Italian, Greek, or any other national language, but the title, subtitle, and abstract should be in English. This will facilitate indexing and the pre-peer review process.

The following is the official style and template developed for publication of a research paper. Authors are not required to follow this style during the submission of the paper. It is just for reference purposes.

Manuscript Style Instruction (Optional)

- Microsoft Word Document Setting Instructions.
- Font type of all text should be Swis721 Lt BT.
- Page size: 8.27" x 11'", left margin: 0.65, right margin: 0.65, bottom margin: 0.75.
- Paper title should be in one column of font size 24.
- Author name in font size of 11 in one column.
- Abstract: font size 9 with the word "Abstract" in bold italics.
- Main text: font size 10 with two justified columns.
- Two columns with equal column width of 3.38 and spacing of 0.2.
- First character must be three lines drop-capped.
- The paragraph before spacing of 1 pt and after of 0 pt.
- Line spacing of 1 pt.
- Large images must be in one column.
- The names of first main headings (Heading 1) must be in Roman font, capital letters, and font size of 10.
- The names of second main headings (Heading 2) must not include numbers and must be in italics with a font size of 10.

Structure and Format of Manuscript

The recommended size of an original research paper is under 15,000 words and review papers under 7,000 words. Research articles should be less than 10,000 words. Research papers are usually longer than review papers. Review papers are reports of significant research (typically less than 7,000 words, including tables, figures, and references)

A research paper must include:

a) A title which should be relevant to the theme of the paper.
b) A summary, known as an abstract (less than 150 words), containing the major results and conclusions.
c) Up to 10 keywords that precisely identify the paper's subject, purpose, and focus.
d) An introduction, giving fundamental background objectives.
e) Resources and techniques with sufficient complete experimental details (wherever possible by reference) to permit repetition, sources of information must be given, and numerical methods must be specified by reference.
f) Results which should be presented concisely by well-designed tables and figures.
g) Suitable statistical data should also be given.
h) All data must have been gathered with attention to numerical detail in the planning stage.

Design has been recognized to be essential to experiments for a considerable time, and the editor has decided that any paper that appears not to have adequate numerical treatments of the data will be returned unrefereed.

i) Discussion should cover implications and consequences and not just recapitulate the results; conclusions should also be summarized.
j) There should be brief acknowledgments.
k) There ought to be references in the conventional format. Global Journals recommends APA format.

Authors should carefully consider the preparation of papers to ensure that they communicate effectively. Papers are much more likely to be accepted if they are carefully designed and laid out, contain few or no errors, are summarizing, and follow instructions. They will also be published with much fewer delays than those that require much technical and editorial correction.

The Editorial Board reserves the right to make literary corrections and suggestions to improve brevity.

Format Structure

It is necessary that authors take care in submitting a manuscript that is written in simple language and adheres to published guidelines.

All manuscripts submitted to Global Journals should include:

Title

The title page must carry an informative title that reflects the content, a running title (less than 45 characters together with spaces), names of the authors and co-authors, and the place(s) where the work was carried out.

Author details

The full postal address of any related author(s) must be specified.

Abstract

The abstract is the foundation of the research paper. It should be clear and concise and must contain the objective of the paper and inferences drawn. It is advised to not include big mathematical equations or complicated jargon.

Many researchers searching for information online will use search engines such as Google, Yahoo or others. By optimizing your paper for search engines, you will amplify the chance of someone finding it. In turn, this will make it more likely to be viewed and cited in further works. Global Journals has compiled these guidelines to facilitate you to maximize the web-friendliness of the most public part of your paper.

Keywords

A major lynchpin of research work for the writing of research papers is the keyword search, which one will employ to find both library and internet resources. Up to eleven keywords or very brief phrases have to be given to help data retrieval, mining, and indexing.

One must be persistent and creative in using keywords. An effective keyword search requires a strategy: planning of a list of possible keywords and phrases to try.

Choice of the main keywords is the first tool of writing a research paper. Research paper writing is an art. Keyword search should be as strategic as possible.

One should start brainstorming lists of potential keywords before even beginning searching. Think about the most important concepts related to research work. Ask, "What words would a source have to include to be truly valuable in a research paper?" Then consider synonyms for the important words.

It may take the discovery of only one important paper to steer in the right keyword direction because, in most databases, the keywords under which a research paper is abstracted are listed with the paper.

Numerical Methods

Numerical methods used should be transparent and, where appropriate, supported by references.

Abbreviations

Authors must list all the abbreviations used in the paper at the end of the paper or in a separate table before using them.

Formulas and equations

Authors are advised to submit any mathematical equation using either MathJax, KaTeX, or LaTeX, or in a very high-quality image.

Tables, Figures, and Figure Legends

Tables: Tables should be cautiously designed, uncrowned, and include only essential data. Each must have an Arabic number, e.g., Table 4, a self-explanatory caption, and be on a separate sheet. Authors must submit tables in an editable format and not as images. References to these tables (if any) must be mentioned accurately.

Figures

Figures are supposed to be submitted as separate files. Always include a citation in the text for each figure using Arabic numbers, e.g., Fig. 4. Artwork must be submitted online in vector electronic form or by emailing it.

Preparation of Eletronic Figures for Publication

Although low-quality images are sufficient for review purposes, print publication requires high-quality images to prevent the final product being blurred or fuzzy. Submit (possibly by e-mail) EPS (line art) or TIFF (halftone/ photographs) files only. MS PowerPoint and Word Graphics are unsuitable for printed pictures. Avoid using pixel-oriented software. Scans (TIFF only) should have a resolution of at least 350 dpi (halftone) or 700 to 1100 dpi (line drawings). Please give the data for figures in black and white or submit a Color Work Agreement form. EPS files must be saved with fonts embedded (and with a TIFF preview, if possible).

For scanned images, the scanning resolution at final image size ought to be as follows to ensure good reproduction: line art: >650 dpi; halftones (including gel photographs): >350 dpi; figures containing both halftone and line images: >650 dpi.

Color charges: Authors are advised to pay the full cost for the reproduction of their color artwork. Hence, please note that if there is color artwork in your manuscript when it is accepted for publication, we would require you to complete and return a Color Work Agreement form before your paper can be published. Also, you can email your editor to remove the color fee after acceptance of the paper.

Tips for writing a good quality Computer Science Research Paper

Techniques for writing a good quality computer science research paper:

1. Choosing the topic: In most cases, the topic is selected by the interests of the author, but it can also be suggested by the guides. You can have several topics, and then judge which you are most comfortable with. This may be done by asking several questions of yourself, like "Will I be able to carry out a search in this area? Will I find all necessary resources to accomplish the search? Will I be able to find all information in this field area?" If the answer to this type of question is "yes," then you ought to choose that topic. In most cases, you may have to conduct surveys and visit several places. Also, you might have to do a lot of work to find all the rises and falls of the various data on that subject. Sometimes, detailed information plays a vital role, instead of short information. Evaluators are human: The first thing to remember is that evaluators are also human beings. They are not only meant for rejecting a paper. They are here to evaluate your paper. So present your best aspect.

2. Think like evaluators: If you are in confusion or getting demotivated because your paper may not be accepted by the evaluators, then think, and try to evaluate your paper like an evaluator. Try to understand what an evaluator wants in your research paper, and you will automatically have your answer. Make blueprints of paper: The outline is the plan or framework that will help you to arrange your thoughts. It will make your paper logical. But remember that all points of your outline must be related to the topic you have chosen.

3. Ask your guides: If you are having any difficulty with your research, then do not hesitate to share your difficulty with your guide (if you have one). They will surely help you out and resolve your doubts. If you can't clarify what exactly you require for your work, then ask your supervisor to help you with an alternative. He or she might also provide you with a list of essential readings.

4. Use of computer is recommended: As you are doing research in the field of computer science then this point is quite obvious. Use right software: Always use good quality software packages. If you are not capable of judging good software, then you can lose the quality of your paper unknowingly. There are various programs available to help you which you can get through the internet.

5. Use the internet for help: An excellent start for your paper is using Google. It is a wondrous search engine, where you can have your doubts resolved. You may also read some answers for the frequent question of how to write your research paper or find a model research paper. You can download books from the internet. If you have all the required books, place importance on reading, selecting, and analyzing the specified information. Then sketch out your research paper. Use big pictures: You may use encyclopedias like Wikipedia to get pictures with the best resolution. At Global Journals, you should strictly follow here.

6. Bookmarks are useful: When you read any book or magazine, you generally use bookmarks, right? It is a good habit which helps to not lose your continuity. You should always use bookmarks while searching on the internet also, which will make your search easier.

7. Revise what you wrote: When you write anything, always read it, summarize it, and then finalize it.

8. Make every effort: Make every effort to mention what you are going to write in your paper. That means always have a good start. Try to mention everything in the introduction—what is the need for a particular research paper. Polish your work with good writing skills and always give an evaluator what he wants. Make backups: When you are going to do any important thing like making a research paper, you should always have backup copies of it either on your computer or on paper. This protects you from losing any portion of your important data.

9. Produce good diagrams of your own: Always try to include good charts or diagrams in your paper to improve quality. Using several unnecessary diagrams will degrade the quality of your paper by creating a hodgepodge. So always try to include diagrams which were made by you to improve the readability of your paper. Use of direct quotes: When you do research relevant to literature, history, or current affairs, then use of quotes becomes essential, but if the study is relevant to science, use of quotes is not preferable.

10.Use proper verb tense: Use proper verb tenses in your paper. Use past tense to present those events that have happened. Use present tense to indicate events that are going on. Use future tense to indicate events that will happen in the future. Use of wrong tenses will confuse the evaluator. Avoid sentences that are incomplete.

11. Pick a good study spot: Always try to pick a spot for your research which is quiet. Not every spot is good for studying.

12. Know what you know: Always try to know what you know by making objectives, otherwise you will be confused and unable to achieve your target.

13. Use good grammar: Always use good grammar and words that will have a positive impact on the evaluator; use of good vocabulary does not mean using tough words which the evaluator has to find in a dictionary. Do not fragment sentences. Eliminate one-word sentences. Do not ever use a big word when a smaller one would suffice.

Verbs have to be in agreement with their subjects. In a research paper, do not start sentences with conjunctions or finish them with prepositions. When writing formally, it is advisable to never split an infinitive because someone will (wrongly) complain. Avoid clichés like a disease. Always shun irritating alliteration. Use language which is simple and straightforward. Put together a neat summary.

14. Arrangement of information: Each section of the main body should start with an opening sentence, and there should be a changeover at the end of the section. Give only valid and powerful arguments for your topic. You may also maintain your arguments with records.

15. Never start at the last minute: Always allow enough time for research work. Leaving everything to the last minute will degrade your paper and spoil your work.

16. Multitasking in research is not good: Doing several things at the same time is a bad habit in the case of research activity. Research is an area where everything has a particular time slot. Divide your research work into parts, and do a particular part in a particular time slot.

17. Never copy others' work: Never copy others' work and give it your name because if the evaluator has seen it anywhere, you will be in trouble. Take proper rest and food: No matter how many hours you spend on your research activity, if you are not taking care of your health, then all your efforts will have been in vain. For quality research, take proper rest and food.

18. Go to seminars: Attend seminars if the topic is relevant to your research area. Utilize all your resources.

19. Refresh your mind after intervals: Try to give your mind a rest by listening to soft music or sleeping in intervals. This will also improve your memory. Acquire colleagues: Always try to acquire colleagues. No matter how sharp you are, if you acquire colleagues, they can give you ideas which will be helpful to your research.

20. Think technically: Always think technically. If anything happens, search for its reasons, benefits, and demerits. Think and then print: When you go to print your paper, check that tables are not split, headings are not detached from their descriptions, and page sequence is maintained.

21. Adding unnecessary information: Do not add unnecessary information like "I have used MS Excel to draw graphs." Irrelevant and inappropriate material is superfluous. Foreign terminology and phrases are not apropos. One should never take a broad view. Analogy is like feathers on a snake. Use words properly, regardless of how others use them. Remove quotations. Puns are for kids, not grunt readers. Never oversimplify: When adding material to your research paper, never go for oversimplification; this will definitely irritate the evaluator. Be specific. Never use rhythmic redundancies. Contractions shouldn't be used in a research paper. Comparisons are as terrible as clichés. Give up ampersands, abbreviations, and so on. Remove commas that are not necessary. Parenthetical words should be between brackets or commas. Understatement is always the best way to put forward earth-shaking thoughts. Give a detailed literary review.

22. Report concluded results: Use concluded results. From raw data, filter the results, and then conclude your studies based on measurements and observations taken. An appropriate number of decimal places should be used. Parenthetical remarks are prohibited here. Proofread carefully at the final stage. At the end, give an outline to your arguments. Spot perspectives of further study of the subject. Justify your conclusion at the bottom sufficiently, which will probably include examples.

23. Upon conclusion: Once you have concluded your research, the next most important step is to present your findings. Presentation is extremely important as it is the definite medium though which your research is going to be in print for the rest of the crowd. Care should be taken to categorize your thoughts well and present them in a logical and neat manner. A good quality research paper format is essential because it serves to highlight your research paper and bring to light all necessary aspects of your research.

Informal Guidelines of Research Paper Writing

Key points to remember:

- Submit all work in its final form.
- Write your paper in the form which is presented in the guidelines using the template.
- Please note the criteria peer reviewers will use for grading the final paper.

Final points:

One purpose of organizing a research paper is to let people interpret your efforts selectively. The journal requires the following sections, submitted in the order listed, with each section starting on a new page:

The introduction: This will be compiled from reference matter and reflect the design processes or outline of basis that directed you to make a study. As you carry out the process of study, the method and process section will be constructed like that. The results segment will show related statistics in nearly sequential order and direct reviewers to similar intellectual paths throughout the data that you gathered to carry out your study.

The discussion section:

This will provide understanding of the data and projections as to the implications of the results. The use of good quality references throughout the paper will give the effort trustworthiness by representing an alertness to prior workings.

Writing a research paper is not an easy job, no matter how trouble-free the actual research or concept. Practice, excellent preparation, and controlled record-keeping are the only means to make straightforward progression.

General style:

Specific editorial column necessities for compliance of a manuscript will always take over from directions in these general guidelines.

To make a paper clear: Adhere to recommended page limits.

Mistakes to avoid:

- Insertion of a title at the foot of a page with subsequent text on the next page.
- Separating a table, chart, or figure—confine each to a single page.
- Submitting a manuscript with pages out of sequence.
- In every section of your document, use standard writing style, including articles ("a" and "the").
- Keep paying attention to the topic of the paper.
- Use paragraphs to split each significant point (excluding the abstract).
- Align the primary line of each section.
- Present your points in sound order.
- Use present tense to report well-accepted matters.
- Use past tense to describe specific results.
- Do not use familiar wording; don't address the reviewer directly. Don't use slang or superlatives.
- Avoid use of extra pictures—include only those figures essential to presenting results.

Title page:

Choose a revealing title. It should be short and include the name(s) and address(es) of all authors. It should not have acronyms or abbreviations or exceed two printed lines.

Abstract: This summary should be two hundred words or less. It should clearly and briefly explain the key findings reported in the manuscript and must have precise statistics. It should not have acronyms or abbreviations. It should be logical in itself. Do not cite references at this point.

An abstract is a brief, distinct paragraph summary of finished work or work in development. In a minute or less, a reviewer can be taught the foundation behind the study, common approaches to the problem, relevant results, and significant conclusions or new questions.

Write your summary when your paper is completed because how can you write the summary of anything which is not yet written? Wealth of terminology is very essential in abstract. Use comprehensive sentences, and do not sacrifice readability for brevity; you can maintain it succinctly by phrasing sentences so that they provide more than a lone rationale. The author can at this moment go straight to shortening the outcome. Sum up the study with the subsequent elements in any summary. Try to limit the initial two items to no more than one line each.

Reason for writing the article—theory, overall issue, purpose.

- Fundamental goal.
- To-the-point depiction of the research.
- Consequences, including definite statistics—if the consequences are quantitative in nature, account for this; results of any numerical analysis should be reported. Significant conclusions or questions that emerge from the research.

Approach:

- Single section and succinct.
- An outline of the job done is always written in past tense.
- Concentrate on shortening results—limit background information to a verdict or two.
- Exact spelling, clarity of sentences and phrases, and appropriate reporting of quantities (proper units, important statistics) are just as significant in an abstract as they are anywhere else.

Introduction:

The introduction should "introduce" the manuscript. The reviewer should be presented with sufficient background information to be capable of comprehending and calculating the purpose of your study without having to refer to other works. The basis for the study should be offered. Give the most important references, but avoid making a comprehensive appraisal of the topic. Describe the problem visibly. If the problem is not acknowledged in a logical, reasonable way, the reviewer will give no attention to your results. Speak in common terms about techniques used to explain the problem, if needed, but do not present any particulars about the protocols here.

The following approach can create a valuable beginning:

- Explain the value (significance) of the study.
- Defend the model—why did you employ this particular system or method? What is its compensation? Remark upon its appropriateness from an abstract point of view as well as pointing out sensible reasons for using it.
- Present a justification. State your particular theory(-ies) or aim(s), and describe the logic that led you to choose them.
- Briefly explain the study's tentative purpose and how it meets the declared objectives.

Approach:

Use past tense except for when referring to recognized facts. After all, the manuscript will be submitted after the entire job is done. Sort out your thoughts; manufacture one key point for every section. If you make the four points listed above, you will need at least four paragraphs. Present surrounding information only when it is necessary to support a situation. The reviewer does not desire to read everything you know about a topic. Shape the theory specifically—do not take a broad view.

As always, give awareness to spelling, simplicity, and correctness of sentences and phrases.

Procedures (methods and materials):

This part is supposed to be the easiest to carve if you have good skills. A soundly written procedures segment allows a capable scientist to replicate your results. Present precise information about your supplies. The suppliers and clarity of reagents can be helpful bits of information. Present methods in sequential order, but linked methodologies can be grouped as a segment. Be concise when relating the protocols. Attempt to give the least amount of information that would permit another capable scientist to replicate your outcome, but be cautious that vital information is integrated. The use of subheadings is suggested and ought to be synchronized with the results section.

When a technique is used that has been well-described in another section, mention the specific item describing the way, but draw the basic principle while stating the situation. The purpose is to show all particular resources and broad procedures so that another person may use some or all of the methods in one more study or referee the scientific value of your work. It is not to be a step-by-step report of the whole thing you did, nor is a methods section a set of orders.

Materials:

Materials may be reported in part of a section or else they may be recognized along with your measures.

Methods:

- Report the method and not the particulars of each process that engaged the same methodology.
- Describe the method entirely.
- To be succinct, present methods under headings dedicated to specific dealings or groups of measures.
- Simplify—detail how procedures were completed, not how they were performed on a particular day.
- If well-known procedures were used, account for the procedure by name, possibly with a reference, and that's all.

Approach:

It is embarrassing to use vigorous voice when documenting methods without using first person, which would focus the reviewer's interest on the researcher rather than the job. As a result, when writing up the methods, most authors use third person passive voice.

Use standard style in this and every other part of the paper—avoid familiar lists, and use full sentences.

What to keep away from:

- Resources and methods are not a set of information.
- Skip all descriptive information and surroundings—save it for the argument.
- Leave out information that is immaterial to a third party.

Results:

The principle of a results segment is to present and demonstrate your conclusion. Create this part as entirely objective details of the outcome, and save all understanding for the discussion.

The page length of this segment is set by the sum and types of data to be reported. Use statistics and tables, if suitable, to present consequences most efficiently.

You must clearly differentiate material which would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matters should not be submitted at all except if requested by the instructor.

Content:

- Sum up your conclusions in text and demonstrate them, if suitable, with figures and tables.
- In the manuscript, explain each of your consequences, and point the reader to remarks that are most appropriate.
- Present a background, such as by describing the question that was addressed by creation of an exacting study.
- Explain results of control experiments and give remarks that are not accessible in a prescribed figure or table, if appropriate.
- Examine your data, then prepare the analyzed (transformed) data in the form of a figure (graph), table, or manuscript.

What to stay away from:

- Do not discuss or infer your outcome, report surrounding information, or try to explain anything.
- Do not include raw data or intermediate calculations in a research manuscript.
- Do not present similar data more than once.
- A manuscript should complement any figures or tables, not duplicate information.
- Never confuse figures with tables—there is a difference.

Approach:

As always, use past tense when you submit your results, and put the whole thing in a reasonable order.

Put figures and tables, appropriately numbered, in order at the end of the report.

If you desire, you may place your figures and tables properly within the text of your results section.

Figures and tables:

If you put figures and tables at the end of some details, make certain that they are visibly distinguished from any attached appendix materials, such as raw facts. Whatever the position, each table must be titled, numbered one after the other, and include a heading. All figures and tables must be divided from the text.

Discussion:

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Position your understanding of the outcome visibly to lead the reviewer through your conclusions, and then finish the paper with a summing up of the implications of the study. The purpose here is to offer an understanding of your results and support all of your conclusions, using facts from your research and generally accepted information, if suitable. The implication of results should be fully described.

Infer your data in the conversation in suitable depth. This means that when you clarify an observable fact, you must explain mechanisms that may account for the observation. If your results vary from your prospect, make clear why that may have happened. If your results agree, then explain the theory that the proof supported. It is never suitable to just state that the data approved the prospect, and let it drop at that. Make a decision as to whether each premise is supported or discarded or if you cannot make a conclusion with assurance. Do not just dismiss a study or part of a study as "uncertain."

Research papers are not acknowledged if the work is imperfect. Draw what conclusions you can based upon the results that you have, and take care of the study as a finished work.

- You may propose future guidelines, such as how an experiment might be personalized to accomplish a new idea.
- Give details of all of your remarks as much as possible, focusing on mechanisms.
- Make a decision as to whether the tentative design sufficiently addressed the theory and whether or not it was correctly restricted. Try to present substitute explanations if they are sensible alternatives.
- One piece of research will not counter an overall question, so maintain the large picture in mind. Where do you go next? The best studies unlock new avenues of study. What questions remain?
- Recommendations for detailed papers will offer supplementary suggestions.

Approach:

When you refer to information, differentiate data generated by your own studies from other available information. Present work done by specific persons (including you) in past tense.

Describe generally acknowledged facts and main beliefs in present tense.

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Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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