

A Novel Two Switches Based Dc-Dc Multilevel Voltage Multiplier

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Abstract – This paper proposes a novel dc-dc converter called the dc-dc multilevel voltage multiplier (mvm). In general, an $N \times$ mvm can be built by using two switches, $2N-2$ diodes and $2N-2$ capacitors, free of magnetic components. It is based on the multilevel converters principle and designed for unidirectional power transfer applications. Each device blocks one voltage level, therefore high voltage converters can be synthesized with low voltage devices. The main advantage of this topology is the reduced number of transistors and gate drives. Possible applications have a wide range from low power silicon-based voltage multipliers to medium power level dc links for multilevel inverters based distributed generation (dg) systems, where a capacitor's voltage balancing is a challenge for more than three levels. Experimental results prove the principle of such converters. **Index terms** – dc-dc converter, multilevel converter, voltage multiplier.

I. INTRODUCTION

Multilevel converters have attracted interest in power conversion [1][8], being the main reason that the devices are exposed to low voltage stress, which means that high voltage converters can be developed using low voltage devices, which is important for high power applications [1][2]. Relative to conventional topologies, some additional advantages of multilevel converters are: (i) low harmonic distortion, (ii) low electromagnetic emission noise, (iii) low switching frequency, (iv) high efficiency, (v) able to operate without magnetic components [2][3][8]. Multilevel converters are one of the most important topics in power electronics, and industrial application research, the three main topologies are: (i) diode clamped, (ii) capacitor-clamped, and (iii) cascaded multi-cell. A generalized topology is proposed in [3], showing that all basic structures and new multilevel topologies can be derived from the generalized topology. It has been shown in [2] that in DC-DC applications the diode-clamped multilevel converter has a voltage capacitor's unbalance problem, because it cannot provide redundant switching states to control capacitors voltage, but the capacitor-clamped multilevel converter have been successfully used for DC-DC conversion in low power converters [2][5][6][10] and ultra low power silicon based converters [9] mainly as a voltage multiplier. Most of the multilevel converter applications are focused in high power motor drives, static VARs generation, and other utility applications [1][2][8]. They are also suitable for FACTS devices [4], low power DC-DC conversion, specially for automotive applications [6] [10], and renewable energy systems [4][5][7]. Initially proposed for DC-AC and AC-DC conversion, it has been shown in [2] that DC-DC converters

generalized topology. They eliminate magnetic components, although they present drawbacks in the capacitor's voltage balancing, being this the main challenge.

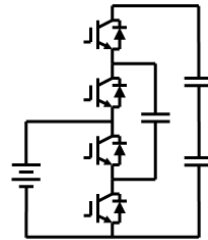


Fig. 1. Two-levels capacitor-clamped DC-DC multilevel converter. This paper proposes a new DC-DC converter, named *DC-DC Multilevel Voltage Multiplier* (MVM), based on two switches, $2N-2$ diodes, and $2N-2$ capacitors, for an $N \times$ converter. It is a voltage multiplier able to maintain and balance the output voltage levels. The reduced number of switches saves valuable circuits in the gate drive. An additional advantage is that the number of levels can be increased by adding diodes and capacitors, and an entire converter can be built with several modules. This converter is based in the multilevel converters' principle; it is proposed for unidirectional power flow applications such as distributed generation to link the DC renewable energy system with a multilevel inverter, and ultra low power applications, such as silicon DC-DC-based converters, and for all applications where a voltage needs to be multiplied without magnetic components and several voltage levels need to be references to the same point. The topology is simulated and prototyped; experimental results are provided.

II. DC-DC MULTILEVEL VOLTAGE MULTIPLIER

Fig. 2 depicts the proposed topology, where the number of switches doesn't depend on the numbers of levels. To explain its operation principle, a $3 \times$ MVM is analyzed, simulated and prototyped.

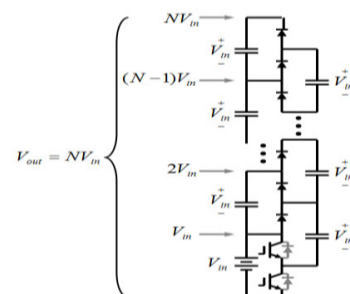


Fig. 2. $N \times$ Multilevel Voltage Multiplier.

Fig. 3 shows the three-level MVM, based on four diodes, four capacitors, and two switches, implemented with IGBTs. The IGBT switches functioning in a complementary way, when switch S1 is turned on, switch S2 is turned off and vice versa with a fixed duty cycle of 0.5. The control is very simple, and it doesn't even need a microcontroller; an oscillator can provide the gate drive signals.

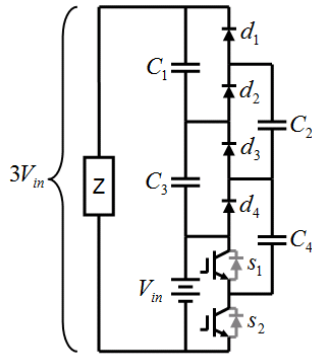


Fig. 3. 3x DC-DC Multilevel Voltage Multiplier.

The converter's operating principle is explained utilizing Fig. 3-5, where a duty cycle (D) equal to 0.5 is assumed. When S1 is *off* and S2 is *on*, C4 is charged to V_{in} , Fig. 4a. At the same time, C2 and C4 are connected to V_{in} and C3, Fig. 4b, while load is connected to V_{in} , C1, and C3, Fig. 4c. Then C4 is clamped to voltage V_{in} , and C2 is clamped to C3. Similarly, when S1 is *on* and S2 is *off*, C4 clamps to C3, Fig. 5a, and the voltage across C1 and C3 is clamped by the voltage across C2 and C4, Fig. 5b; the load Z is connected to V_{in} , C2, and C4, Fig. 5c. Thus, all capacitors are subjected to the same voltage V_{in} . From Fig. 4-5 all diodes and switches block just one voltage level, and a high voltage converter can be implemented with low voltage devices.

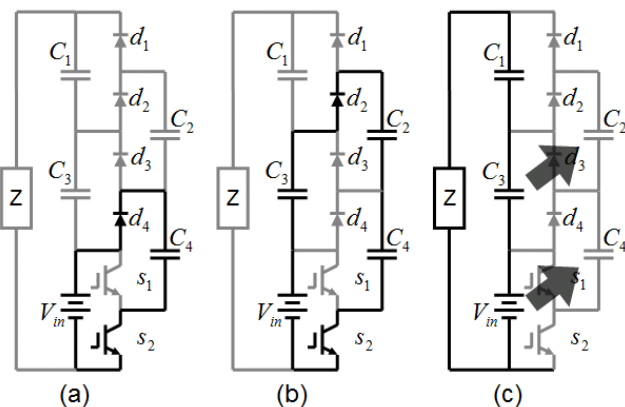


Fig. 4. S1 is off S2 is on.

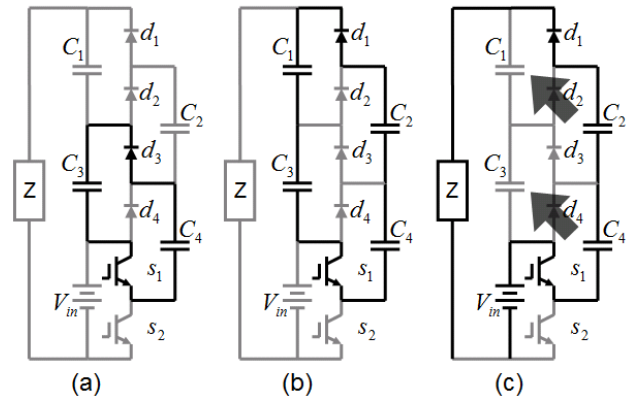


Fig. 5. S1 is on and S2 is off.

This strategy keeps all capacitors' voltage to V_{in} , and the number of gate drive circuits is limited to two. The number of levels can be increased in a modular way, adding diodes and capacitors, allowing a multistage structure. The self-balancing's voltage capacitor allows the MVM to feed neutral points multilevel inverters for more than three levels, where the neutral point topology cannot balance the capacitors' voltage by itself.

III. DIODE AND SWITCH VOLTAGE DROP LIMITATION

In actual implementations the switches' and diodes' voltage drop must be taken into account since it avoids capacitors to be charged to V_{in} , this effect is studied in the present section. The voltage drop in conventional IGBTs and power diodes are around 2 volts, and it can be ignored in medium and high power applications with several hundred volts, but in low voltage applications should be considered. For simplicity, the voltage drop in switches and diodes is assumed to be equal to V_d . From Fig. 4a and Fig 6 it can be seen that the actual voltage across C4 becomes:

$$\begin{aligned} V_{C4} &= V_{in} - V_{switch} - V_{Diode} \\ V_{C4} &= V_{in} - 2V_d \end{aligned} \quad (1)$$

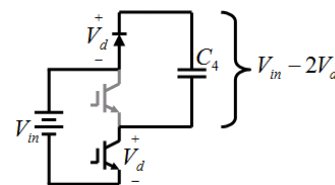


Fig. 6. Charging C4 with diode's and switch's voltage-drop.

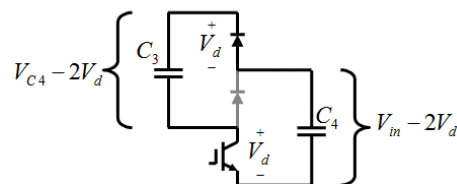


Fig. 7. Charging C3 with diode's and switch's voltage-drop.

From Fig. 5a, Fig 7, and (1), it can be written:

$$V_{C3} = V_{C4} - 2V_d = V_{in} - 4V_d \quad (2)$$

C2 is charged from V_{in} and C3 with C4 in series, as it is shown in Fig. 4b and Fig. 8. The voltage across C2 can be evaluated by:

$$\begin{aligned} V_{in} + V_{C3} - 2V_d &= V_{C4} + V_{C2} \\ V_{in} + (V_{in} - 4V_d) - 2V_d &= (V_{in} - 2V_d) + V_{C2} \\ V_{C2} &= V_{in} - 4V_d \end{aligned} \quad (3)$$

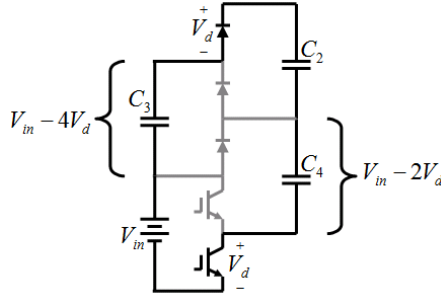


Fig.8. Charging C2 with diode's and switch's voltage-drop.

Likewise, C1 is charged in a similar way as it can be seen in Fig. 5b and Fig 9. Voltage across C1 can be expressed as:

$$\begin{aligned} V_{C4} + V_{C2} - 2V_d &= V_{C3} + V_{C1} \\ (V_{in} - 2V_d) + (V_{in} - 4V_d) - 2V_d &= (V_{in} - 4V_d) + V_{C1} \\ V_{C1} &= V_{in} - 4V_d \end{aligned} \quad (4)$$

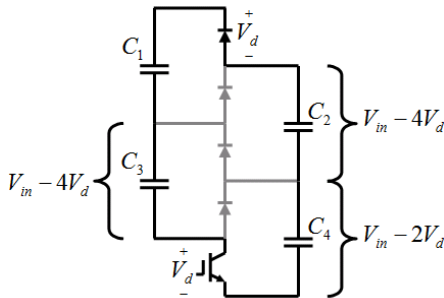


Fig.9. Charging C1 with diode's and switch's voltage-drop.

From (1)-(4), Fig. 3 becomes Fig 10, and the expression for the output voltage is as follows:

$$V_{out} = V_{in} - 8V_d \quad (5)$$

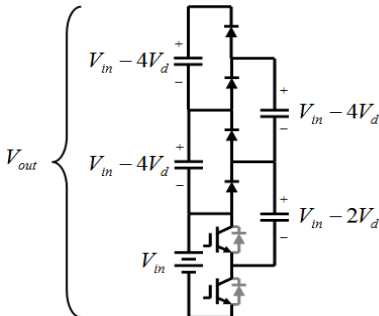


Fig.10. 3x MVM adding the diodes' and switches' voltage-drop.

Fig. 11 displays the equivalent to Fig. 2 including all the devices' forward voltage-drop. Finally, the general expression for the output voltage in an Nx multilevel voltage multiplier is shown in (6). This one must be considered to design an multilevel voltage multiplier:

$$V_{out} = NV_{in} - (N-1)4V_d \quad (6)$$

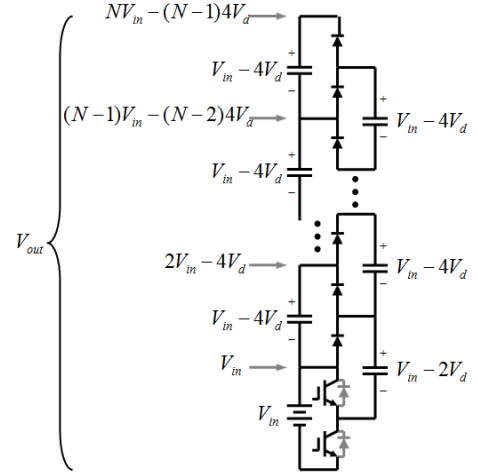


Fig.11. Nx MVM including diodes' and switches' voltage-drop.

The previous analysis indicates that the total output voltage is limited by the devices' forward voltage-drop, although the voltage capacitor keeps practically equal and constant, independent of the capacitor's level, except the lower one which exhibits a slight higher voltage. The load doesn't affect the multilevel operation, and all capacitors have a self-balanced voltage; this fact allows the MVM to feed multilevel inverters or loads with several voltage levels. A similar analysis can be done for all multilevel converters to get the actual output voltage taken into account the discrete devices' voltage-drop.

IV. EXPERIMENTAL RESULTS

The circuit in Fig. 3 is simulated in *-Saber* and prototyped. Capacitors have a capacitance of $C = 12000\mu F$, Fig. 12.

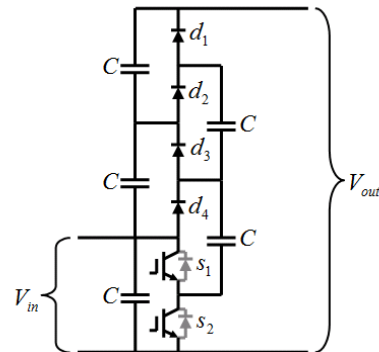


Fig. 12. MVM schematic prototype, $C = 12000\mu F$.

The two gate drive signals are provided by an eight bits Freescale microcontroller model MC68HC908QT4CP. Fig. 13 and Fig. 14 exhibit the test bench.

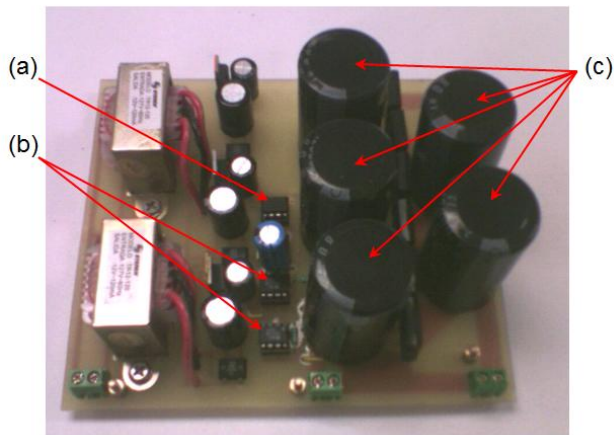


Fig. 13. (a) Microcontroller, (b) gate drives, (c) capacitors.

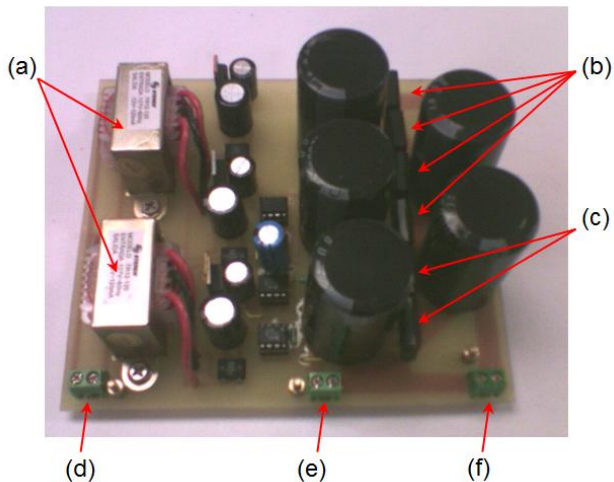


Fig. 14. (a) Isolated gate drives power supplies, (b) diodes, (c) IGBTs, (d) gate drives power input, (e) DC input voltage, (f) DC output voltage.

Fig. 15 illustrates the gate drive signals generated by the microcontroller at 5.7 kHz with a security dead-time. Several tests were done, Fig. 15-18 show the test waveforms. Fig. 15 shows the gate drive signals generated by the microcontroller, the duty cycle is 50%, and a dead-time was included. Fig. 16 displays the voltage across the lower device S2. Fig. 17-18 present the input and output voltage for two cases: (i) $V_{in} = 20V$, (ii) $V_{in} = 30V$.

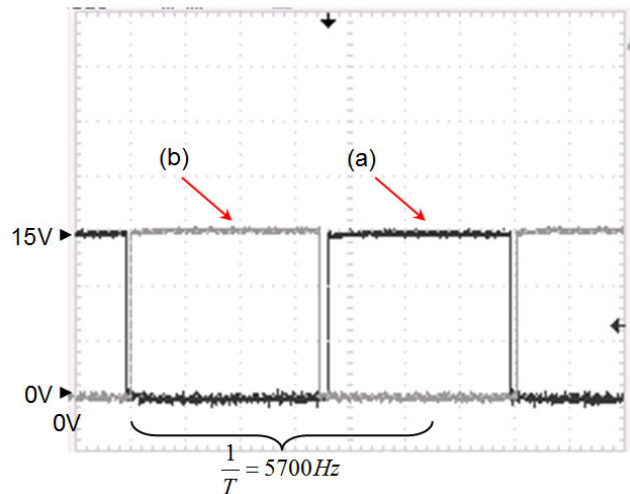


Fig. 15. (a) S1 gate signal, (b) S2 gate signals.

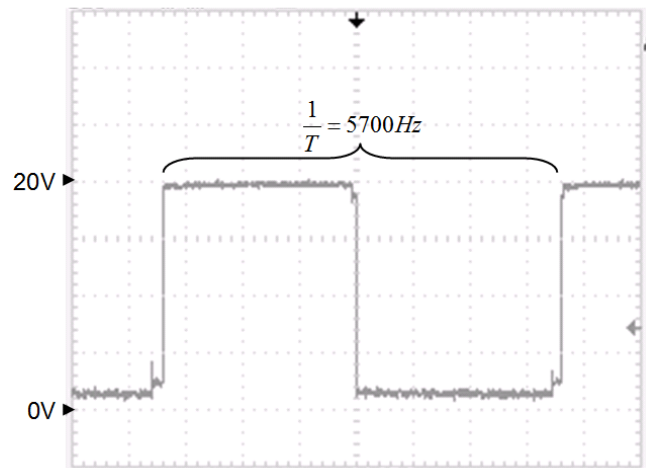


Fig.16. Voltage across S2 with an input voltage of 20V.

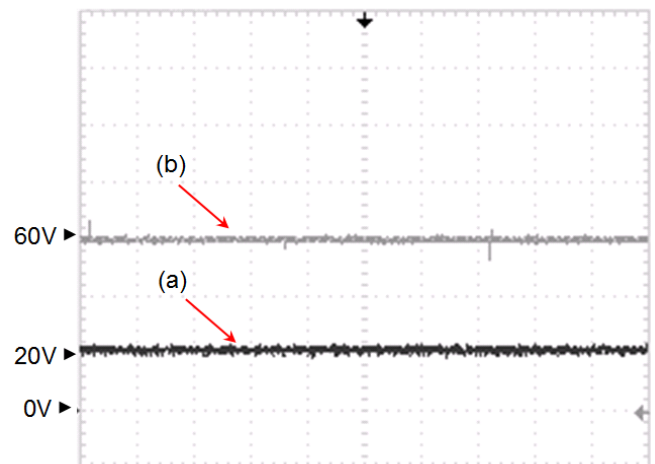


Fig. 17. (a) Input voltage, (b) output voltage.

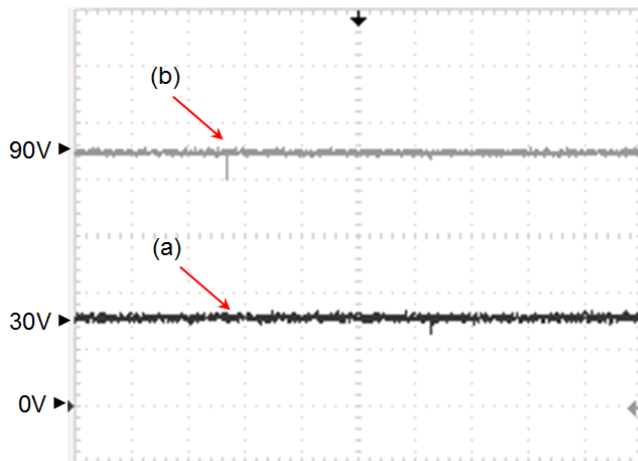


Fig. 18. (a) Input voltage, (b) output voltage.

V. CONCLUSION

A novel DC-DC N_x converter has been proposed, based on two switches, $2N-2$ diodes and $2N-2$ capacitor. It is a voltage multiplier able to maintain closely the same voltage level in all output levels. The effect of diodes' and switches' voltage-drop has been analyzed, and the output voltage expression has been corrected according to such analysis, which can be applied to all multilevel converters. The reduced number of switches saves valuable circuits in the gate drive, reducing the price in low power applications. The number of levels can be increased just adding diodes and capacitors achieving a modular topology. This converter is proposed for unidirectional power flow applications, such as distributed generation to link the DC renewable energy system with a multilevel inverter, or ultra low power application such as silicon based DC-DC converters, and for all applications where a DC voltage needs to be multiplied without magnetic components, the topology is simulated and prototyped; experimental results are provided.

VI. REFERENCES

- 1) Rodriguez, J.; Jih-Sheng Lai; Fang Zheng Peng; Multilevel inverters: a survey of topologies, controls, and applications Industrial Electronics, IEEE Transactions on Volume 49, Issue 4, Aug. 2002 Page(s):724–738.
- 2) Fan Zhang; Peng, F.Z.; Zhaoming Qian; Study of the multilevel converters in DC-DC applications Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual Volume 2, 20-25 June 2004 Page(s):1702 - 1706 Vol.2
- 3) Fang Zheng Peng; A generalized multilevel inverter topology with self voltage balancing Industry Applications, IEEE Transactions on Volume 37, Issue 2, March-April 2001 Page(s):611 – 618.
- 4) Tolbert, L.M.; Peng, F.Z.; Multilevel converters as a utility interface for renewable energy systems Power Engineering Society Summer Meeting, 2000. IEEE Volume 2, 16-20 July 2000 Page(s):1271-1274 vol. 2.

- 5) Khan, F.H.; Tolbert, L.M.; A Multilevel Modular Capacitor-Clamped DC-DC Converter Industry Applications, IEEE Transactions on Volume 43, Issue 6, Nov.-dec. 2007 Page(s):1628 – 1638.
- 6) Fang Zheng Peng; Fan Zhang; Zhaoming Qian; A magnetic-less DC-DC converter for dual-voltage automotive systems Industry Applications, IEEE Transactions on Volume 39, Issue 2, March-April 2003 Page(s):511 – 518.
- 7) Walker, G.R.; Sernia, P.C.; Cascaded DC-DC converter connection of photovoltaic modules Power Electronics, IEEE Transactions on Volume 19, Issue 4, July 2004 Page(s):1130 – 1139.
- 8) Jih-Sheng Lai; Fang Zheng Peng; Multilevel converters-a new breed of power converters Industry Applications, IEEE Transactions on Volume 32, Issue 3, May-June 1996 Page(s):509 – 517.
- 9) Corona-Murguia, O.; Sandoval-Ibarra, F.; A Silicon-based Voltage Doubler: Preliminary Results Electrical and Electronics Engineering, 2006 3rd International Conference on Sept. 2006 Page(s):1 – 4.
- 10) Peng, F.Z.; Fan Zhang; Zhaoming Qian; A novel compact DC-DC converter for 42 V systems Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual Volume 1, 15-19 June 2003 Page(s):33 - 38 vol.1.