Global Journal of researches in engineering
Electrical and Electronics engineering
Volume 11 Issue 7 Version 1.0 December 2011
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

FPGA Based Sigma Delta Modulator Design for Biomedical Application Using Verilog HDL

By Sheikh Md. Rabiul Islam, A. F. M. Nokib Uddin
University of Engineering and Technology, Khulna, Bangladesh

Abstract - This paper proposes the design of micro power Sigma-delta modulator with using verilog HDL based on been mapped on small commercially available FPGAs (Field Programmable Gate Arrays). This Sigma-delta modulator design is paid special attention to its low power application of portable electronic system in digitizing biomedical signals such asElectrocardiogram(ECG),Electroencephalogram(EEG) etc. A high performance, low power second order Sigma-delta modulator is more useful in analog signal acquisition system. Using Sigma-delta modulator can reduce the power consumption and cost in the whole system. The original biomedical signal can be reconstructed by simply applying the digital bit stream from the modulator output through a low-pass filter. In this second order sigma delta modulator simulation result there is no distortion. It is very suitable for low power application of biomedical instrument design. Key words- Sigma delta modulator, Low power, Verilog HDL, biomedical application.

Keywords : *Sigma delta modulator, Low power, Verilog HDL, biomedical application.*

GJRE-F Classification : *FOR Code: 090609*

Strictly as per the compliance and regulations of :

FPGA Based Sigma Delta Modulator Design for Biomedical Application Using Verilog HDL

Sheikh Md. Rabiul Islam[α], A. F. M. Nokib Uddin[Ω]

Abstract - This paper proposes the design of micro power Sigma-delta modulator with using verilog HDL based on been mapped on small commercially available FPGAs (Field Programmable Gate Arrays). This Sigma-delta modulator design is paid special attention to its low power application of portable electronic system in digitizing biomedical signals such asElectrocardiogram(ECG),Electroencephalogram(EEG) etc. A high performance, low power second order Sigma-delta modulator is more useful in analog signal acquisition system. Using Sigma-delta modulator can reduce the power consumption and cost in the whole system. The original biomedical signal can be reconstructed by simply applying the digital bit stream from the modulator output through a low-pass filter. In this second order sigma delta modulator simulation result there is no distortion. It is very suitable for low power application of biomedical instrument design. Key words- Sigma delta modulator, Low power, Verilog HDL, biomedical application.

Keywords : Sigma delta modulator, Low power, Verilog HDL, biomedical application.

I. Introduction

The application of portable electronic systems such as wireless communication devices, consumer electronics and battery powered biomedical devices ECG, EEG [1] increases the requirement for low-voltage and low- power circuit techniques [2]. Designing of low-voltage circuit can reduce the number of battery cells for low weight and small system size. At the same time, low- power circuit design can increase the operation time for biomedical application [3].Sigma-delta modulator has become a usual technique for analog-to-digital (A/D) conversion. This is because sigma delta modulators circuits are structured simply with low-accuracy analog parts and very suitable in low frequency, high performance and low power application. The single-bit signals of sigma- delta modulator are converted into multi-bit signals at the Nyquist sampling rate for biomedical application. Thus, currently usable types of biomedical systems with sigma-delta based A/D converter need single-bit conversion hardware including decimation filter. Sigma-delta modulator utilizes a negative feedback loop consist of an integrator, comparator and one-bit DAC that are very simply components. The input analog signal is first integrated and compared with ground using comparator. Its output drives a one bit DAC which switches reference voltages to the summing node of the integrator, minimizing the difference signal. In this paper, the second order sigma delta modulator can be widely utilized for low-power with biomedical applications.

Author[αΩ] : Department of Electronics and Communication Engineering Khulna University of Engineering and Technology, Khulna-9203, Bangladesh. E-mail[α] : robi@ece.kuet.ac.bd, E-mail[Ω] : nokib.ece@gmail.com

II. Background

Suppressing the power consumption will be widely utilized for biomedical application. At the same time, in order to get accurate data, the simple Sigma-delta modulation is first-selected to incorporate on the system chip definitely. Sigma-delta modulator has proven to be very suitable in low frequency, high-performance application. A simple block diagram of the second order Sigma Delta Modulator is shown in Figure 1, where x (t) and y (t) are the input and the output signal of sigma delta modulator respectively. The values of y (t) have only two levels as the output because of 1-bit ADC which is comparator is simply used. The 1-bit ADC and DAC are both driven by the same clock signal. Due to the non-linearity incorporated in the ADC, simpler model is used for analysis. The system can be viewed in its discrete time in Figure 2.

The comparator is replaced by an adder and sum of noise source Q[z] emulating the quantization noise. The integrator is replaced by the function block of z-1/ (1-z-1). After some mathematical manipulations in Figure 2, the time-domain, we can get

$$y(n) = x(n-2) + q(n) - 2q(n-1) + q(n-2) + 3y(n-1) - 3y(n-2)$$

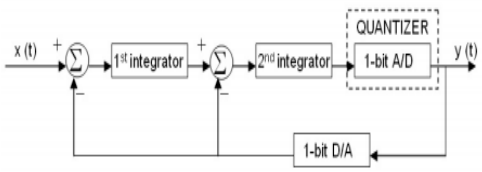

Fig.1: Block diagram of second order sigma delta modulator.

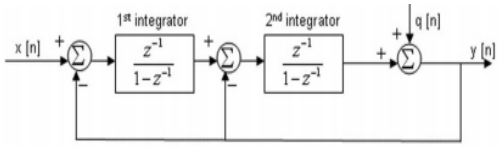

Fig.2 : Simplified model for second order sigma delta modulator.

III. Proposed Architecture for Second Order Sigma Delta Modulator

In this section, block diagram of our proposed architecture of programmable digital filter has been represented based on data bus, control bus and including internal connection.

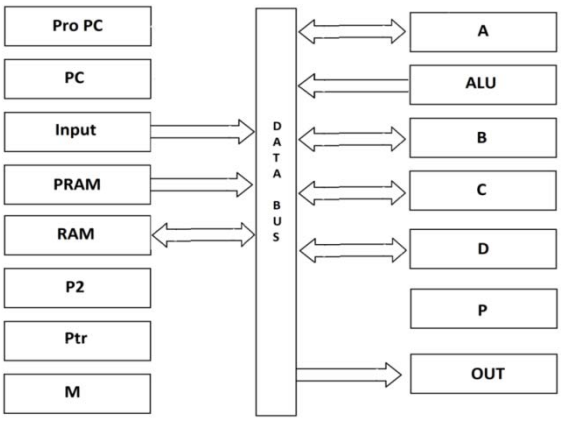

Fig.3 : Block diagram of the system sigma delta modulator.

In proposed architecture as shown in Fig.3 Pro PC block is used to control the output state of the program counter (PC). First the input data and error bits are saved in the internal register of the Input block. When the PC starts counting then the Control block starts to control the operation of the device automatically. The PRAM block is a Programmable RAM, which contains the educational specification of the second order modulator and RAM block is a permanent memory for the proposed architecture. The Pointer (Ptr) and P block are used to generate address for the RAM according to the instruction of PRAM block. The P2 block points the memory location and read the saved data of PRAM by using some control signals.

The arithmetic and logic unit (ALU) performs the all arithmetic and logic operation of the proposed architecture and save data temporarily. The Register A, B and C are used to save data for performing the operation of ALU and the output block is used to get the output. The Middle(M) block contains some special common bus.

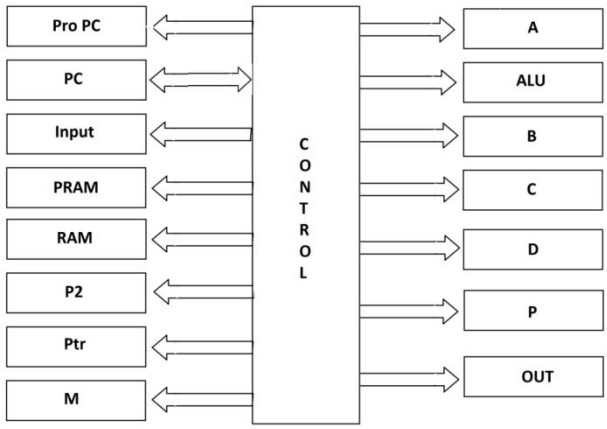

Fig.4 : Block diagram of the system including control bus.

IV. Synthesis Result

The simulation result of the 2nd order sigma delta modulator for the proposed architecture contains the block diagram and the timing diagram of each block.

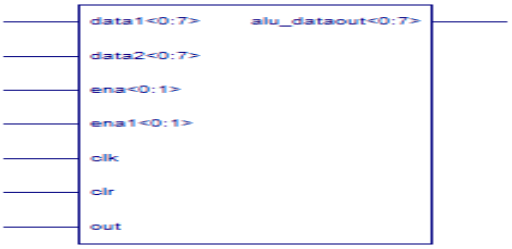

Fig.5 : Block diagram of ALU.

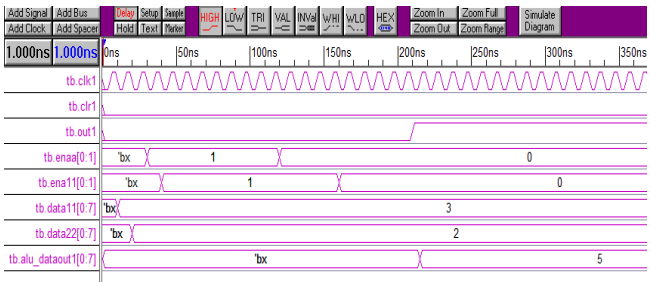

Fig.6 : Timing diagram of ALU.

In this timing diagram the addition of two data is done. We have given the data 2 and 3 is added and the output is 5 as shown in Fig.6.

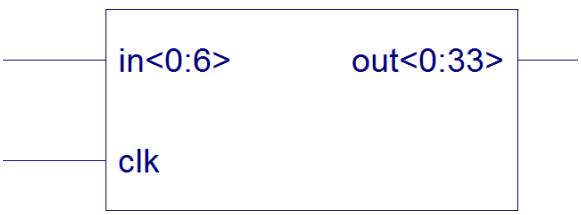

Fig.7 : Block diagram of Control unit.

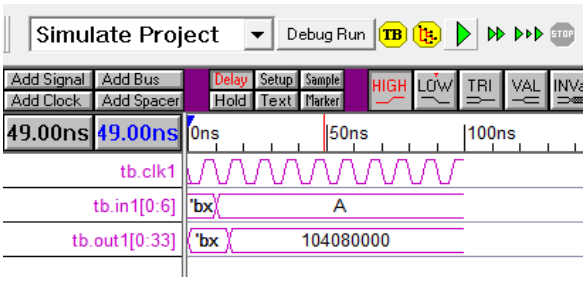

Fig.8 : Timing diagram of Control unit.

After the synthesized the block diagram the control unit as shown in Fig.7. The execution of process data gets a signal A in hexadecimal format and makes a 34bit control signal as shown in Fig 8..

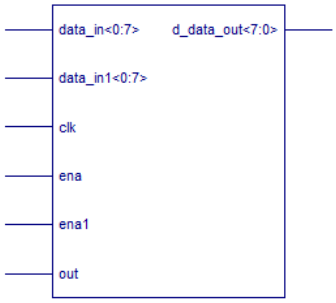

Fig.10 : Block diagram of Input block.

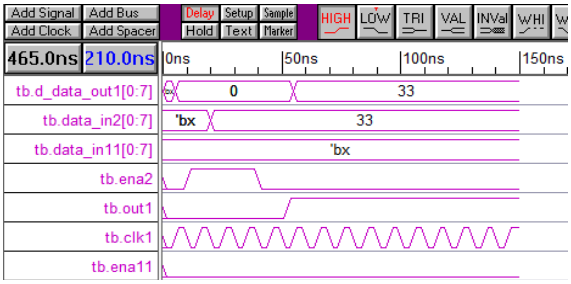

Fig.11 : Timing diagram of Input block.

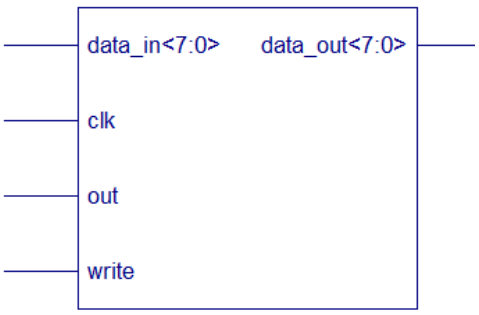

Fig.12 : Block diagram of OUT block.

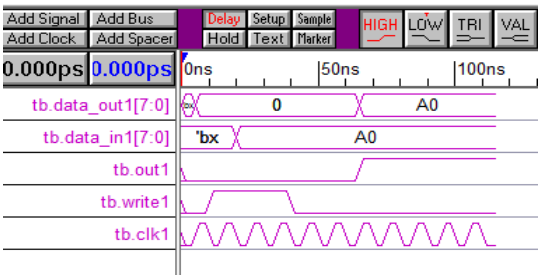

Fig.13 : Timing diagram of OUT block.

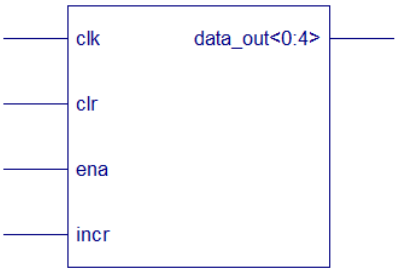

Fig.14 : Block diagram of P2 block.

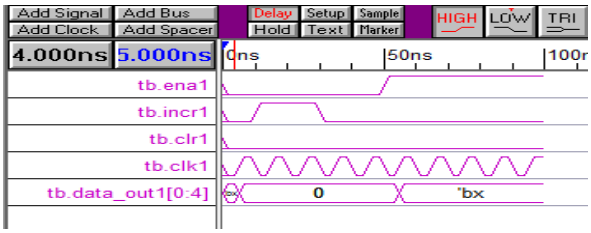

Fig.15 : Timing diagram of P2.

In the timing diagram as shown in Fig.15 the output is 0 because the output control signal is low at the first time it generate a address which index is 0 as a memory location.

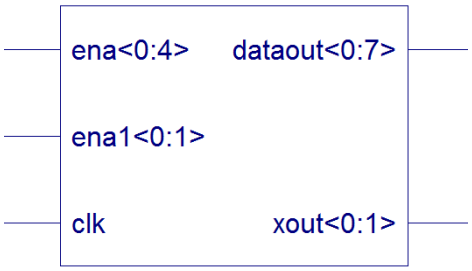

Fig.16 : Block diagram of PRAM.

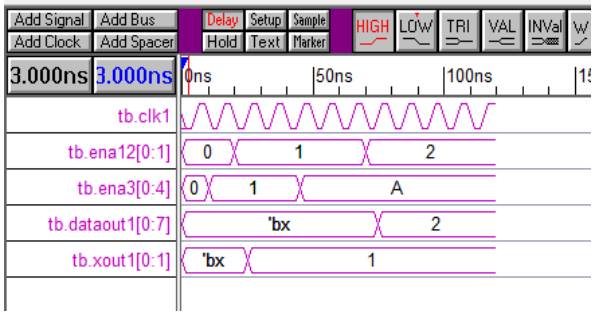

Fig.17 : Timing diagram of PRAM.

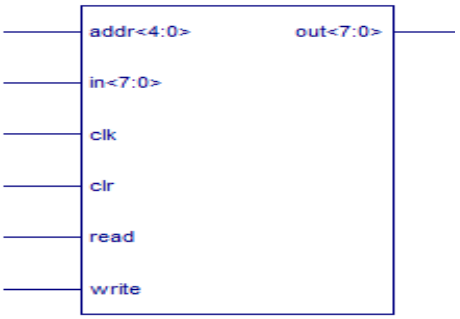

Fig.18 : Block diagram of RAM.

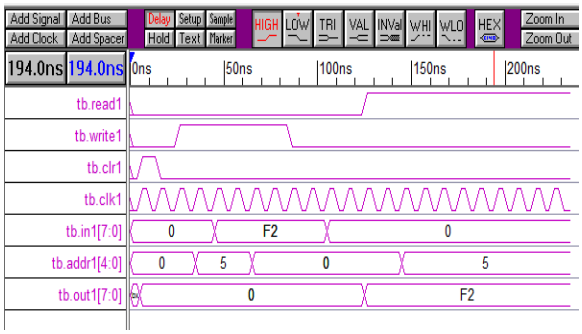

Fig.19 : Timing diagram of RAM.

In this timing diagram as shown in Fig.19 the data F2 is saved in memory location 5 in the RAM and after some instance the data is read from this location.

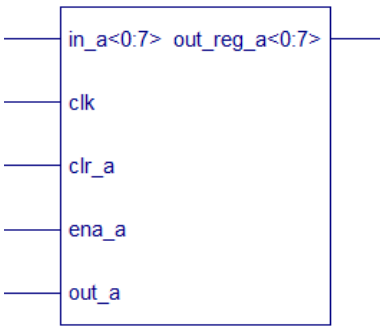

Fig. 20 : Block diagram of register A.

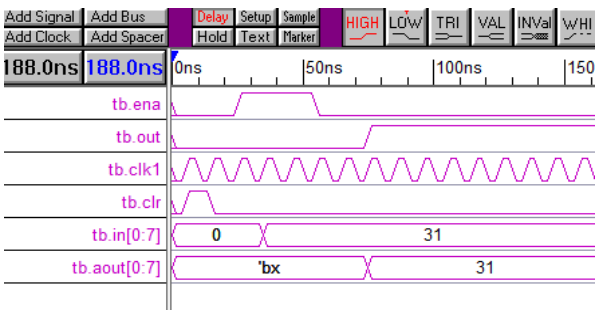

Fig.21 : Timing diagram of register A.

In the timing diagram as shown in Fig.21 a 8bit data 31 is stored in register A and after some time intervals it is read. The operation of register B and C are same as register A.

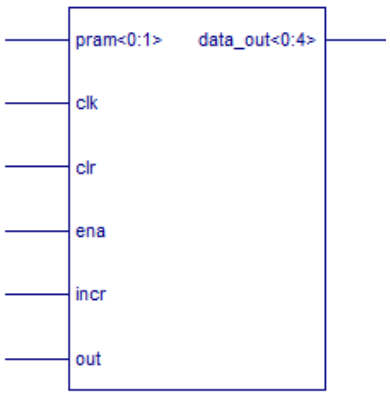

Fig. 22 : Block diagram of Ptr block.

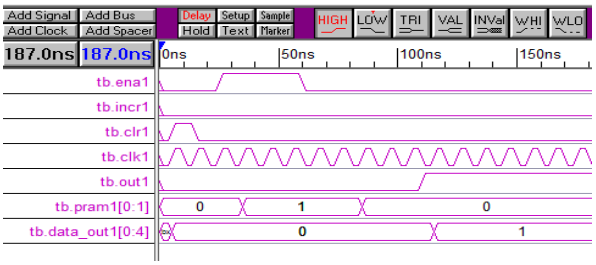

Fig.23 : Timing diagram of Ptr block.

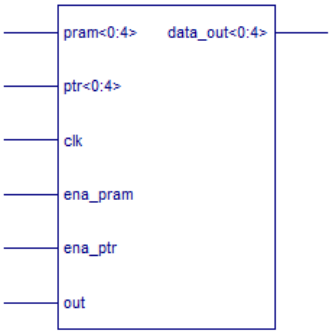

Fig.24 : Block diagram of block P.

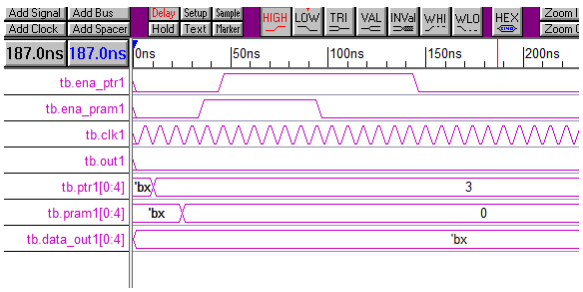

Fig.25 : Timing diagram of block P.

In Fig 23 Ptr gets a data 1 from PRAM block and for it's corresponding it detects the input data bit or error data bit or output data bit. Here it finds that the data is input data bit. In Fig 25 the Block P generates the address in RAM for saving the input bit stream. Page 5 of 6

Fig.26 : Block diagram of Pro_PC.

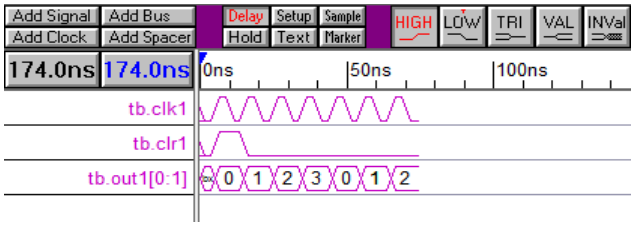

Fig.27 : Timing diagram of Pro_PC.

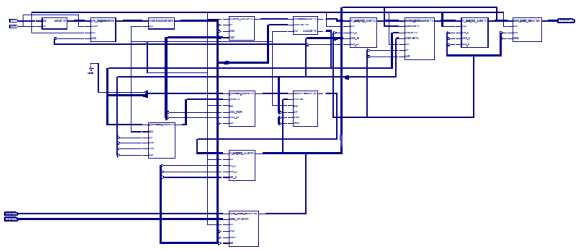

Fig.28 : Chip layout of 2nd order sigma delta modulator.

In Fig.28 2nd order sigma delta modulator chip has four inputs and one output terminal. The four inputs are modulating signal, noise signal, clock input and clear the chip signal. The output will be shown 8bit data of the sigma delta modulated signal. The proposed model implemented upon on XILINX SPARTAN XC2S150 FPGA board. Processor supported by the clock frequency of the processor is 1MHZ ,power consumption, signal bandwidth and CMOS technology on the XC2S150 processor.

The architecture of low-power of second order discrete-time sigma delta modulator has been presented. Due to the lower bandwidth of biomedical signals, sigma delta modulation is feasible. A low power sigma delta can be design by digital circuit that either modulating or recovering circuit with oversampling technique. Using Verilog HDL in designing the modulator, not only the restraints in analogy circuit can be relaxed, the quantization noise can also be reduced better than any other design technique. After all, the analog biomedical signal can be reconstructed from the digital bit stream of modulator output by simple low pass filter.

References Références Referencias

1. Joseph JC and John MB: Introduction to Biomedical Equipment Technology. In: Prentice Hall. Upper Saddle River, 2001.
2. Guessab S, Benabes P and Kielbasa R: A passive delta-sigma modulator for low-power applications.IEEE Circuits and Systems 2004; 3: 295-298
3. Leung SW and Zhang YT: Digitization of electrocardiogram (ECG) signals using delta-sigma modulation. IEEE Engineering in Medicine and Biology Society 1998; 4: 1964 -1966.
4. Ho-Yin Lee, Chen-Ming Hsu, Sheng-Chia Huang, Yi-Wei Shih, Ching-Hsing Luo : Biomedical Engineering Applications, Basis and Communications Vol 17 no. 4 August 2005.
5. Samid L, Manoli Y: Micro Power Continuous-Time Sigma Delta Modulator. Conference on European Solid-State Circuits 2003; 165-168
6. Norsworthy SR, Schreier R, and Temes GC: Delta-sigma converters:/ theory, design and simulation. In: IEEE Press, New York, 1997; 223-234.
7. Fujisaka H, Kurata R, Sakamoto M, Morisue M: Bit-stream signal processing and its application to communication systems. IEE Circuits, Devices and Systems 2002; 149: 159-166.
8. Razavi B:Design of analog CMOS integrated circuit. In: McGraw-Hill, New York, 2001.
9. Thompson H, Hufford M, Evans W and Naviasky E: A low-voltage low-power sigma-delta modulator with improved performance in overload condition. IEEE Custom Integrated Circuits Conference, 2004; 519 - 522.

This page is intentionally left blank