Global Journal of researches in engineering
Electrical and Electronics engineering
Volume 11 Issue 7 Version 1.0 December 2011
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

# Electrical Characteristics Of Trigate Finfet

By M. Zakir Hossain, Md.Alamgir Hossain, Md.Saiful Islam, Md. Mijanur Rahman, Mahfuzul Haque Chowdhury
*Dhaka University of Engineering & Technology*

*Abstract* - FinFET devices are comprehensively investigated owing to the projection for application in the CMOS integrated circuits fabrication. Deducing MOSFET size have great influence on electrostatic characteristic.The indiscriminate variations of the characteristics lead to a divergence effect which is imperative from the point of view of design and manufacture. We have considered only n-channel devices. The behaviors of hole mobility of multigate devices is of course of great importance [1-2]. Electron mobility of n-channel FinFET has simulated with respect to effective electric field. Mobility degradation has been observed with thinner silicon film, at higher electric field, which can be attributed to "volume inversion" in FinFET. In this paper, different types of electrical characteristics have been simulated for different operating regions and different channel lengths and also for different oxide thickness. The considerations are illustrated with measurement data of a series of devices and with distributions of the parameters extracted from these data. The analytical expressions in this work can be useful tool in device design and optimization.

*Keywords : FinFET, MOSFET, mobility, electrical characteristics.*

*GJRE-F Classification : FOR Code: 090604*

*Strictly as per the compliance and regulations of :*

© 2011 M. Zakir Hossain, Md.Alamgir Hossain, Md.Saiful Islam, Md. Mijanur Rahman, Mahfuzul Haque Chowdhury. This is a research/review paper, distributed under the terms of the Creative Commons Attribution-Noncommercial 3.0 Unported License http://creativecommons.org/licenses/by-nc/3.0/), permitting all non commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

# Electrical Characteristics Of Trigate Finfet

M. Zakir Hossain[α], Md.Alamgir Hossain[Ω], Md.Saiful Islam[β], Md. Mijanur Rahman[ψ], Mahfuzul Haque Chowdhury[¥]

*Abstract -* FinFET devices are comprehensively investigated owing to the projection for application in the CMOS integrated circuits fabrication. Deducing MOSFET size have great influence on electrostatic characteristic.The indiscriminate variations of the characteristics lead to a divergence effect which is imperative from the point of view of design and manufacture. We have considered only n-channel devices. The behaviors of hole mobility of multigate devices is of course of great importance [1-2]. Electron mobility of n-channel FinFET has simulated with respect to effective electric field. Mobility degradation has been observed with thinner silicon film, at higher electric field, which can be attributed to "volume inversion" in FinFET. In this paper, different types of electrical characteristics have been simulated for different operating regions and different channel lengths and also for different oxide thickness. The considerations are illustrated with measurement data of a series of devices and with distributions of the parameters extracted from these data. The analytical expressions in this work can be useful tool in device design and optimization

*Keywords : FinFET, MOSFET, mobility, electrical characteristics.*

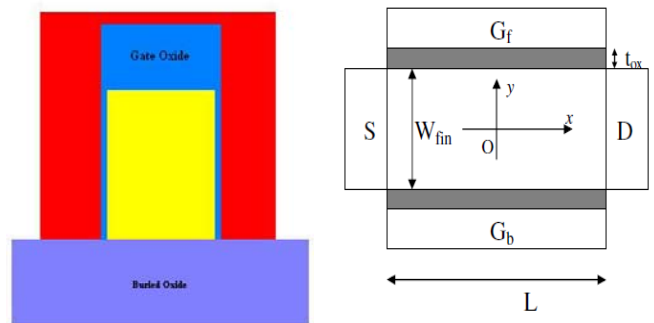
## I. Introduction

The continuing scaling of CMOS (Complementary Metal-Oxide-Semiconductor) technology requires noteworthy innovations in different fields, from short channel effect restraint to carrier transport improvement [3-7].As devices get smaller further and further,the problem with conventional MOSFETs are increasing. We are facing severel problem such as threshold voltage(VT)rolloff ,drain induced barrier lowering (DIBL), increasing leakage current,mobility degradation and so on . To reduce these effect several MOSFET has been introduced such as double gate,FinFET,Trigate,Fourgate,All around gate and etc.We will discuss here the eletrostatic characteristic of FinFET such as current – voltage, effective mobility variation with effective electric field. The distinguishing characteristic of FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the gate of the device. Considering the gate length as the effective channel length. It is very important to know the characteristics of MOSFET to work properly from this aspect we tried to discuss the qualitative feature of FinFET characteristics.

*Author α : Assistant professor of DUET. Dhaka University of Engineering & Technology. E-mail α: mzakir99@gmail.com.*
*Author Ω : Lecturer of Eastern University. Dhaka University of Engineering & Technology. E-mail Ω : alamgir_duet@hotmail.com*
*Author ψ¥β : Dhaka University of Engineering & Technology.*
*Ph β - 08801718871213. E-mail β : saifful69@gmail.com*
*Mobile ψ :+88-01724217996, E-mail ψ : mijan.duet@yahoo.com*
*E-mail ¥ : tmahfuz14@gmail.com*

## II. Theory

All the MOSFET characteristics are expressed as the functions of surface potential at the source and drain ends. In the threshold voltage approach separate solutions are available for different regions of operation (Fig. 1).




a) Cross section area of FinFET. b)Top view of FinFET .

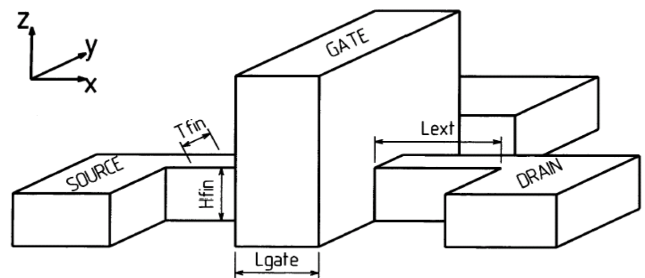



Fig. 1. Schematic of a FinFET structure.

*Fig.1 :* Device structure used in this study .(FinFET consists of a vertical Si fin controlled by self_aligned double gate)

### *a) Linear Region*

It is the region in which $I_{ds}$ , increases linearly with $v_{ds}$ , for a given $v_g > v_t$ . To a first approximation, $I_{ds}$ , in the linear region is given by [8]

$$I_{ds} = 2\,\mu C_{ox}\frac{W}{L}\left(v_g - v_t - \frac{v_{ds}}{2}\right)v_{ds} \quad \text{----------------(A)}$$



© 2011 Global Journals Inc. (US)

Global Journal of Researches in Engineering ( F ) Volume XI Issue VII Version I December 2011



where $\mu$ is the effective mobility in the channel (inversion) region, **Cox** is the oxide capacitance per unit area, W is effective channel width,L is the effective channel length and $v_t$ is threshold voltage.

*b) Saturation Region*

In this region $I_{ds}$ no longer increases as $v_{ds}$ increases. Once more to a first rough calculation, $I_{ds}$ in the saturation region is given by [9]

$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{\left(v_g - \mathrm{v_t}\right)^2}{2\mathrm{m}} \quad \text{-------------------------(B)}$$

Where, $m = 1 + \frac{3t_{ox}}{X_d}$ ----------------------------------(C)

$X_d$ is the depletion layer thickness and $t_{ox}$ is the oxide thickness .

*c) Cut-Off Region*

This is the region where $v_g < v_t$. so that no channel subsist between the source and drain, In fact for $v_g < v_t$, drain current follows an exponential decompose is referred to subthreshold current. The low electron concentration results in low electric field along the channel and as a result the subthreshold current is primarily owing to difusion of carriers. The current in subthreshold region is approximated as [8]

$$I_{ds} = \mu \frac{W}{L} k T n_i t_{si} e^{\frac{q(v_g - \Delta\phi)}{kT}} \left(1 - e^{-\frac{qv_{ds}}{kT}}\right) \quad \text{-----(D)}$$

$\Delta\varphi$ is the work function difference between the gate electrode and the almost intrinsic silicon body.

The FinFET characteristics shown in Figures 2 is often called output characteristics while those shown in Figure 3 and 4 are called transfer characteristics.The threshold Voltage, $V_t$ for FinFET is given as [10]:

$$V_{th} = \phi + n \frac{kT}{q} \ln \left( \frac{2 C_{ox} kT}{q^2 n_i t_{si}} \right) + \frac{h^2 \pi^2}{2 m_{ds} W_{si}^2}$$

The applied Effective electric field, $E_{eff}$ is defined as[11]

$$E_{eff} = \frac{1}{2} \frac{q}{\varepsilon} \left( \frac{N_{inv}}{2} + N_{sub} \times t_{si} \right) \quad \text{--------------------(E)}$$

The mobility is resolute by numerous scattering mechanisms through which the carriers exchange momentum with the semiconductor. the scattering mechanisms are owed to the imperfections of the semiconductor crystal, namely lattice vibrations, ionized impurity atoms, and interface related imperfections, such as surface roughness and interface trapped charges.The mobility in the inversion channel has long been a subject of powerful examination [12].

In the scrupulous case of the MOSFET, three mechanisms combine to determine the effective mobility, namely

Coulomb scattering[13],

$$\mu_{col} = \mu_0^{ph} \left(1 + \frac{E_{eff}}{E_c^{col}}\right)^{v^{col}}$$

phonon scattering[13],

$$\mu_{ph} = \frac{\mu_0^{ph}}{\left(1 + \frac{E_{eff}}{E_c^{ph}}\right)^{v^{ph}}}$$

and surface roughness scattering[14],

$$\mu_{sr} = \mu_0^{sr} \left(\frac{E_{eff}}{E_{effo}}\right)^{\gamma}$$

These three factors that contribute to the total mobility can be combined using Matthiesen's rule [11g17], which states that

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{col}} + \frac{1}{\mu_{sr}} \quad \text{--------------------------------}(F)$$

In equation (F), $\mu_{eff}$ is the total mobility and the factors in the right-hand side of (F) represent the phenomena contributing to mobility. Figure 5 shows the dependence of the inversion layer mobility on the effective electric field .

## III. Results

Most important Features of FinFET are:

1. Ultra thin Si fin for suppression of short channel effects.
2. Raised source/drain to reduce parasitic resistance and improve currrent drive.
3. Symmetric gates yield great performance, but can built asymmetric gates that target VT.
4. FinFETs are designed to use multiple fins to achieve larger channel widths.Source/Drain pads connect the fins in parallel. As the number of fins is increased ,the current through the device increases.For eg: A 5 fin device 5 times more current than single fin device.
5. The main advantage of the FinFET is the ability to drastically reduce the short channel effect. In spite of his doublegate structure, the FinFET is closed to its root, the conventional MOSFET in layout and fabrication.

© 2011 Global Journals Inc. (US)

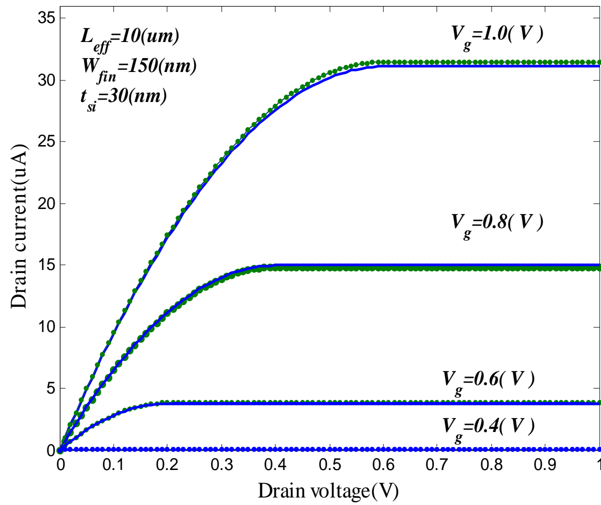



*Fig. 2 :* show the output characteristics of FinFET of Lch=10µm, Wfin=150nm, tsi= 30nm for various gate voltage. Symbols are for experimental data and solid line for simulation result of this work.

Figure 2 Indicate that drain current increase with increase in drain voltage this condition is true upto pinch off voltage then there is no effect of drain voltage over drain current.

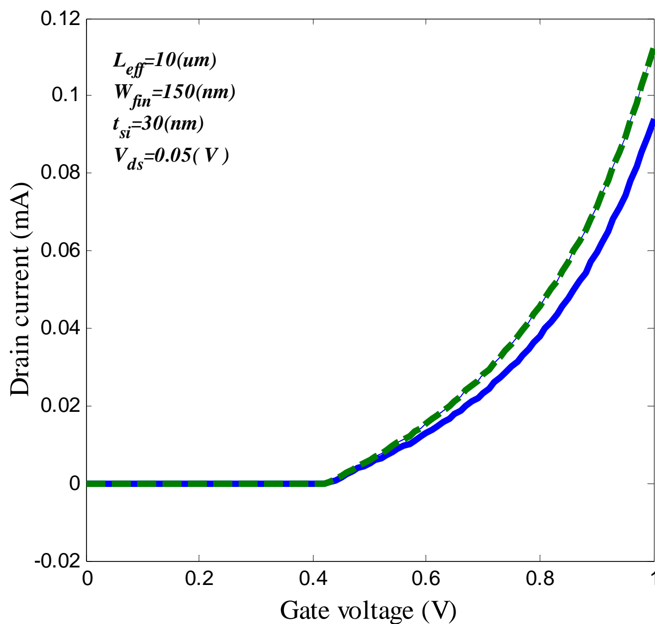



*Fig.3 :* Transfer characteristics of FinFET of Lch=10µm, Wfin=150nm and tsi= 30nm.Desh line for the experimental data and solid line for simulation result of this work.

Figure 3 shows that there is no current flowing upto threshold volteage but after this voltage, current start increasing linearly.This is ideal condition. In pratical situation current flow before threshold volteage reaching.

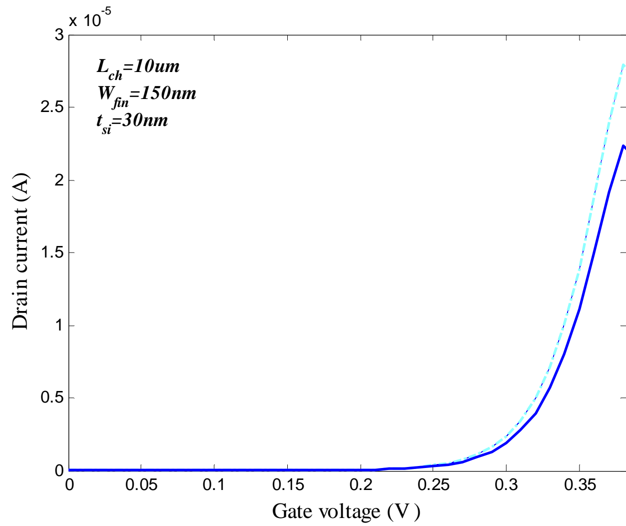



*Fig.4 :* Subthreshold current of n-Channel FinFET of Lch=10µm Wfin=150nm, tsi= 30nm. Desh line for the experimental data and solid line for simulation result of this work.

This figure indicate the Subthreshold current of n- Channel FinFET flowing though threshold volteage limit do not cross.

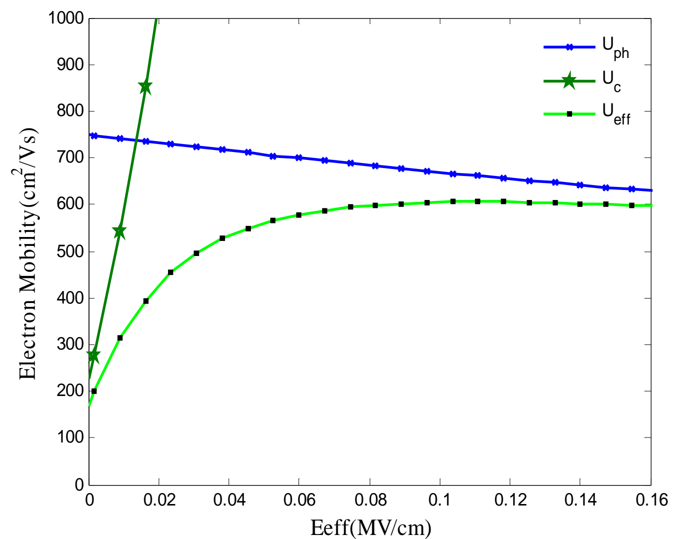



*Fig.5 :* Effective mobilities versus effective field for 10µm n-channel FinFET and $t_{si}$ =30nm.

Figure 5 Indicata that The two components that contribute to the effective mobility degradation. Coulomb scattering ($\mu_{col}$) at low field rise sharply where phonon scattering( $\mu_{ph}$ ) at high field fall gradually.For $\mu_{col}$ , effective mobility ($\mu_{eff}$) rise at low value of $E_{eff}$ but after certain value of $E_{eff}$ , *it* goes straightly due to phonon scattering.



© 2011 Global Journals Inc. (US)

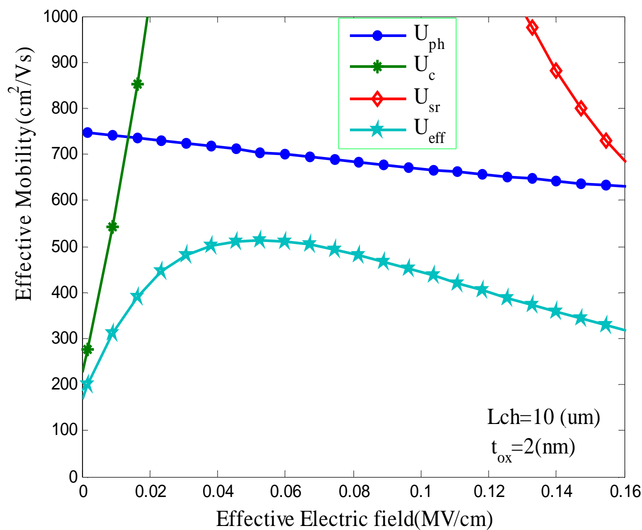



*Fig.6 :* Inversion layer due to effective mobility in the different scattering mechanisms with respect to $E_{eff}$

Fig.6. Indicata that the three components that contribute to the effective mobility degradation. In this figure surface roughness scattering ($\mu_{sr}$) taken into account it fall swiftly as $E_{eff}$ is very high.For $\mu_{sr}$ effective mobility start going down where in previous figure it was straight line.

Coulomb scattering from ionized impurities as well as charged defects near and at the interface Coulomb scattering is more important for low electric fields, becoming less effective for higher fields due to carrier screening.

Phonon scattering is caused by the interaction of carriers with lattice vibrations. Increasing temperatures make the carrier-phonon interaction more intense, thus decreasing the mobility component due to phonon scattering.

Surface roughness scattering from deviations of the Si- SiO2 interface from an ideal flat plane which displays a strong dependence on the effective field. Strong fields pull carriers toward the surface, making surface roughness the dominant scattering contributing to mobility degradation with strong fields.

At room temperature (300 K): For light inversion, Coulomb and phonon scattering dominate. For heavy inversion, surface roughness and phonon scattering dominate.

Major compensation of FinFET.

1. Having excellent control of short channel effects in submicron regime and making transistors still scalable. Due to this reason, the small- length transistor can have a larger intrinsic gain compared to the bulk counterpart.
2. Much Lower off-state current compared to bulk counterpart.
3. Promising matching behavior.

## IV. Conclusion

In this paper presented electrical charecteristics of trigate FinFET from various aspect. FinFET circuits can achieve lower functional voltage supply and lower optimal energy consumption compared to CMOS circuits. In addition, FinFET has better immunity to soft error in sub-threshold region. Trigate FinFET has been projected as a gifted alternative for bulk CMOS technology to continue the technology scaling. The imulation result of this work for n-channel FinFETs are cope with available experimental and/or simulation data.The analytical expressions in this work can be useful tool in device design and optimization such as CVcharacteristic, dopping profile etc.

## References Références Referencias


1. Z. Ren, S. Hegde, B. Doris, P. Oldiges, T. Kanarsky, O. Dokumaci, R. Roy, M. Leong, E. C. Jones, and H. P. Wong: An experimental study on transport issues and electrostatics of ultrathin body SOI pMOSFETs, IEEE Electron Device Lett. 23, 609 (2002).
2. X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu: Sub 50-nm FinFET: PMOS. IEDM Tech. Digest, 67 (1999).
3. International Technology Roadmap for Semiconductors. 2006 Edition
4. S.Cristoloveanu and S.S.Li: Electrical Characterization of Silicon-on- Insulator Materials and Devices (Kluwer, Boston, 1995).
5. G. C. Celler and S. Cristoloveanu: Frontiers of silicon-on-insulator. J. Appl. Phys. 93, 4955 (2003).
6. J.P.Colinge: Silicon-On-Insulator Technology: Materials to VLSI (Kluwer, Boston, 1991).
7. W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, M. V. Fischetti: Silicon CMOS devices beyond scaling. IBM J. Res. & Dev. 50, 361 (2006).
8. Y. Taur, X. Liang, W. Wang, and H. Lu, “A continuous, analytic drain-current model for DG MOSFETs”, IEEE Trans. on Electron Devices letters, vol.25, no.2, Feb.. 2004.
9. Z. Zhang, “Integration of silicide nanowires as Schottky barrier source/drain in FinFETs”, Ph.D Thesis, Royal Institute of Technology (KTH), Stockholm, Sweden, 2008.
10. J. P. Colings, “FinFETs and Other Multi-Gate Transistors,” ISBN 978-0-387-71751-7.
11. Y. Xu, L. Chen, L. Zhang, W. Zhou and F. He, “Study on Electron Mobility in Nanoscale DG MOSFETs with Symmetric, Asymmetric and Independent Operation Modes”, IEEE International Nano Electorics Conference 2010 (INEC 2010).




© 2011 Global Journals Inc. (US)

12. J. R. Schrieffer, “Effective carrier mobility in surface-space charge layers,” *Phys. Rev.*, vol. 97, no. 3, pp. 641-646, Feb. 1955.
13. J. song, Y. Yaun, B. Yu, W. Xiong and Y. Taur, “Compact modeling of experimental n- and p-channel FinFETs”, IEEE Trans. on Electron Devices, vol.57, no.6, June. 2010.
14. S. Reggiani, E. Gnani, A. Gnudi, M. Rudan and G. Baccarani, “Low-Field Electron Mobility Model for Ultrathin-Body SOI and Double-Gate MOSFETs With Extremely Small Silicon Thicknesses”, IEEE Trans. On Electron Devices, vol. 54, no.9, September 2007.

© 2011 Global Journals Inc. (US)

This page is intentionally left blank

© 2011 Global Journals Inc. (US)