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Low Power On-Chip Amplifier For CCD Array

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Abstract- The field of Analog VLSI design is an essential part of any electronics system because of our real world is analog, In this paper low power amplifier is presented for CCD array[1] .CCD are used to capture the images modern digital cameras and high resolution cameras consists of CCD array but all the performance of the CCD array is depends on the performance of On-Chip amplifier which is placed at the end of the array in this paper single and two stage amplifier are simulated and the result is presented for the power and bandwidth by varying the sizes of the different transistors all the results are verified by using the Tanner tool (version 7.1) [11]there are number of analysis presented by the researchers in the literature to improve the power dissipation but most of the structure are compromise sometimes with the area or sometimes with the bandwidth here we have achieve the lesser power dissipation but with the handsome value of bandwidth is also maintained to support this claim the detailed results are presented in the result section.

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Low Power On-Chip Amplifier For CCD Array

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Abstract : The field of Analog VLSI design is an essential part of any electronics system because of our real world is analog, In this paper low power amplifier is presented for CCD array[1] .CCD are used to capture the images modern digital cameras and high resolution cameras consists of CCD array but all the performance of the CCD array is depends on the performance of On-Chip amplifier which is placed at the end of the array in this paper single and two stage amplifier are simulated and the result is presented for the power and bandwidth by varying the sizes of the different transistors all the results are verified by using the Tanner tool (version 7.1) [11]there are number of analysis presented by the researchers in the literature to improve the power dissipation but most of the structure are compromise sometimes with the area or sometimes with the bandwidth here we have achieve the lesser power dissipation but with the handsome value of bandwidth is also maintained to support this claim the detailed results are presented in the result section.

I. Introduction

Charge Coupled Devices (CCDs) were invented in the 1970s and originally found application as memory devices Charge Coupled Devices (CCD) have many applications, but the most important is in imaging [3]. The basic operation of the sensor is to convert light into electrons. When light is Incident on the active area of the image sensor it interacts with the atoms that make up the silicon crystal. The energy transmitted by the light (photons) is used to enable an electron to escape from the tight control of one atom to roam more freely about the device as a "conduction"electron, leaving behind an atom shy of one electron. Modern CCD has two types of architecture:

1. Full-Frame (FF)
2. Frame-Transfer (FT)

FF CCDs have the simplest architecture and are the easiest to fabricate and operate. They consist of a parallel CCD shift register, a serial CCD shift register and a signal sensing output amplifier. Images are optically projected onto the parallel array which acts as the image plane the architecture is shown in the fig. 1

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FT CCDs are very much like FF architectures. The difference is that a separate and identical parallel register, called a storage array, is added which is not light sensitive. The idea is to shift a captured scene from the photosensitive, or image array, very quickly to the storage array [5]. Readout off chip from the storage register is then performed as described in the FF device previously while the storage array is integrating the next frame. The architecture is shown in the fig. 2

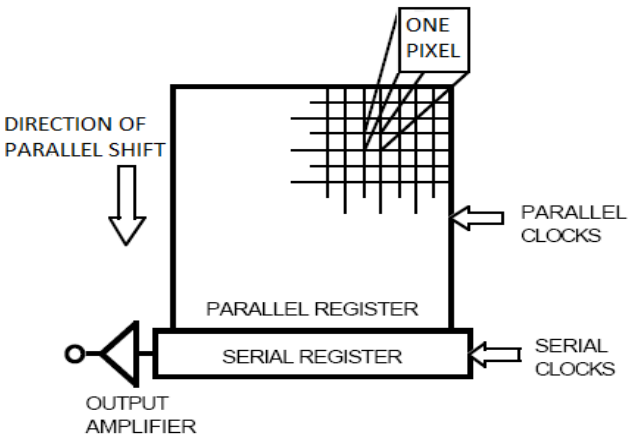

Fig. 1: Full Frame architecture

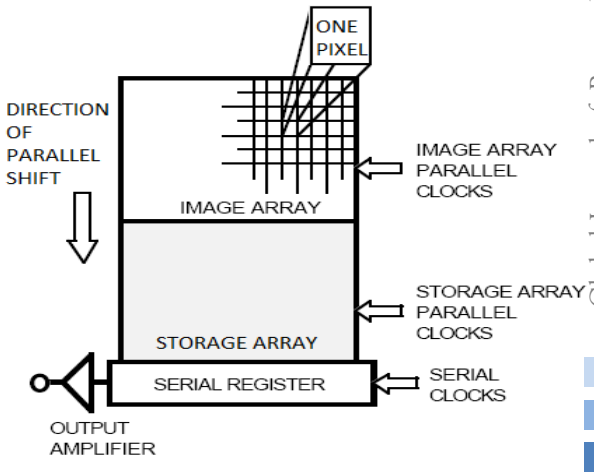

Fig. 2: Frame transfer architecture

Both of the above architecture are widely used but the performance of both the architecture are depends on the type and the quality of the On-chip (output) amplifier which is fabricated at the last stage of the structure as shown in the fig above.

II. Architecture of On-Chip Amplifier

Output amplifier has also two type of the architecture

1. Single stage amplifier
2. Two stage amplifier

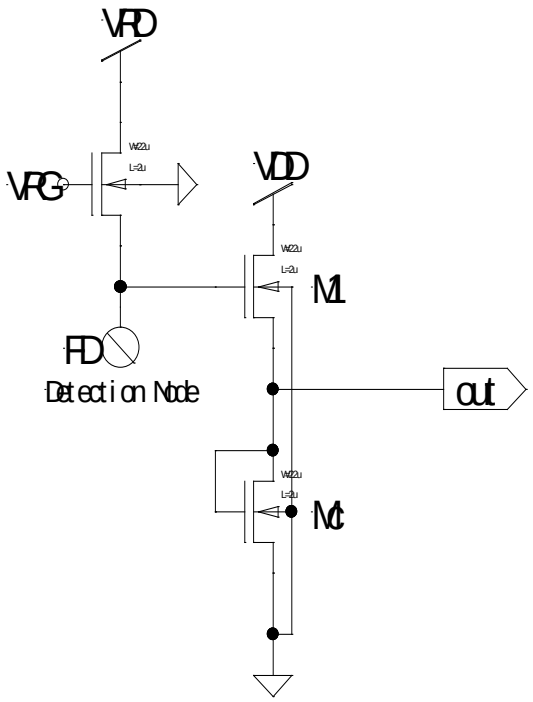

Fig. 3: Single Stage CCD On-Chip amplifier

The single stage amplifier consists of source follower M1 and load transistor Mc for biasing. The reset FET is connected to the detection node and consists of floating diffusion [6, 7] and the gate of M1. In the ON state it resets the detection node to a reference voltage (VRD) and in the OFF state the floating can receives the next charge packet. The voltage source between the gate and source of the current sink Transistor Mc determines the bias current of the first stage and can be used as a signal injection point to measure the ratio between total capacitance and the effective sense capacitance and the bandwidth in the off state. The Two stage amplifier further improves the character tics of the amplifier and gives the better result which is shown in the result section of the paper and the architecture of two stages is shown two stage amplifier also improves the sensitivity of the amplifier and this also reduces the noise level of the overall CCD.

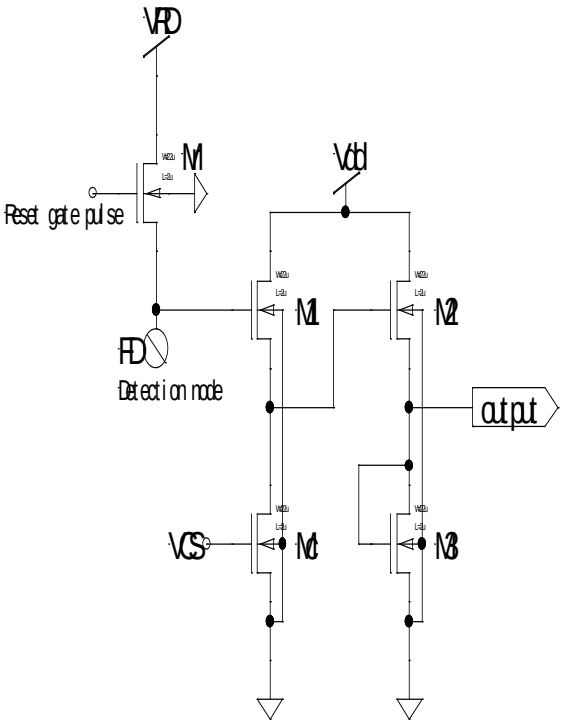

Fig. 4: Two Stage CCD On-Chip amplifier

III. Optimization

For optimization of the on-chip amplifier Length and Width of the individual transistor are varied and the various optimization results are obtained. The effect of increase and decrease of Length and Width of the transistor is given as

To achieve maximum gain:

Transistor 'M1': -The gain can be maximized by increasing the width of this transistor as this increases the difference in the output voltage amplitude.

Transistor 'MC': -The gain can be maximized by decreasing the width of this transistor as this increases the difference in the output voltage amplitude.

Transistor 'M2': -The gain can be maximized by increasing the width of this transistor as this increases the difference in the output voltage amplitude.

Transistor 'M3': -The gain can be maximized by decreasing the width of this transistor as this increases the difference in the output voltage amplitude.

To achieve maximum bandwidth:

Transistor 'M1': - The bandwidth of the circuit can be increased by increasing the width of this transistor as the increase in width increases the transconductance which helps in increasing the bandwidth as the impedance decreases.
Transistor 'MC': - The bandwidth of the circuit can be increased by increasing the width of this transistor as the increase in width increases the transconductance which helps in increasing the bandwidth as the impedance decreases.
Transistor 'M2': - The bandwidth of the circuit can be increased by increasing the width parameter of this transistor. So bandwidth can be increased by changing this parameter.
Transistor 'M3': - The bandwidth of the circuit can be increased by increasing the width of this transistor as the increase in width increases the Tran conductance which helps in increasing the bandwidth as the impedance decreases, although the change desired is not that large.

To achieve minimum power dissipation:

Transistor 'M1': - The power dissipation of the circuit can be reduced by reducing the width of this transistor as the current flowing into this transistor reduces with the reduction in the width while power dissipation can be reduced by increasing the length because increase in length reduces transconductance which in turn reduces the amount of current flowing into the transistor.
Transistor 'MC': - The power dissipation of the circuit can be reduced by reducing the width of this transistor as the current flowing into this transistor reduces with the reduction in the width while power dissipation can be reduced by increasing the length because increase in length reduces transconductance which in turn reduces the amount of current flowing into the transistor.
Transistor 'M2': - The power dissipation of the circuit can be reduced by reducing the width of this transistor as the current flowing into this transistor reduces with the reduction in the width.
Transistor 'M3': - The power dissipation of the circuit can be reduced by reducing the width of this transistor as the current flowing into this transistor reduces with the reduction in the width.

IV. Results

Transistor Dimensions (W× L) µm		M2 (W× L) µm	M3 (W× L) µm	Power Dissipation (mW)	Bandwidth BM (MHz)
M1	Mc				
15×25	12×10	20x10	10x25	5.9	302
15×25	12×10	20x10	12x25	5.95	320
15×25	12×10	20x10	15x25	6.0	242
15×25	12×10	20x10	18x25	6.1	207

Table 1: When the width of the transistor M3 varied

Transistor Dimensions (W× L) µm		M2 (W× L) µm	M3 (W× L) µm	Power Dissipation (mW)	Bandwidth BM (MHz)
M1	Mc				
15×25	12×10	20x10	10x25	5.15	69
15×25	12×10	18x10	10x25	5.25	62
15×25	12×10	16x10	10x25	5.2	78
15×25	12×10	14x10	10x25	5.3	70
15×25	12×10	12x10	10x25	5.4	87
15×25	12×10	10x10	10x25	5.7	122
15×25	12×10	8x10	10x25	5.8	148

Table 2 : When the width of the transistor M2 varied

Transistor Dimensions (W× L) µm		M2 (W× L) µm	M3 (W× L) µm	Power Dissipation (mW)	Bandwidth in (MHz)
M1	Mc				
15×25	12×10	20x10	10x5	7.0	580
15×25	12×10	20x10	10x10	6.4	594
15×25	12×10	20x10	10x15	6.1	596
15×25	12×10	20x10	10x18	6.0	365
15×25	12×10	20x10	10x20	5.9	270
15×25	12×10	20x10	10x25	5.7	122
15×25	12×10	20x10	10x30	5.8	109

Table 3: When the Length of the transistor M3 varied

Transistor Dimensions (W× L) µm		M2 (W× L) µm	M3 (W× L) µm	Power Dissipation (mW)	Bandwidth in (MHz)
M1	Mc				
15×25	12×10	20x5	10x15	6.4	150
15×25	12×10	20x10	10x15	6.1	490
15×25	12×10	20x15	10x15	5.9	550
15×25	12×10	20x18	10x15	5.8	570
15×25	12×10	20x20	10x15	5.8	326
15×25	12×10	20x25	10x15	5.75	380

Table 4: When the Length of the transistor M2 varied

The results of the above table are taken from the Tanner T-spice tool by using the 2.0 Mosis model file for the enhancement MOSFET transistor. The power dissipation and the bandwidth are directly, measures from the waveform editor in the Tanner EDA tool.

V. Conclusion and Future Scope

It is observed from the result that in case of single stage On-Chip amplifier minimum power dissipation and maximum bandwidth is achieved when the Width of the M1 transistor is 18µm and the Length of the M1 transistor is 25µm meter and the Width of the Mc transistor is 10µmr and the Length of the Mc transistor is 16µm. In this case power dissipation is 4.3 milli-watts and the gain of the amplifier is 0.82 and bandwidth is 617MHz. In case of two stage amplifier maximum bandwidth is achieved when dimension of transistor is as M1(15µmx25µm), M2(20µmx10µm), M3(10µmx15µm) & Mc(12µmx10µm) and for minimum power dissipation the dimension of all the transistor should be M1(15µmx25µm), M2(20µmx10µm), M3(10µmx25µm) & Mc(12µmx10µm). The whole design simulated using MOSIS/Orbit 2.0µm process by using Tanner tool. In this thesis Analog simulation is done by using the Tanner tool and using the enhancement type MOSFET transistor is used, this thesis can be further extended for the depletion type MOSFET because in depletion type MOSFET noise level will get further reduce and the other thing which can be improved in future is, semiconductor and environmental noise effect which is not consider in this current thesis.

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