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Power Optimization in 3 Bit Pipelined ADC Structure

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POWER OPTIMIZATION IN 3 BIT PIPELINED ADC STRUCTURE

Strictly as per the compliance and regulations of :

Power Optimization in 3 Bit Pipelined ADC Structure

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I. Introduction

The Pipelined analog-to-digital converter (ADC) is an attractive architecture for high-speed data conversion in CMOS technologies. However, its linearity is limited due to its reliance on precise analog component matching [1] and signal processing..shown in fig. 1.

With the continued growth of mixed signal VLSIsystems, supporting diverse integrated functionalities on a chip, the need for small sized, low-power and high-speed ADCs (analog to digital converters) using CMOS process has increased. As CMOS technologyscales down size of transistors and supply voltage (VDD) levels are reduced to decrease the effective area of the chip and power dissipation. For high-speed applications, flash ADCs generally achieve the highest conversion rate. However, formore than 6-bits resolution, flash converters sufferfrom the exponential growth of die area and powerdissipation. Pipelined ADCs feature high throughput while dissipating less power compared to flash ADCs. In the context of current-mode design similar argument is valid. As an effort in the direction of current-mode mixed-signal design two current-mode.CMOS pipelined ADCs, one aimed for high speed applications and other aimed for high resolution applications in 0.18µm CMOS process are presented in this paper.

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Pipelined Structure

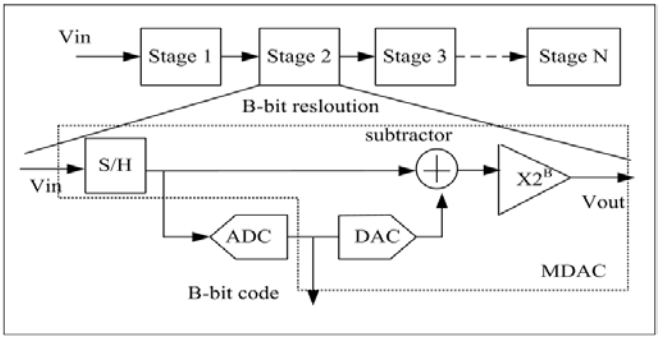

Fig. 1

A main advantage of the pipeline converter is its high throughput. After aninitial delay of *N* clock cycles, one conversion will be completed per clock cycle. Whilethe residue of the first stage is being operated on by the second stage, the first stage is free to operate on Samples.

II. Related Work

For Better Gain and Reliability Cascading Logic Of Op-amp Implemented in Below 3 bit Pipeline ADC Structure which Designing in Microwind Software. Analog signal at Op-amp Inverting Input and Output through LED we can Measure.

Circuit Diagram

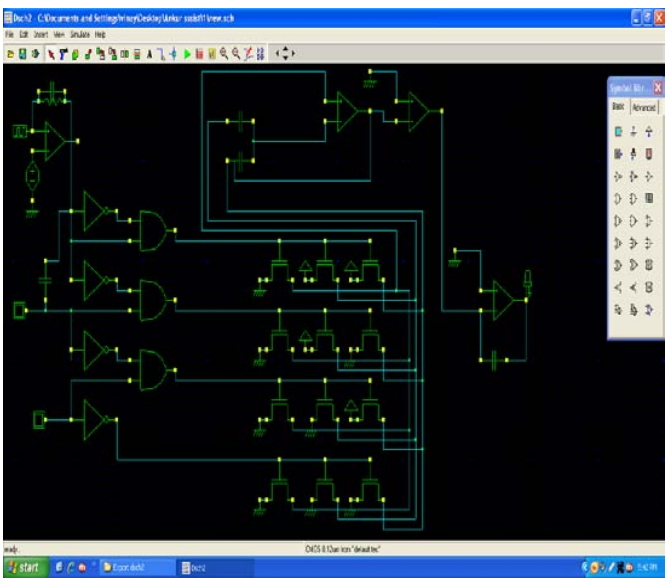

Fig. 2

In Above Design fig.2 Two main Parts can operate whole the operation. First Part is of Switched Capacitor and second is of Cascading Logic.

Circuit Function

When Clock signal and Analog input simulate through the design ,Capacitor charge and discharge depends on their output it pass through the Sample and hold part and 3 Pipeline Stages.Cascading Logic Of opamp gives boost to the output and pass through the LED which reflects Output Square wave .

One interesting aspect of this converter is its dependency on the most significant
stages for accuracy. A slight error in the first stage propagates through the converter and results in a much larger error at the end of the conversion. Each succeeding stage requires less accuracy than the one before, so special care must be taken when considering the first several stages.

Simulation Result

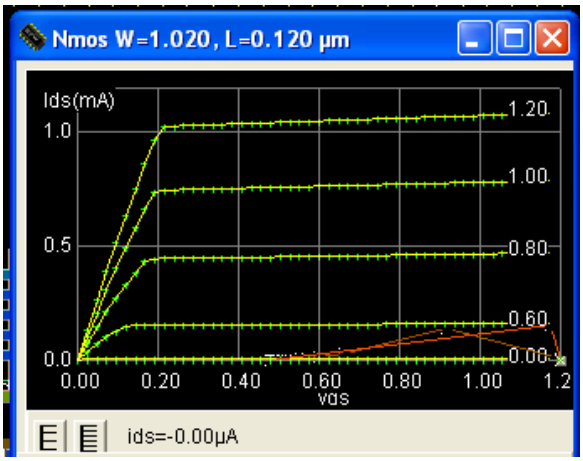

Fig. 3

From Above Result shown in fig. 3 Voltage approximate we get 0.50 Vds and Current 0.20 mA. The oversampling ADC [18-20] is able to achieve much higher resolution than the Nyquist rate converters. This is because digital signal processing techniques are used in place of complex and precise analog components. The accuracy of the converter does not depend on the component matching, precise sample-and-hold circuitry, or trimming, and only a small amount of analog circuitry is required. Switched-capacitor implementations are easily achieved, and, as a result of the high sampling rate, only simplistic anti-aliasing circuitry needs to be used. However, because of the amount of 838 Part IV Mixed-Signal Circuits time required to sample time less.

III. Modified Layout

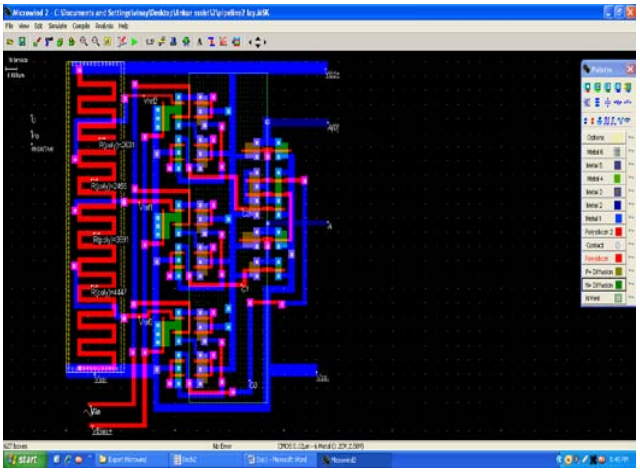

Fig. 4

As Past Results are such not satisfactory ,modified circuit layout designed shown in fig. 4. Just a Cascading Part of the circuit using opamp in past circuit converted to Nmos and Pmos Part. As Operation now Slightly change.

The implementation of the MDAC differential amplifier determines the speed and accuracy of the converter; the first stage of the pipelined ADC is the most critical for the accuracy of the entire ADC. To meet 10-bit accuracy with an MDAC feedback factor of 1/3 the open loop gain of the differential amplifier must be greater than 69.7dB. While open loop gain determines accuracy, the speed of the converter is determined by the speed of the amplifier. A single stage amplifier is typically used to maximize speed but limits gain. Conventionally, cascode architectures are used to produce high-gain single stage amplifiers. However, full cascode stages limit the output signal swing when used at minimum supply voltages. To achieve wide swing and high gain in a single stage a folded cascode architecture may be augmented with an active bootstrapped gain enhancement technique.

IV. Results

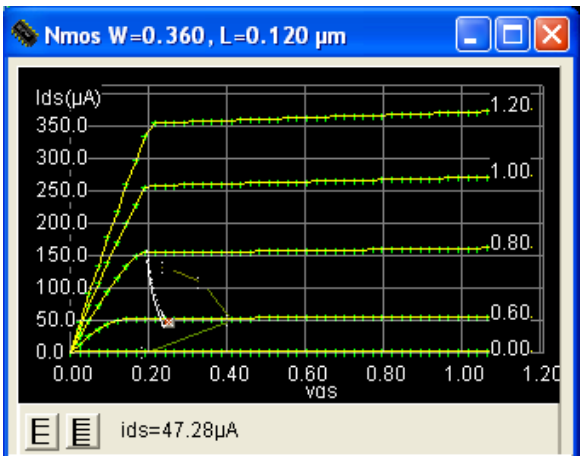

Fig. 5

New Result in fig. 5 Shows approx. half of Vds 0.20 and 150 μA of Current Drawn. So better result we gain when modified layout. The digital code for each pipeline stage is determined by a three level ADC which is implemented with two comparators.

A single MDAC sample cycle consists of an ADC conversion,DAC addition/subtraction, and signal amplification. The amplifier output is based on the DAC output which relies on the ADC code. Thus, the conversion time of the MDAC ADC comparators adds directly to the sampling and settling time of the stage. To minimize the conversion time a positive feedback latched comparator is used. The comparator inputs use switched capacitor sampled signals with *Vre f* driven capacitors to create the comparator trip points as shown in Fig. 5. At the *S*1 transition *Vin+/−* are forced to *Vdd* by the previous stage. The comparator trip points are determined by the capacitor ratio *CA*2/*CA*1 and the voltage levels of the *Vre f* signals. The ADC trip points are become The actual capacitor ratio should be decreased further to meet the maximum *Vtrip* limit while accounting for capacitor mismatches and comparator and MDAC offsets.

VII. Conclusion

A 3-bit ADC converter has been designed and implemented in a 0.60 μm CMOS process for operation at supply voltages below *2 V* . The ADC design uses a fully differential active bootstrapped gain enhancement technique for high gain single stage differential amplifier operation. So We can achieve approx half of the Power consumed in Circuit. This Design Also achieves more power Saving when implemented With different components and Softwares.

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