Global Journal of Researches in Engineering
Electrical and Electronics Engineering
Volume 12 Issue 11 Version 1.0 Year 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

A First Principle's Approach to Study of the Silicon Drift Detector with Embedded JFET: Noise Analysis, Simulations & Analytical Modeling

By Pourus Mehta
Bhabha Atomic Research Centre

Abstract - Proto-type commercial grade Silicon Drift Detectors (SDDs) with on-chip low noise JFETs have been realized using silicon bipolar technology at Bharat Electronics Ltd (BEL), Bangalore. Noise analysis articulating the relationships of various noise sources on the electrical parameters of the fabricated SDD and JFET have been discussed. TCAD device simulations have been performed for the SDD and on-chip JFET for static (dc) and dynamic cases. The static case simulations revealed values of critical dc performance parameters like leakage current, anode capacitance etc. Dynamic simulations meant to study the effect of radiation, revealed the relationship between drift time & drift distance within the detector. Analytical modeling of the I-V characteristics of the SDD has also been performed to predict the leakage current behavior for various other designs fabricated at BEL.

Keywords : *Silicon Drift Detectors, Junction Field Effect Transistors, Technology Computer aided Design & Equivalent Noise Charge.*

GJRE-F Classification : *PACS : 85.30.-z, 85.30.De & 85.30.Tv*

Strictly as per the compliance and regulations of :

A First Principle's Approach to Study of the Silicon Drift Detector with Embedded JFET: Noise Analysis, Simulations & Analytical Modeling

Pourus Mehta

Abstract - Proto-type commercial grade Silicon Drift Detectors (SDDs) with on-chip low noise JFETs have been realized using silicon bipolar technology at Bharat Electronics Ltd (BEL), Bangalore. Noise analysis articulating the relationships of various noise sources on the electrical parameters of the fabricated SDD and JFET have been discussed. TCAD device simulations have been performed for the SDD and on-chip JFET for static (dc) and dynamic cases. The static case simulations revealed values of critical dc performance parameters like leakage current, anode capacitance etc. Dynamic simulations meant to study the effect of radiation, revealed the relationship between drift time & drift distance within the detector. Analytical modeling of the I-V characteristics of the SDD has also been performed to predict the leakage current behavior for various other designs fabricated at BEL.

Keywords : Silicon Drift Detectors, Junction Field Effect Transistors, Technology Computer aided Design & Equivalent Noise Charge.
PACS : 85.30.-z, 85.30.De & 85.30.Tv

I. Introduction

Silicon drift detector (SDD) is a detector based on the principle of lateral charge transport within the bulk of a fully depleted detector, as proposed by Gatti and Rehak (Reference-1). SDDs are fabricated over high resistivity *n*-type substrate with *p-n* junctions on both top and bottom sides of the substrate. PN junctions on the top-side are segmented field shaping cathodes whereas the back-cathode is a uniform *p-n* junction. A reverse bias gradient is applied to the field shaping cathodes, which results in creation of a potential energy distribution in the shape of a "Potential Gutter" with its ultimate electron potential energy minimum at the anode. Electron-hole pairs are created by passage of ionizing radiation and get swept vertically across the parabolic potential along the depth and are focused at the local potential minima. They then get drifted along the lateral drift channel towards the anode. The noteworthy feature of the SDD is that its small output (anode) capacitance is independent of its large detector active area. SDDs are suitable for high resolution (127eV @ 5.9 keV for Mn-Kα line; Ketek Vitus SDD) and high count rate (~$1x10^6$ cps) X-ray spectroscopy applications. These detectors have found wide application in high-energy physics for tracking applications. SDDs have been incorporated in the ALICE detector experiment along the Large Hadron Collider at CERN. SDD's high-resolution capability can be further augmented by integrating the input device of the pre-amplifier (JFET) within the detector so as to avoid stray capacitance and microphonism. The integration of JFET onto the detector also facilitates better matching between detector and transistor capacitances/ impedances. The proto-typing stage fabrication of SDDs at IIT-B has been successfully completed (Ref. 5). Commercial grade SDDs have already been fabricated at BEL and have yielded satisfactory performance (Ref. 8). This paper gives a broad outline on the noise analysis, dc and dynamic TCAD simulations of the SDDs fabricated at BEL. An attempt has been made to model the static current-voltage characteristics of the SDD to predict the electrical behavior for various other kinds of SDDs fabricated at BEL.

II. Detector Design

Fig. 1(b) shows the 2D cross-section of the SDD of circular geometry with a cathode pitch of 120 μm {p+ cathode width (70μm) + Inter-strip gap (50μm)}. An n-type high resistivity (4 kΩ.cm) <111> orientation substrate of 300 μm thickness is employed to fabricate the SDD-JFET composite device. The peak concentration in p+ cathode region is approximated to be $1x10^{18}$ cm^{-3} with a gaussian distribution profile. Similarly, the back junction is also having the same concentration and profile. This version of SDD had an on-chip poly-resistor network for biasing the intermediate p+ strips together with an on-chip JFET for first level amplification [Fig. 1(a)]. This device had 20 p+ cathodes with two guard rings encircling its outer perimeter. The first, fifth, tenth, fifteenth, twentieth, and last p+ strips were individually biased whereas

Author : Bhabha Atomic Research Centre, Electronics Division, MOD Lab, Trombay, Mumbai 400085, India.
E-mails : pdmehta@barc.gov.in, pourus@cern.ch & pourus_m@yahoo.com

intermediate cathodes got biased through an on-chip poly-resistor network. Each poly resistor was designed to present a resistance of 102.4 kΩ (R_S=138.88 kΩ/□). The anode being an annular ring (radius = 50 μm) having area of 7.7 x 10^4 μm^2 which fetched an analytical full depletion anode capacitance of 27 fF for 300 μm thick fully depleted silicon wafer. The total detector active area of the detector was 2.31 x 10^7 μm^2. The embedded lownoise JFET (named as JFET-10) for this SDD design had the smallest channel length (15 μm) possible with BEL process [Fig. 1(c)]. For a designed channel length of 15 μm and the channel width of 172 μm, the analytical Transconductance (g_m) worked out to be 0.247 mS.

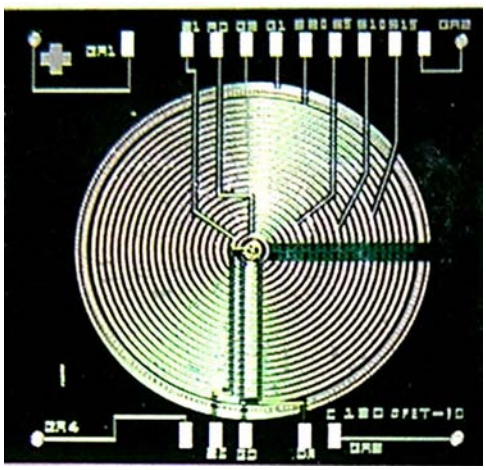

Fig. 1 (a) : Photograph of the completely fabricated SDD with in-built JFET.

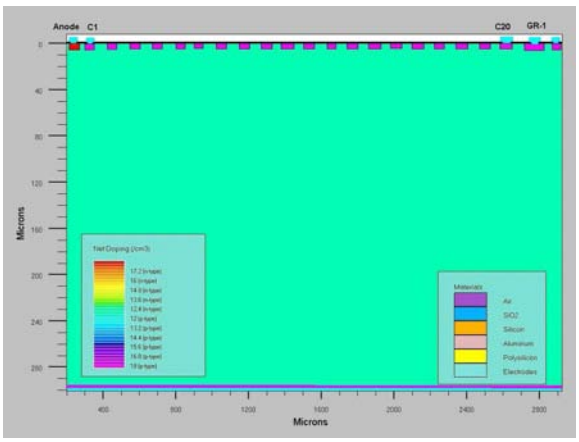

Fig. 1 (b) : 2-dimensional doping contours of the SDD (Pitch=120 μm).

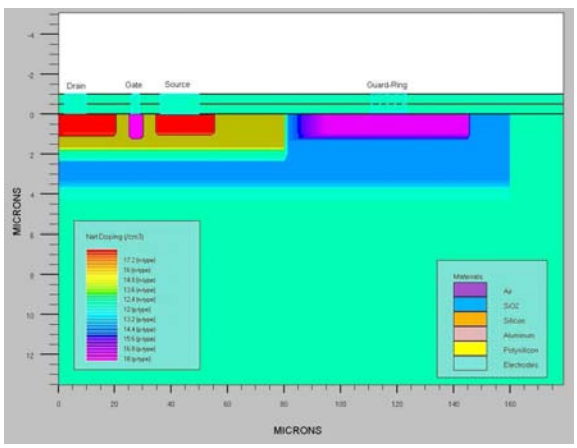

Fig. 1 (c) : 2-dimensional doping contours of the embedded JFET.

III. Noise Analysis

The Equivalent Noise Charge (ENC) has a strong dependence on the optimum shaping time (TM) (Equations 1-5) (Refer Spieler notes). It can be inferred from equations 1-5 that TM should be as small as possible to reduce the components of noise playing a critical role in the SDD & JFET system. It was found that for a particular value of Transconductance g_m and detector leakage current I_D, the optimum shaping time was least for a capacitance mismatch factor (h) of ~1. This means that the detector capacitance and JFET gate capacitance should not only be small but also nearly equal to each other. To prove this argument, a numerical simulation has been performed using values obtained from simulation of the JFET & SDD together. The plot in figure 2 shows the graphical representation of the relationship between optimum shaping time and mismatch factor. Figure 3 shows the mathematical relationship of the ENC on mismatch factor for the SDD-JFET system.

$$T_M = 0.65 \times \frac{1}{2} \times \left(\sqrt{h} + \frac{1}{\sqrt{h}} \right) \times \sqrt[3]{\frac{C_{FET}}{g_m}} \times \sqrt[3]{\frac{C_D}{I_{leak}}}$$

$$\text{Where } h = \frac{C_D}{C_{FET}} \quad \text{(Mismatch Factor)}$$

---- Eq. 1

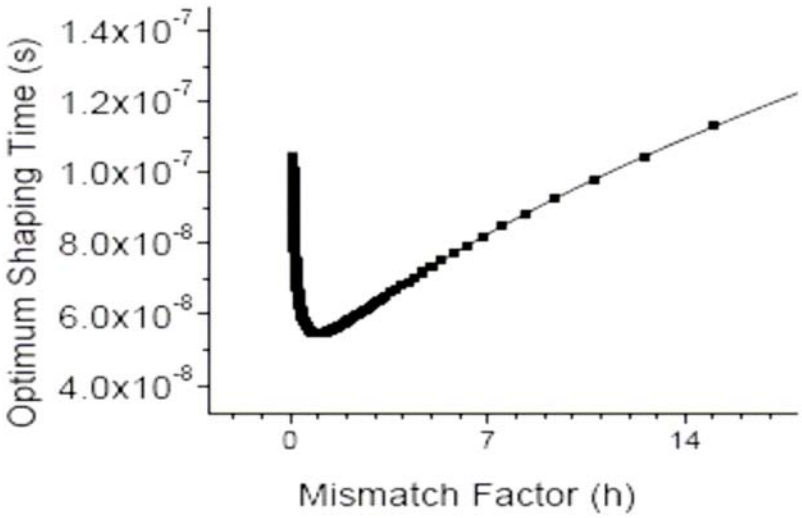

Fig. 2 : Optimum shaping time versus Capacitance mismatch factor.

a) Equivalent Noise Charge for Gate Current Noise (Ig)

As stated earlier the gate current is a source of noise in the JFET and its relationship with ENC is shown in equation 2. From the equation 2 it is also inferred that the gate current should be as small as possible to reduce the ENC_1 component of noise.

$$ENC_1 = \frac{e}{2q}\sqrt{q \times T_M \times I_g} \quad \mathbf{e} = 2.718,\ \mathbf{q} = \text{electron charge}$$

---- Eq. 2

b) Equivalent Noise Charge for Detector Leakage Current Noise (ID)

Similarly, it is seen from equation 3 that the detector leakage current should be minimum for reduction of ENC_2 component.

$$ENC_2 = \frac{e}{2q}\sqrt{q \times T_M \times I_D}$$

--- Eq. 3

c) Equivalent Noise Charge for feedback circuit

The noise due to feedback circuit can be minimized by choosing a very high value of feedback and bias resistors so as to make the effective parallel combination R_P large.

$$ENC_3 = \frac{e}{2q}\sqrt{\frac{2\times K\times T\times T_M}{R_P}}$$ --- Eq. 4

Where $R_P = \frac{R_B \times R_f}{R_B \oplus R_f}$

$R_P = R_B \parallel R_f$

R_B = Bias resistor

R_f = Feedback resistor

d) Equivalent Noise Charge due to JFET drain shot noise

This component can be minimized by having a small value for capacitances together with a high g_m.

$$ENC_4 = \frac{e}{2q}\times(C_D + C_F + C_{GS})\times\sqrt{\frac{4\times K\times T}{3\times T_M \times g_m}}$$ --- Eq. 5

Where C_D = Detector Capacitance

C_f = Feedback capacitor

C_{GS} = JFET gate-source capacitance

e) Net effective Equivalent Noise Charge

$$ENC^2 = ENC_1^2 + ENC_2^2 + ENC_3^2 + ENC_4^2$$

$$ENC = \sqrt{ENC_1^2 + ENC_2^2 + ENC_3^2 + ENC_4^2}$$ ----- Eq. 6

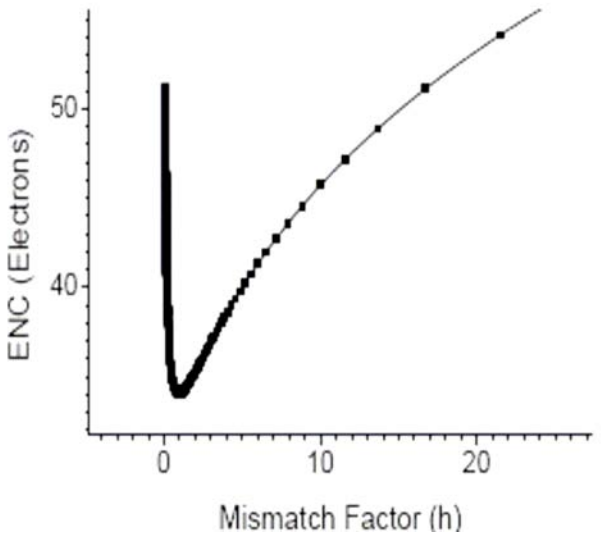

Fig. 3 : Equivalent Noise Charge versus Capacitance mismatch factor.

IV. Device Simulations

Three Dimensional device simulations have been carried out keeping a two fold approach in mind. Firstly, device simulations carried out for the static case (without application of any radiation) on the SDD-JFET composite device system. Secondly, to study the effect of application of incident radiation (X-ray photons; λ = 2 A°) on the performance curves of the SDD.

a) Static Case Simulations (Without application of Incident Radiation)

i. *Silicon Drift Detector*

The 2D cross-section of the SDD-JFET system [Fig. 1(b)] has been used as input to run a static case current voltage simulation. The 2D cross-section in figure 1(b) has been subjected to application of appropriate voltages and suitable boundary conditions were added to ensure that the solution to the poisson & continuity equations would converge. The biases were applied such that the anode was at a zero potential, cathode-1 was given -5 volts potential and cathode-20 at -100 V. The intermediate cathodes got biased through the on-chip poly-resistor network. This peculiar biasing develops a potential distribution resembling a gutter (Ref. 4). The one dimensional potential along the depth is parabolic in nature. This leads to confinement of electrons generated by photo-electric absorption of incident photons. The photoelectrons are first concentrated within the minima along the depth and then drifted along the horizontal channel towards the anode where they ultimately get collected. The above biasing scheme results in an electric field of 370 V/cm. Corresponding to the field strength & an Electron Mobility of 1350 cm^2/ V.s at 300°K, Electron Drift Velocity works out to be 5 × 10^5 cm/s. This implies a detector response time (Drift Time) of around 100 nano seconds for a drift distance of around ~500 µm. Value of resistance of poly-resistor was fixed at 100 kΩ for *W* = 120 *µ*m & L = 80 *µ*m, which corresponds to a total resistor chain current of around 65 *µ*A under these biasing conditions. The simulated detector anode (output) capacitance at full depletion is around 200 femto Farad which is flexible enough to play with and tune with the integrated transistor's capacitance.

Fig. 4 shows the leakage current of the detector as a function of reverse bias applied to cathode C-20 whereas figure 5 gives the C-V characteristics of the simulated SDD structure respectively. As the reverse bias is increased, the depletion region extends as function of $\sqrt{V}$ from both sides of the device. The capacitance decreases to significant low value during initial reverse bias of -5 V when the depletion region from first strip touches the n^+ anode. Further increase in reverse bias continues to deplete the bulk (and reduce the capacitance) till full depletion is reached at -30 V. Beyond this bias anode capacitance saturates to a low value corresponding to a parallel plate capacitor of area that of anode and spacing between the plates being the detector thickness.

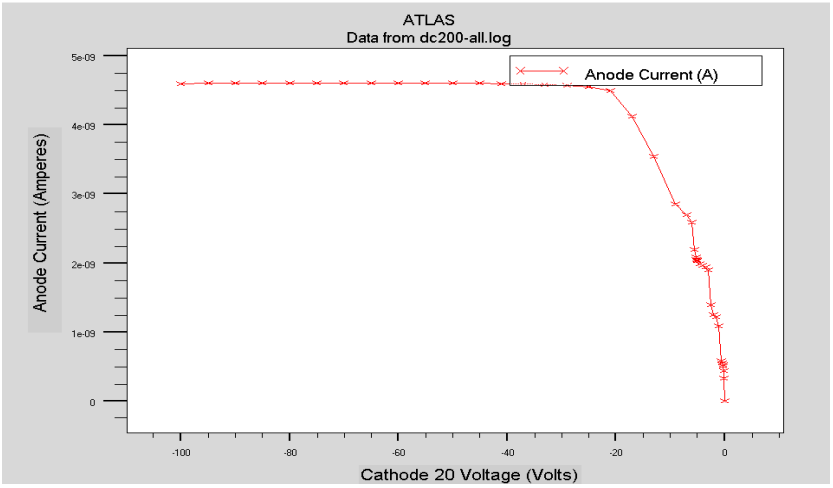

Fig. 4 : Anode current versus last cathode (C-20) voltage.

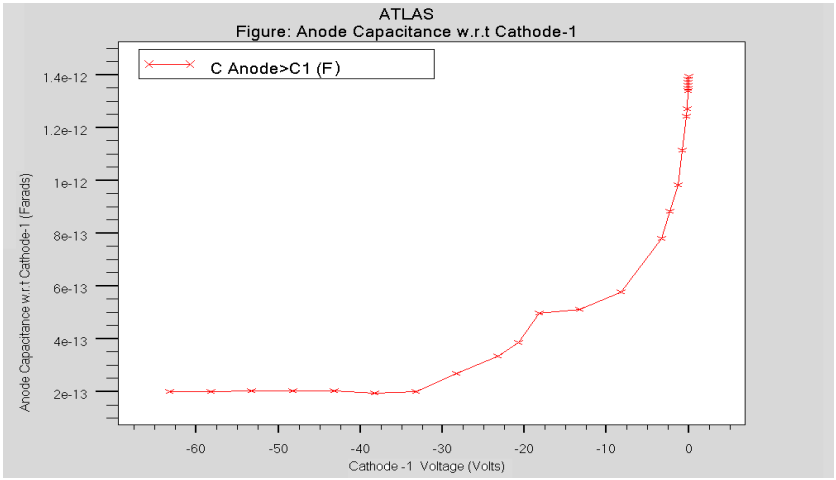

Fig. 5 : Anode Capacitance versus Cathode-1 voltage.

ii. *Junction field effect transistor (JFET)*

The virtual SDD-JFET detection system was again ported to the device simulator and device characteristics of the JFET alone were studied. The JFET was biased in common source configuration with the source at 0V and drain voltage of 30.5V and gate voltage varied from 0V to –20V (Transfer characteristics illustrated in figure 7). Fig. 6 shows the I_D-V_{DS} (Drain) of the JFET having gate width of 172 μm. The gate pinch-off voltage is V_{GSOFF} = -6 V with a saturation drain current of ~6 mA (Fig. 6). The extracted Transconductance at I_D = 5 mA and V_{DS} =30 V is g_m = 1.7 mS. The slope of the I_D-V_{DS} curve in the saturation region corresponds to an output resistance of 18 kΩ. The extracted gate leakage current was 1 pA at operating conditions, which would be significantly small as compared to leakage current of the detector (4.5nA). This ensures that the shot noise contribution due to gate current is negligibly small as compared to the one associated with the detector leakage current. It was observed that the transistor does not breakdown even at V_{DS} = 42 V. The gate capacitance is in such a range that output capacitance of the SDD can be matched to get optimal results.

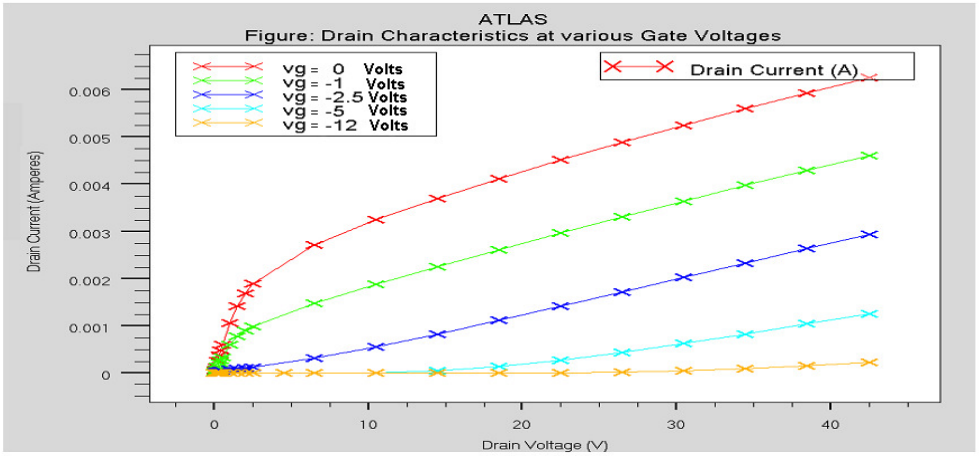

Fig. 6 : Drain Characteristics of embedded JFET.

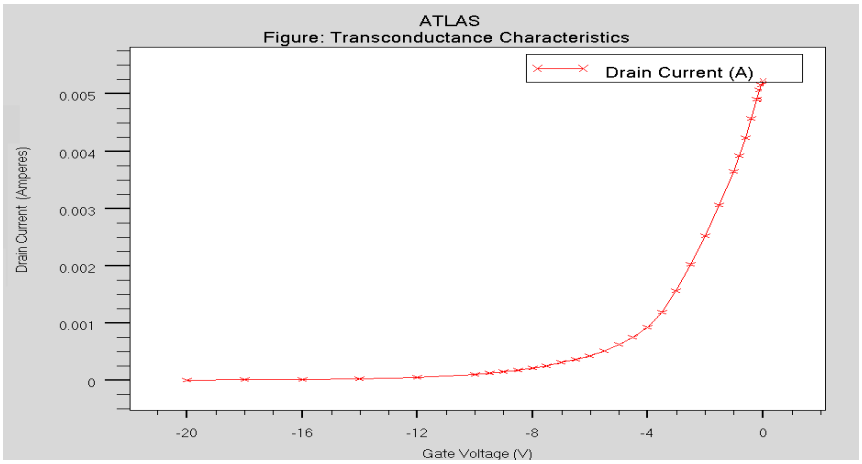

Fig. 7 : Transfer Characteristics of embedded JFET.

b) Dynamic Case Simulations of SDD-JFET composite system (with application of incident radiation)

The SDD - JFET system described in fig 7 has been subjected to an X-ray beam ($\lambda = 2$ A°) through a 10 μm wide slit. This was done to emulate a point source of light instead of a uniform shower to accurately estimate the drift time. Since the nuclear pulses are of short duration (nano seconds say) the simulated X-ray beam was a Gaussian with rise time of 0.1 ns and fall time of 0.4 ns. The beam intensity was fixed at 1 W/cm^2 as the beam aperture was only 10 μm wide, the actual optical power in this case turns out to be only 1 μWatt for an incidence area of 10 x 10 μm^2. The resultant anode current was extracted as a function of transient time, which gave a Gaussian current pulse (Equation-7) with the rise time depending upon the distance from the point of incidence on the detector. Simulations were performed for X-ray incidence distances of 500, 1000, 1500, 2000 and 2200 μm from the anode, and the current pulses at the anode were extracted. It was found that the current at the anode was delayed and rise times increased with increase in the distance of the X-ray incidence point from the anode. Drift times varied proportionately with the drift distance thus maintaining drift time to drift distance linearity. Alternatively, it was also found that the current pulse at the anode experienced significant broadening due to diffusion of the charge cloud. This effect is incremental with increase in drift distance from the anode. The net deposited charge (0.24 femto-Coulomb) always remains conserved in all cases. This dynamic simulation helped in accurate estimation of pulse timing and height characteristics. This helped in designing the latter end of the instrumentation chain like pre-Amplifier, shaper etc.

Additionally, a simulation was also performed in which both the SDD and JFET were biased in such a way that the anode of the SDD was shorted to the gate of the JFET and the combined node was connected to a resistor of 100 k Ohm and the other end of the resistor was connected to ground potential. This ensured that the anode current would be dropped across the resistor and this voltage drop would be fed to the gate of the JFET, which in turn would result in a dynamical change in the drain current (ref. Fig. 8). This ensures that the small change in the anode current would be amplified by the transistor to give a large change in the drain

current. In this simulation the rest of the SDD biasing remained same and the drain bias was fixed at 30 Volts through a bias resistor of 10 kΩ for a source bias of zero volts (common source configuration).

$$I = \frac{I_o}{\sigma\sqrt{2\pi}} e^{\frac{-(x-x_o)^2}{2\sigma^2}} \quad \text{--- Eq. 7}$$

Where

I_o = Maximum anode leakage current

x_o = Drift distance

σ = Width of current pulse

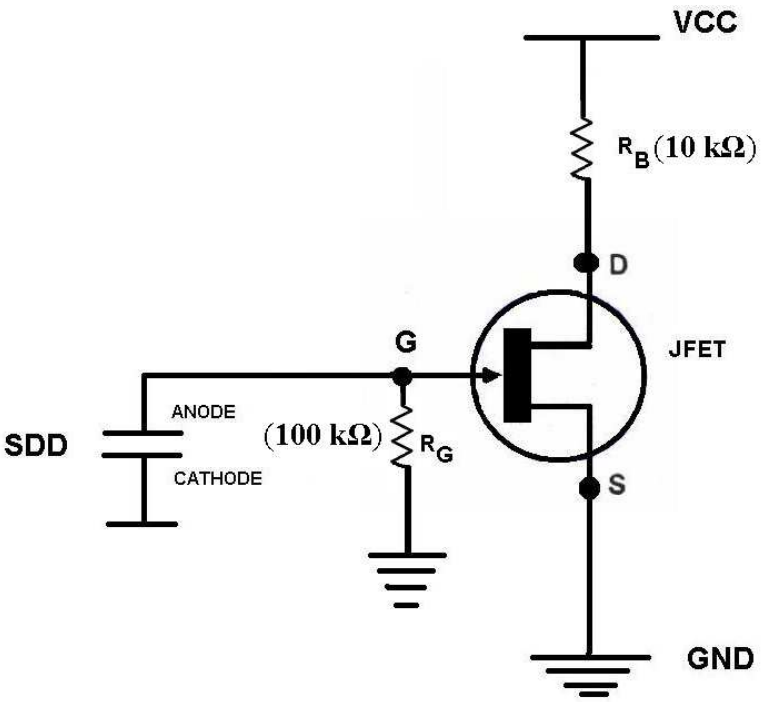

Fig. 8 : Circuit showing parasitics modeled in simulation.

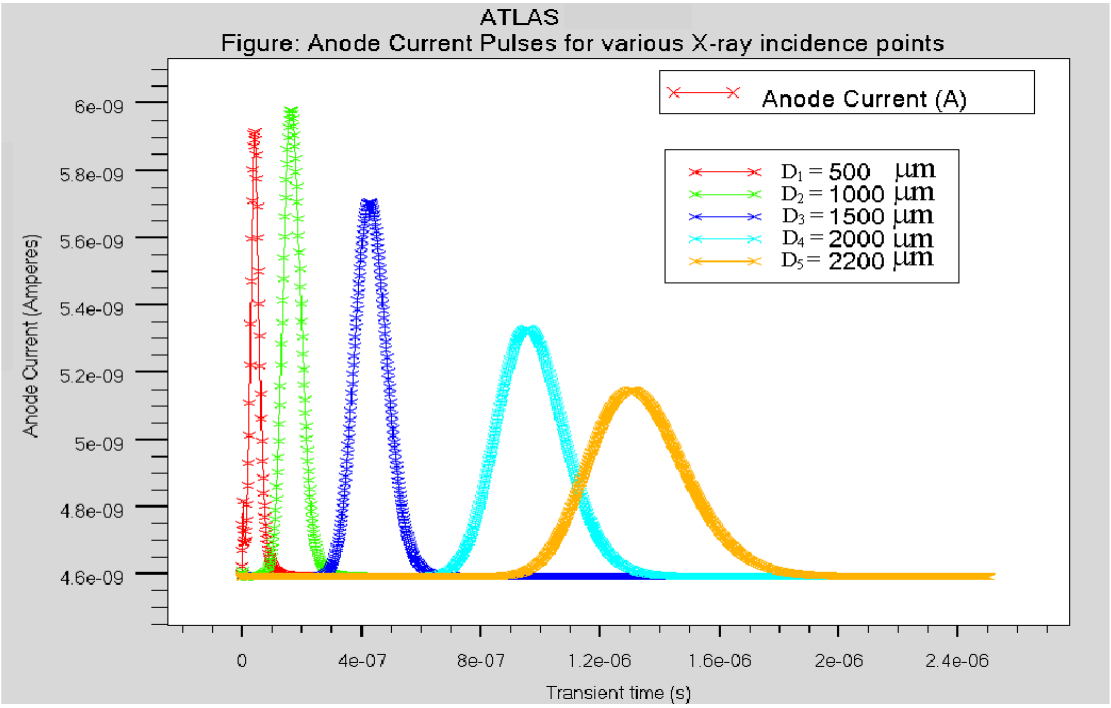

Fig. 9 : Dynamic current characteristics of the SDD.

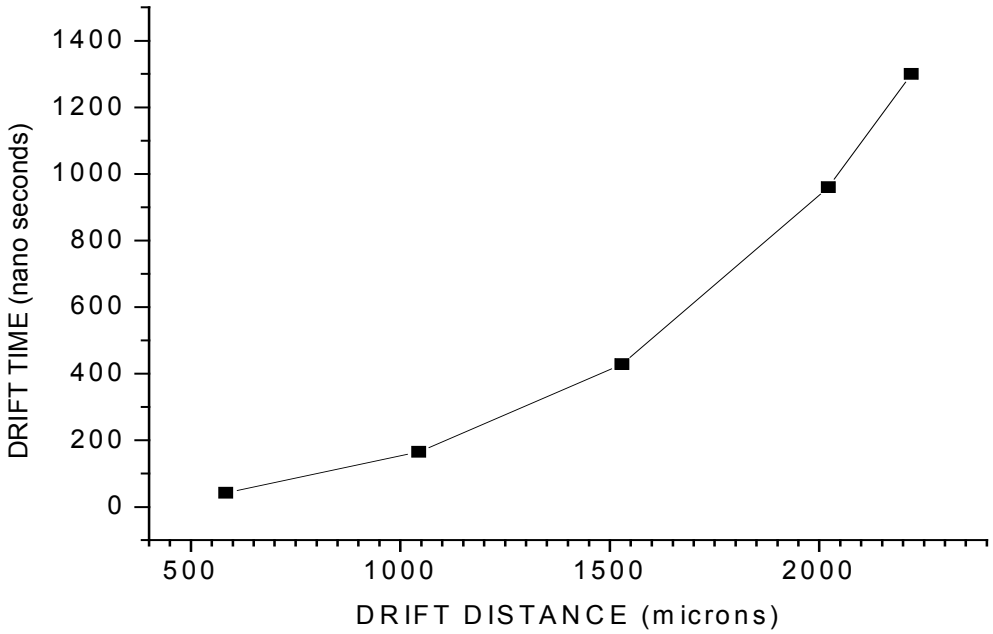

Fig. 10 : Drift time versus drift distance relationship in SDD.

V. Analytical Modeling Of SDD I-V Characteristics (Static Case)

I-V characteristics of the SDD have been analytically deduced to predict the leakage current behavior for various other designs fabricated at BEL. The values of the constituent parameters of equations 8 & 9 have been enlisted below in Table-1. The I-V curve resulting from the equations 8 & 9 has been illustrated in figure 11. As seen from the curve, the saturation behavior is similar to the one derived from simulation. The deviation of the saturation anode current derived from simulation from that achieved from I-V model is merely 4.8 %. This small value of deviation in saturation current shows that the model is fairly successful in predicting the behavior of the SDD's I-V characteristics.

$$I_R = J_s A\left|\left(1-e^{\left(\frac{qV}{\alpha KT}\right)}\right)*\left(e^{\frac{qV}{KT}}-1\right)\right| \text{------Amperes}$$

---- Eq. 8

α = Constant = 200 (depends on surface recombination velocity)

$$J_s = q\left(\sqrt{\frac{D_p}{\tau_p}}\frac{ni^2}{N_D}+\sqrt{\frac{D_n}{\tau_n}}\frac{ni^2}{N_A}\right);\ \text{Js} = 1.75\ \text{x}10^{-8}\ \text{Amperes/cm}^2$$

----- Eq. 9

Table 1 : Tabular form listing the values of constituent parameters of the Equations 8 & 9.

Sr. No.	Parameter	Symbol	Value
1	Total leakage current at anode	I_R	
2	Leakage current density	J_S	$1.75\ \text{x}10^{-8}$ Amperes/cm^2
3	Detector Active Area	A	0.27 cm^2
4	Boltzmann constant	K	$1.38\ \text{x}10^{-23}$ J/^{o}K
5	Electronic charge	q	$1.6\ \text{x}10^{-19}$ Coulombs
6	Ambient Temperature	T	300 ^{o}K
7	Applied reverse bias	V	0 to -100 Volts
8	Constant	α	200
9	Diffusion coefficient for Holes	D_P	12 cm^2/s
10	Diffusion coefficient for Electrons	D_n	36 cm^2/s
11	Hole Lifetime	τ_P	$1\text{x}10^{-5}$ s
12	Electron Lifetime	τ_n	$2\text{x}10^{-3}$ s

13	Intrinsic carrier concentration (300 ^{o}K)	n_i	$1x10^{10}$ cm^{-3}
14	Donor concentration	N_D	$1x10^{12}$ cm^{-3}
15	Acceptor concentration	N_A	$1x10^{18}$ cm^{-3}

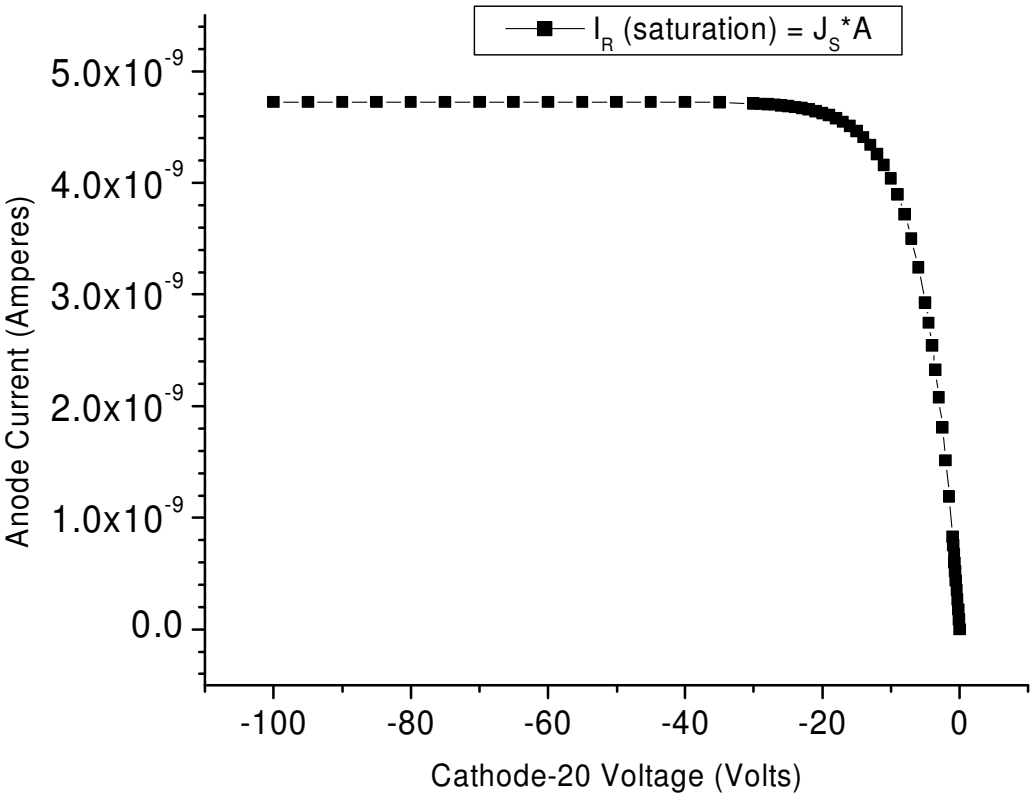

Fig. 11 : I-V Characteristics of SDD derived using I-V model.

VI. Conclusions

Noise analysis revealed the optimum value of capacitance mismatch factor (h) between SDD and JFET capacitances to be ~ 1. The relationship of shaping time with mismatch factor was found to be parabolic with minima at the optimum mismatch value. The net ENC too was found to be minimum at the optimum mismatch value. The full depletion anode capacitance derived from simulation was 200 fF for a full depletion voltage of -30V. The saturation value of anode leakage current was 4.5 nA. The transconductance derived from I-V simulation of the embedded JFET was 1.7mS for a gate pinchoff voltage of -6V. Dynamic simulations revealed the near linear dependence of drift time on drift distance within the SDD. Analytical modeling of the SDD's I-V characteristics showed a deviation of 4.8% in saturation anode current values achieved from simulation and analysis.

Acknowledgements

The author expresses a deep sense of gratitude for Late Dr. S. K. Kataria for his guidance and leadership. The author would like to especially thank Mr. Shekhar Basu and Dr. Sinha for their support, in addition to Mr. G. P. Srivastava, Mr. C. K. Pithawa, Mr. V.B. Chandratre, Mr. V.D. Srivastava & Mr. Sudheer K. M.

References Références Referencias

1. **E.Gatti, P.Rehak,** Nucl. Instrum. Meth. A, **225**, 608 (**1984**).
2. **P.Lechner, C.Fiorini, R.Hartmann, J.Kemmer, et al.,** Nucl. Instr. & Meth. **A**, 458, 281 (**2001**).
3. **A.Rashevsky, V.Bonvicini, P.Burger, S.Piano, C.Piemonte, A.Vacchi,** Nucl. Instr. & Meth. A, **485**, 54 (**2002**).
4. **P.Mehta, V.Mishra & S.K.Kataria,** " *Silicon drift detectors with integrated JFET: Simulation and design*", **Indian Journal of Pure and Applied Physics,** 43, 705 (**2005**).
5. **Pourus Mehta***, Sudheer K.M., **et al**, "*Studies of the Silicon Drift Detector: Design, Technology Development, Characterization & Physics Simulations*", **Armenian Journal of Physics**, Vol. 4, (**2011**), Issue 3, Pg. 175-192.
6. **Pourus Mehta**, "*Development of First Proto-Types of Silicon Drift Detectors: Design, Technology*

Development, Characterization & TCAD Simulations", International Journal on Electronic & Electrical Engineering, Vol 16 (2011), Issue 01, Pg. 58-70.

7. Pourus Mehta, "*A Proof of Principle Study of A Novel Semiconductor based Charge Particle Identification Telescope*", Armenian Journal of Physics, Vol. 5 (2012), Issue 01, Pg. 35-42.
8. Pourus Mehta, et.al, "Development of Commercial Grade Silicon Drift Detector with on-Chip JFET: Device Design, Technology & Characterization", Global Journal of Researches in Engineering, Volume 12 Issue 11 Version 1.0 September 2012.