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Capacitance-Voltage characteristics of nanowire trigate MOSFET considering wave function penetration

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Abstract - Capacitance is the heart of MOSFET because of its application in the real life. Capacitance indicates switching speed of the MOSFET. It is our goal to minimize capacitance as possible as we can in MOSFET. Due to our necessary to compact the Integrated Circuit as possible as we can for getting small electronics devices. Capacitance determine the speed of the IC. Every engineer in this section should know capacitance of his implementing device MOSFET to get exert result from this device. Whenever we deal with 10X10 nm scale or less device of MOSFET. We must be concerned the effect of wave function penetration into device in this stage classical mechanics fails to describe exact result of the system because electron can move in only one direction (say x) where in 3Dimention, it cannot move in other two direction (y, z). i.e. confined in two direction which is not predictable by classical mechanics here quantum mechanics (QM) gives better solution of this problem. Therefore we consider QM in our study. Here we presented how wave function play vital role when you consider small area of trigate MOSFET. This result will be helpful when you are determining capacitance of trigate MOSFET.

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CAPACITANCE-VOLTAGE CHARACTERISTICS OF NANOWIRE TRIGATE MOSFET CONSIDERING WAVE FUNCTION PENETRATION

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Capacitance-Voltage characteristics of nanowire trigate MOSFET considering wave function penetration

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Abstract - Capacitance is the heart of MOSFET because of its application in the real life. Capacitance indicates switching speed of the MOSFET. It is our goal to minimize capacitance as possible as we can in MOSFET. Due to our necessary to compact the Integrated Circuit as possible as we can for getting small electronics devices. Capacitance determine the speed of the IC. Every engineer in this section should know capacitance of his implementing device MOSFET to get exert result from this device. Whenever we deal with 10X10 nm scale or less device of MOSFET. We must be concerned the effect of wave function penetration into device in this stage classical mechanics fails to describe exact result of the system because electron can move in only one direction (say x) where in 3Dimention, it cannot move in other two direction (y, z). i.e. confined in two direction which is not predictable by classical mechanics here quantum mechanics (QM) gives better solution of this problem. Therefore we consider QM in our study. Here we presented how wave function play vital role when you consider small area of trigate MOSFET. This result will be helpful when you are determining capacitance of trigate MOSFET.

Keyword : Trigate MOSFET, wavefunction penetration, classical mechanics

I. INTRODUCTION

Trigate is a new technology which controls gate current using three wing around silicon dioxide of MOSFET. This device is called nanowire when its gate length is less than 100nm. Wave function penetration becomes vital role when cross section area of silicon of MOSFET becomes less than 10x10nm. We will consider 7x7 nm cross section area of silicon and channel length will be 20nm. Which is shown in figure(1). We also consider SiO_2 as insulator and Aluminum as electrode in our experiment. It is necessary to know the capacitance-voltage characteristics of trigate MOSFET whenever we implement this type of MOSFET. As transistor per chip is reducing day by day so we have to consider quantum mechanics not

classical mechanics because quantum mechanics give actual probability of C-V characteristics than classical mechanics. To get actual result from quantum mechanics we used here self –consistent of Schrödinger-Poisson's solver. Capacitance has mainly three region 1) accumulation region 2) depletion region and 3) inversion region. Actually inversion layer becomes volume inversion in our selected area this is cause of quantum effect.

II. THEORY

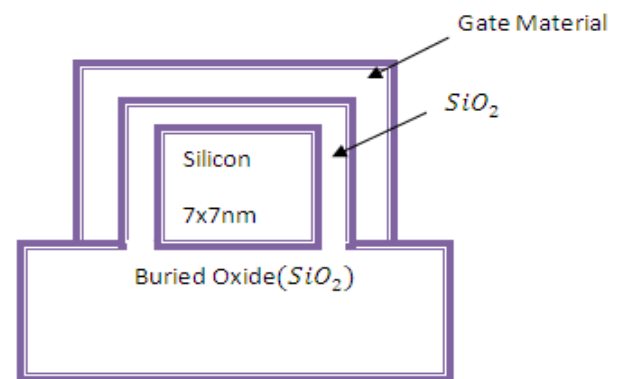


Figure1 : Cross section area of trigate MOSFET.

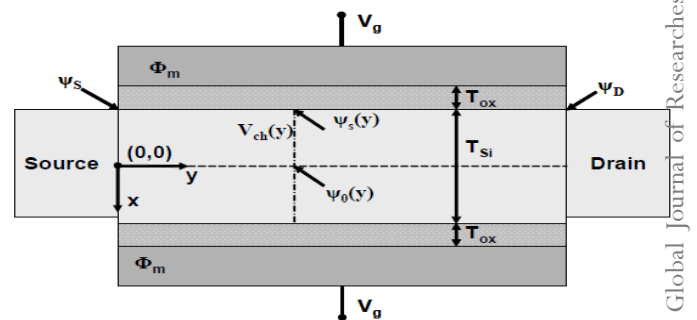


Figure 2 : Schematic of the symmetric common-gate DG-FET under study.

The I-V model is adequate only for describing the DC behavior but for transient description the capacitances are absolutely essential. The intrinsic capacitances of the transistor are derived from the terminal charges. The charge on the top and bottom gate electrodes is equal to total charge in the body. The total charge is computed by integrating the charge

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along the channel since the two gates are electrically interconnected, we have

$$Q_g = 2WC_{ox} \int_0^L (V_g - V_{fb} - \psi_s(y)) \cdot dy \quad (1)$$

Where

Q_g = the charge on the electrically interconnected gate.

$\psi_s(y)$ = surface potential as a function of the position y along the length of the transistor.

The inversion charge in the body is divided between the source and drain terminals using the Ward-Dutton charge partition approach [1].

The charge on source terminal (Q_s) is:

$$Q_s = -2WC_{ox} \int_0^L \left(1 - \frac{y}{L}\right) \cdot \left(V_g - V_{fb} - \psi_s(y) - \frac{Q_{bulk}}{C_{ox}}\right) \cdot dy \quad (2)$$

Where

V_g = the gate voltage.

Q_{bulk} = bulk charge = $\sqrt{2q\epsilon_{Si}N_A\psi_{pert}}$

ψ_{pert} = perturbation potential.

V_{fb} = the flat band voltage.

Using charge conservation, the charge on drain terminal (Q_d) can be expressed as:

$$Q_d = -2WC_{ox} \int_0^L \frac{y}{L} \cdot \left(V_g - V_{fb} - \psi_s(y) - \frac{Q_{bulk}}{C_{ox}}\right) \cdot dy \quad (3)$$

The surface potential as a function of the position y along the length of the transistor ($\psi_s(y)$) is obtained using current continuity. Current continuity states that the current is conserved all along the length of the transistor.

$$I_d(L) = I_d(y) \quad \text{where } 0 \leq y \leq L$$

$\psi_s(y)$ can be related to ψ_S and ψ_D by

$$\frac{y}{L} \cdot (B - \psi_S - \psi_D)(\psi_D - \psi_S) = (B - \psi_S - \psi_s(y))(\psi_s(y) - \psi_S)$$

where

$$B = 2 \left(V_g - V_{fb} - \frac{Q_{bulk}}{C_{ox}} + 2 \frac{kT}{q} \right)$$

ψ_D = the surface potential at the drained .

ψ_S = Surface potential at source terminal.

$$\psi_s = 2 \frac{kT}{q} \left(\ln(\beta) - \ln(\cos(\beta)) + \ln \left(\frac{2}{T_{Si}} \sqrt{\frac{2\epsilon_{Si}kTN_A}{qn_i^2}} \right) \right) + \psi_{pert}$$

Where

$$\beta = \frac{T_{Si}}{2} \sqrt{\frac{q^2}{2\epsilon_{Si}kT} \frac{n_i^2}{N_A} e^{\frac{q(\psi_0(y) - V_{ch}(y))}{kT}}}$$

Where

$V_{ch}(y)$ = the channel potential.

$\psi_0(y)$ = the potential at the center of the body.

The terminal charges are obtained by substituting $\psi_s(y)$ in Eqs. (1-3) and evaluating the integrals

$$\begin{aligned}
 Q_g &= 2WLC_{ox} \left(V_{gs} - V_{fb} - \frac{\psi_s + \psi_D}{2} + \frac{(\psi_D - \psi_s)^2}{6(B - \psi_D - \psi_s)} \right) \\
 Q_d &= -2WLC_{ox} \left(\frac{V_{gs} - V_{fb} - \frac{Q_{bulk}}{C_{ox}}}{2} - \frac{\psi_s + \psi_D}{4} + \frac{(\psi_D - \psi_s)^2}{60(B - \psi_D - \psi_s)} \right. \\
 &\quad \left. + \frac{(5B - 4\psi_D - 6\psi_s)(B - 2\psi_D)(\psi_s - \psi_D)}{60(B - \psi_D - \psi_s)^2} \right) \\
 Q_s &= -(Q_{fg} + Q_{bg} + Q_{bulk} + Q_d)
 \end{aligned} \quad (4)$$

The expressions for terminal charges are continuous and are valid over sub-threshold, linear and saturation regimes of operation. The terminal charges are used as state variables in the circuit simulation. All the capacitances are derived from the terminal charges to ensure charge conservation. The capacitances are defined as:

$$C_{ij} = \frac{\partial Q_i}{\partial V_j} \quad (5)$$

Where, i and j denote the multi-gate FET terminals. Note that C_{ij} satisfies

$$\sum_i C_{ij} = \sum_j C_{ij} = 0 \quad (6)$$

Effect of Quantum mechanics on capacitances

Using a self-consistent Schrodinger-Poisson solver, we can analyze the effect of wave function penetration on the capacitance. The study reveals that accounting for wave function penetration into the gate dielectric causes carrier profile to be shifted closer to the gate dielectric reducing the electrical oxide thickness. This shift increases with increasing gate voltage. This shifting results in an increased capacitance.

It is well known that direct tunneling currents become significant in this regime and that the penetration of the wave function cannot be neglected [2]–[3], the capacitance of NMOS capacitors in the inversion region accounting for wave function penetration into the gate dielectric. The physical basis has been presented in [4] and [5].

In this work, the Schrodinger and Poisson equations are solved self consistently assuming that the wave function penetrates the gate dielectric. The wave function is assumed to go to zero at some point deep inside the substrate, while a traveling wave boundary condition is imposed at the gate dielectric-gate electrode interface. The wave function inside the gate dielectric is connected to the asymptotic wave function in the gate electrode using the quantum transmitting boundary method [6].

The gate capacitance under strong-inversion conditions can be described by the equivalent circuit shown in Figure 3 consisting of the oxide capacitance C_{ox} and the inversion-layer capacitance C_{inv} [7], [8]. The latter includes the contributions of both the electrostatic capacitance $C_{es,Si}$ and the quantum capacitance C_q [9] of the inversion layer. While $C_{es,Si}$ is related to the average distance of the channel electrons from the Si/SiO₂ interface, C_q is related to the density of states (DOS) in the inversion layer.

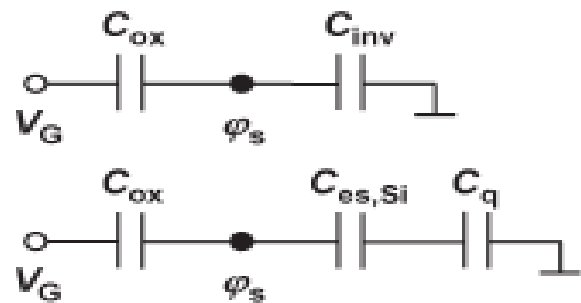


Figure 3 : Equivalent circuit for the gate capacitance in silicon MOS structures

Where

C_q =quantum capacitance.

$C_{es,si}$ = electrostatic capacitance.

C_{ox} = oxide capacitance .

C_{inv} = inversion-layer capacitance.

III. RESULT AND DISCUSSION

In the text [2], Schrodinger's equation has been solved by forcing the wave function to zero at the dielectric-gate electrode boundary.

The C-V characteristics have come by solving Schrodinger-Poisson equation. These figure indicate that how wave function penetration play vital role in the case of small thickness of oxide. In our simulation we present wave function penetration in the gate electrode rather than classical mechanics.

The C-V calculated assuming such a border condition differs by an immaterial quantity from the C-V calculated by letting the wave function penetrate into the gate electrode.

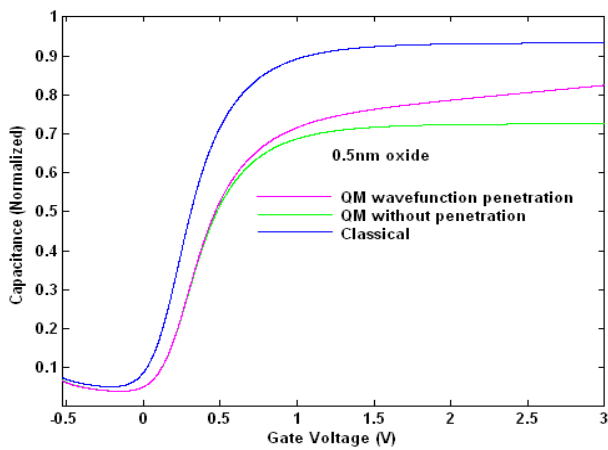


Figure 4 : Normalized classical and quantum mechanical capacitance obtained with and without wave function penetration for 0.5 nm oxide capacitor.

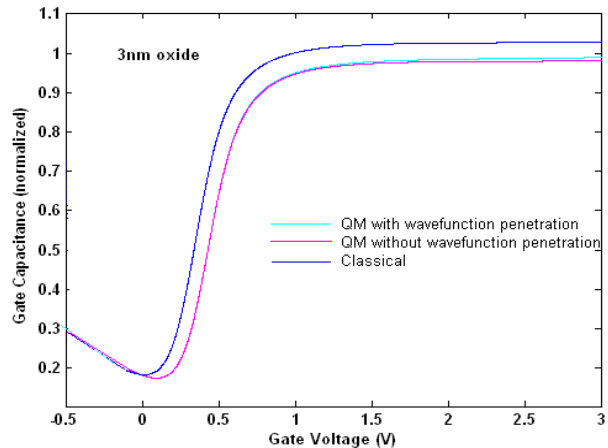


Figure 5 : Normalized classical and quantum mechanical capacitance obtained with and without wave function penetration for 3 nm oxide capacitor.

The classical and quantum-mechanical $C-V$ individually with and without wave function penetration for a metal- SiO_2 - Si system of gate oxide thicknesses 0.5 nm and 3.0 nm are exposed in Figs. 4 and 5 correspondingly. The capacitances are normalized to the strong inversion.

Classical capacitance values to help comprehend the impact of accounting for wave function penetration. It can be undoubtedly seen that the impact is larger for the 0.5 nm gate oxide case. There are two effects that contribute to the considerably superior impact for the 0.5 nm case. They are

- 1) the field across the 3 nm gate oxide device is weaker than the field across the 0.5 nm device and
- 2) the percentage contribution of the shift of the wave function closer to the interface is larger for the 0.5 nm gate oxide device the impact of this shift would be larger for the thinner oxide case.

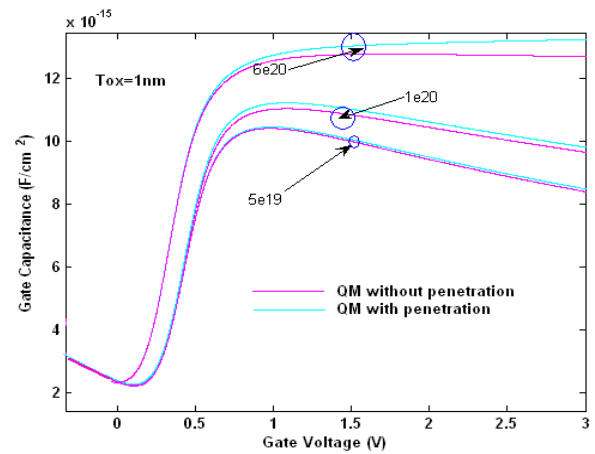


Figure 6 : Capacitance values for a 1.0 nm gate oxide capacitor with different doping with and without wave function penetration.

The $C-V$ simulations discussed thus far were performed on devices with a metal gate. However, despite detrimental effects, poly silicon is still being used as the gate electrode. Hence, simulations were also performed with poly silicon replacing the metal as the gate electrode. The simulation results (Figure 6) show that the wave function shift in the wave function influences the $C-V$ significantly only for poly doping of greater than 1×10^{20} cm⁻³. This seems to indicate that the poly-depletion effect dominates over the shift effect due to wave function penetration and the models developed so far seem sufficient. It must, however, be pointed out that as the devices are scaled down to sub-20 nm gate lengths, metal gate electrodes will have to be used to obtain lower effective oxide thicknesses and higher capacitance values. Thus when metal gate electrodes are used the effect of wave function penetration will have to be considered.

Accounting for wave function penetration into the gate electrode causes a shift in the wave function closer to the interface, the more so the greater the voltage. This bias dependent shift results in a lower electrical oxide thickness and hence higher gate capacitance. The poly depletion effect is dominant over the wave function penetration effect. However, this effect is significant when highly doped poly silicon gates are used and will become significant when metal gate electrodes are used and the oxide thickness is reduced.

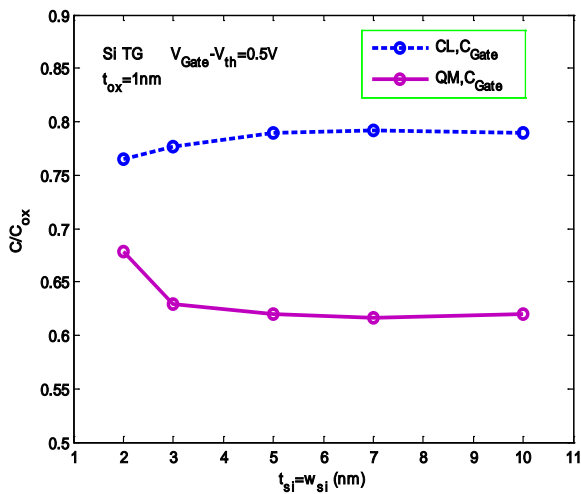


Figure 7 : C_{ox} in series and C_q and gate capacitance normalized to the C_{ox} of trigate MOS structures as a function of the silicon cross section. (Full symbols) Quantum-mechanical and (open symbols) classical results are compared.

Figure 7: the gate capacitance is shown normalized to C_{ox} , i.e., the maximum achievable capacitance value for every structure, as a function of the silicon size. Both quantum-mechanical and classical results are compared. From Figure 7 a continuous increase in the C_G/C_{ox} ratio can be observed as the channel cross section is scaled below 7 nm x 7 nm. We have actually observed an increase in the C_G/C_{ox} ratio when the channel cross section is scaled below 7 nm x 7 nm. We have related this to quantum effects since no increase in C_G/C_{ox} has been observed from classical calculations. The gate capacitance of trigate MOS structures is affected by quantum effects mainly via the spatial electron distribution. The quantum effects on C_q have been found to be less important for the gate capacitance except for very small cross sections in the order of 2 nm x 2 nm.

IV. CONCLUSION

A comprehensive analysis of the effects of wave function penetration on the capacitance of NMOS capacitors has been performed. The study reveals that accounting for wave function penetration into the gate dielectric causes carrier profile to be shifted closer to the gate dielectric reducing the electrical oxide thickness. This shift increases with increasing gate voltage. In our work we present Capacitance-Voltage characteristics of Trigate MOSFET considering wave function penetration which is necessary for implementing Integrated Circuit in real life. We hope it will be helpful instrument for working in practical life.

REFERENCES RÉFÉRENCES REFERENCIAS

1. D. Ward, R. Dutton: A charge-oriented model for MOS transistor capacitances. *IEEE J. Solid State Circuits* 13, 703 (1978).
2. F. Rana, S. Tiwari, and D. A. Buchanan, "Self-consistent modeling of accumulation layers and tunneling currents through very thin oxides," *Appl. Phys. Lett.*, vol. 69, pp. 1104–1106, 1996.
3. W.-K. Shih *et al.*, "Modeling gate leakage current in nMOS structures due to tunneling through an ultra-thin oxide," *Solid-State Electron.*, vol. 42, pp. 997–1006, 1998.
4. S.-H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum mechanical modeling of electron tunneling from the inversion layer of ultra-thin oxide nMOSFET's," *IEEE Electron Device Lett.*, vol. 18, pp. 209–211, May 1997.
5. S. Mudanai *et al.*, "Modeling of direct tunneling current through gate dielectric stacks," in *Proc. SISPAD*, Sept. 2000, pp. 200–203.
6. C. S. Lent and D. J. Kirkner, "The quantum transmitting boundary method," *J. Appl. Phys.*, vol. 67, pp. 6353–6359, May 1990.
7. S. Takagi and A. Toriumi, "Quantitative understanding of inversion-layer capacitance in Si MOSFETs," *IEEE Trans. Electron Devices*, vol. 42, no. 12, pp. 2125–2130, Dec. 1995.
8. F. Schwier, H. Wong, and J. J. Liou, *Nanometer CMOS*. Singapore: Pan Stanford Publishing, 2010.
9. S. Luryi, "Quantum capacitance devices," *Appl. Phys. Lett.*, vol. 52, no. 6, pp. 501–503, Feb. 1988.