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Design and Implementation of Low Power 12-Bit 100-MS/s Pipelined ADC Using Open-Loop Residue Amplification

By Appa Rao M., Dr. Ramana Reddy P. & Cyril Prasanna Raj P.
JNTUA College of Engineering. Ananthapur

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I. Introduction

Many and the communication systems today digital signal processing (DSP) to resolve the transmitted information. Therefore between the received analog signal and DSP system an analog-to-digital interface is necessary. This interface achieves the digitization of received waveform subject to a sampling rate requirement of the system. Being a part of communication system, the low power constraint mentioned above the A/D interface also needs to address to the low power constraint. There are many ADC architectures; pipelined ADCs are advantageous and widely used in applications with signal bandwidths that are too high for oversampling delta-sigma ADCs and resolution requirements that are too high for flash ADCs. Nevertheless they are sensitive to distortion introduced by the residue amplifiers in their first few stages, and residue amplifier distortion tends to be inversely related to both power supply voltage and power consumption. Therefore, the residue amplifiers are usually the dominant consumers of power in high-resolution pipelined ADCs, particularly in low supply voltage designs [1]–[6]. Among the key building blocks in pipelined ADCs are the residue amplifiers that interface successive converter stages. Especially in the converter front-end, these gain elements have to meet very stringent speed, noise, and linearity requirements and tend to dominate overall power dissipation. To address this issue, a variety of techniques have been developed to minimize amplifier power in pipelined ADCs. Among them, stage scaling [3], [4], optimization of the per-stage resolution [5]–[7], and amplifier sharing techniques [8], [9] are commonly used. In addition to their dominance in power consumption, it has also been recognized that residue amplifiers are most susceptible to complications that arise from continuing integrated circuit technology scaling [10], [11]. For implementations in future deep submicron processes, it is often predicted that limited supply headroom and low intrinsic device gain may lead to a relative power increase in such noise-limited precision analog circuit blocks [12], [13]. In this paper, a pipelined ADC is designed that achieves superior SNR, and operates at 100Msps, with power dissipation less than 70mW. Section II discusses pipelined ADC architecture, section III discusses design of software model for proposed pipelined ADC. Section IV discusses the schematic design of pipelined ADC and layout design. Section V presents conclusion.

a) Architecture of Pipelined ADC

The purpose of analog to digital converts is to sample and digitize an analog signal. The more precisely the analog signal is converted to digital, the more information can be obtained from it. It is also desirable to convert high bandwidth or high frequency analog signals; thus, ADCs must be capable of a fast sampling rate as well being accurate. The pipeline ADC is the architecture of choice for applications that require both speed and accuracy and where latency is not concern. The basic idea behind the pipeline ADC is that each stage will first sample and hold the input then it is compared with *VREF*/2. If the input is greater than

Author α : Research Scholar, JNTUA college of Engineering, Anantapur & Associate Professor in PACE Institute of Technology and Sciences, Ongole. E-mail : dsajvrao@gmail.com

Author σ : Associate Professor & Head, JNTUA College of Engineering, Anantapur. E-mail : prrjntu @gmail.com

Author ρ : Professor & Course Manager, MSRSAS, Bangalore. E-mail : cyrilyahoo@gmail.com

VREF/2, output a 1 for that stage and pass the input voltage directly to the next stage. If the input is less than *VREF*/2, output a 0 for that stage and multiply the input voltage by 2 before passing it to the next stage. Figure 1 shows the block diagram for this basic operation.

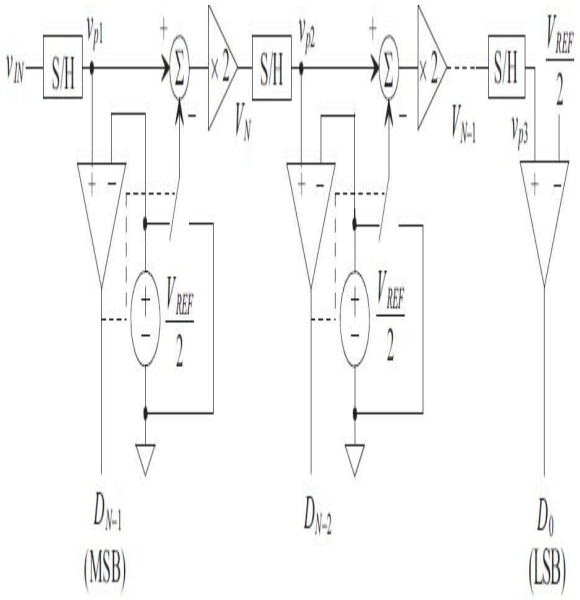


Fig. 1 : Pipeline ADC Block Diagram [1]

There are a few challenges with the basic pipeline ADC architecture that this project will attempt to address. Before looking at the sources of error, it is worth noting that an error in the early stages of the pipeline will propagate through the pipeline affectively being amplified by 2 by each successive stage. Errors can be created by the comparators not switching at the correct point. This means that the comparator may have some offset which will result in it making the wrong decision. The sample and hold may also have some offset causing the wrong voltage to be passed to the comparator which will result in the same problem of the comparator making a wrong decision. The other source of error is the multiply by 2 function, because it is difficult to multiply by a gain of exactly 2. These limitations with real op-amps and comparators will result in integral nonlinearity (INL) and differential nonlinearity (DNL) errors. This design requires 12-bit resolution. This means that there will be 2^{12} or 4096 possible output bit combinations. Assuming a *VREF* of 1V, 1LSB or the level of analog resolution is given by

$$1LSB = \frac{V_{REF}}{2^N} = \frac{1}{4096} = 244\mu V$$

To correct the errors caused by the offsets in the comparators and the sample and hold op-amps, a technique called 1.5 bits/stage will be used. The name 1.5 bits/stage is based on the fact that each stage has an output with three possible cases consisting of *a* and *b* signals, where *ab* can be 00, 01, or 11. The ideal transfer curve for the 1.5 bits/stage of *vin* versus *vout* is shown in Figure 2. And, the relationship between *vin* and *vout* can be expressed as:

$$v_{out} = 2 \cdot \left(v_{in} + \overline{ab}\frac{V_{CM}}{2} - \bar{a}b\frac{V_{CM}}{2} - ab\frac{3V_{CM}}{2}\right).$$

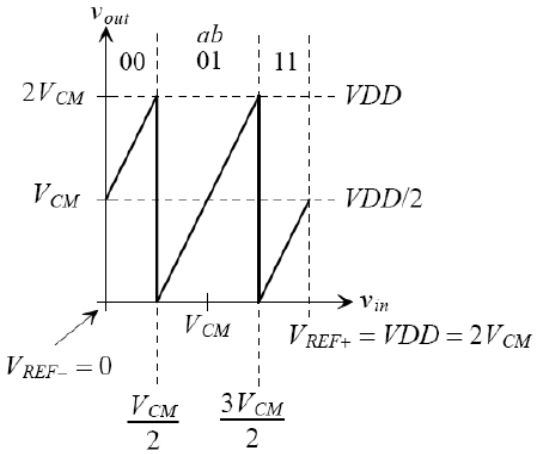


Fig. 2 : 1.5 Bits/Stage Transfer Curve (Single-ended) [1]

b) Software reference model design of Pipelined ADC

The functional block diagram of the pipelined ADC is simulated using Simulink in MATLAB. The 1-bit single stage converter behavioural block has been designed and simulated. The behaviour of the block has been developed using the equations given below.

- If Vin > Vmid Vresidue=2(Vin-Vref)
- If Vin < Vmid Vresidue=2(Vin)

Using a reference value this single stage block would act as a comparator and gives a bit as output. Again that bit will be converted in to analog value that value again compared with the actual input signal and the difference signal will be produced. The difference signal will be in the range of half of the actual input range. Since the total pipelined architecture has been developed using these similar types of 1-bit single stage blocks should give the same input rage to all stages. To get that voltage range we should multiply the error signal with 2 then we can give output of one stage to input of next stage. Every stage has its own sample and hold circuit operating at 100 MS/s. the output of the sample and hold stage will be consider as the input to the 1-bit converter. Figure 3 shows the software reference model of 1-bit conversion.

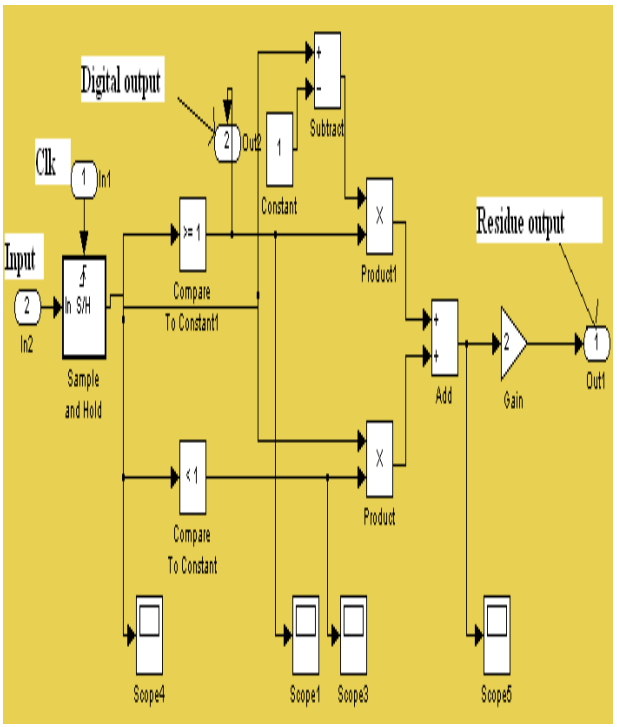


Fig. 3 : Simulink model for the 1-bit conversion stage

The input and output waveforms of this single stage are shown in Figure 4. The 1 MHz input sine wave has been sampled by the 100 MHz clock signal. Theoretically we can estimate the signal to noise ratio (SNR). SNR (worst case) = 6.02 n+4.24 dB Hence we have established the boundary conditions for the choice of the resolution of the converter based upon a desired level of SNR. Based on this calculation the 12-bit pipelined ADC having (SNR) 68 dB.

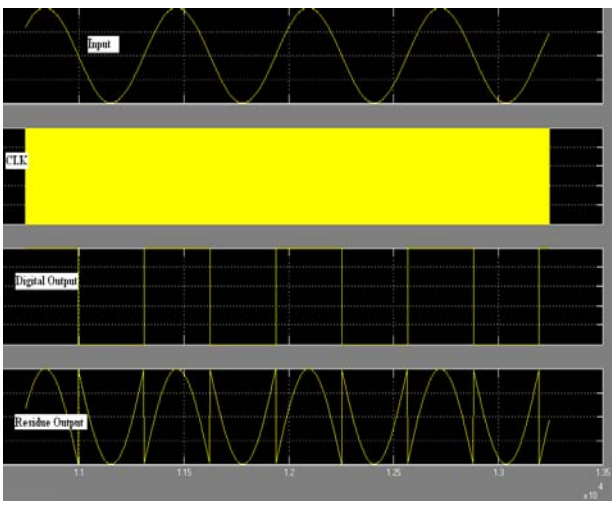


Fig 4 : Digital and Residue output waveforms of the single stage pipelined ADC

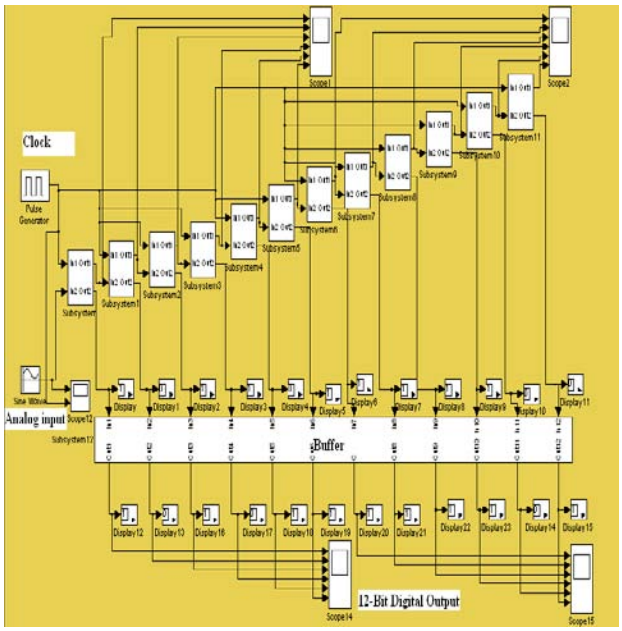


Fig. 5 : Matlab simulink model for the 12-bit pipelined ADC

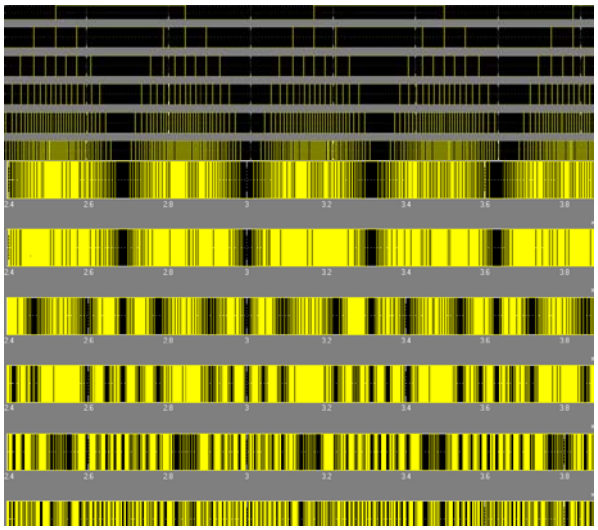


Fig. 6 : Digital output from the 12-bit pipelined ADC for sine wave

II. VLSI Implementation Of The 12-Bit Pipe Lined ADC

a) Bit Single Stage of Pipelined architecture

This stage is consist of sample and hold circuit followed by 1-bit ADC, 1-bit DAC, subtracted and multiplier. The analog signal will be sampled and fed to the comparator acts as the 1-bit ADC that would give the 1-bit digital output. Before giving to the comparator the sample signal should lift to the .9V of the DC voltage so that the comparator can compare the value to the threshold voltage and give the output. The digital output again converted to the analog value through the 1-bit DAC Uses two reference voltage levels. This converted value will be subtracted from actual sampled signal to

produce an error signal using a difference circuit. This signal often called as residue signal. This residue signal again multiplied by two with an open loop amplifier. The sub tractor and the multiplier are working at 100 MS/s and input rage of +/-300mV. The sub tractor and the multiplier are designed based on Op amp this op amp should work at 100 MHz by using normal op amps it is difficult to reach 100 MHz frequency.

b) Sample& Hold Circuit

In this paper work sampled hold circuits are implemented by the transmission gates and capacitors. The switched capacitor technique has been implemented to reduce the power. The input to the sample and hold circuit is sine wave having bandwidth of 1MHz and the sampled signal frequency is 100MHz. The delay between in out and output that will be offered by this sample and hold signal is 17ns. The output of the sample Hold signal is sampling signal having frequency of 100MHz

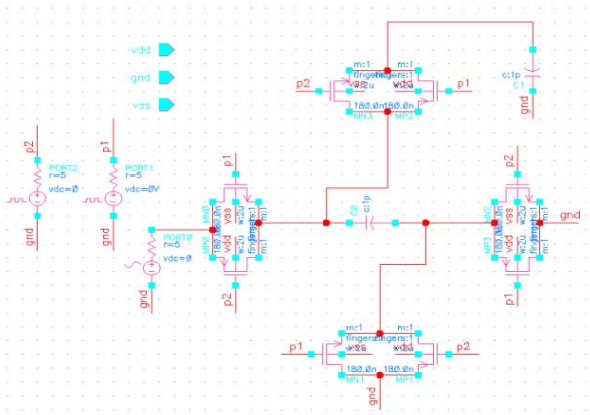


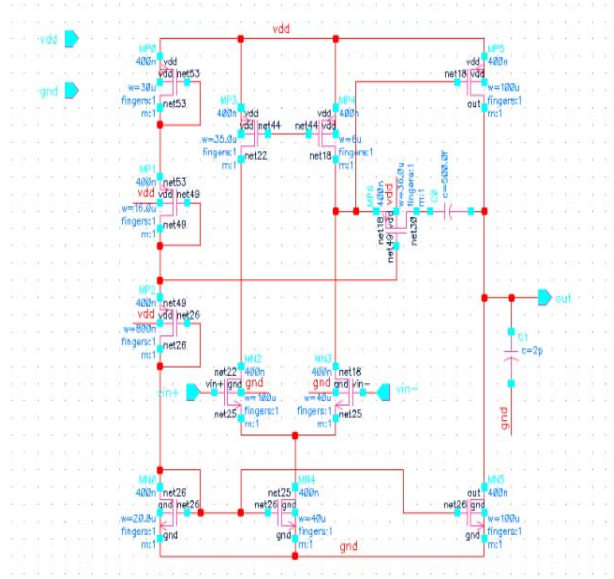
Fig. 7 : Schematic diagram and output results of the sample and hold circuit

c) Wideband Operational Amplifier Design

Subtraction and multiplier circuits are designed using the wideband op amp. The specifications of the amplifier identified from the top level simulation of 12-bit pipelined ADC by the MATLAB Simulink. The achieved parameters from the operational amplifier simulation are

DC Gain =75dB
Unity Gain Freq=160 MHz
Slew Rate=9.8e6 V/Sec
Phase Margin=57°
Input swing= +/- 0.35mV
Output swing= +/- 1.15V

The 3dB Bandwidth of the op- amp is selected as 100 MHz to meet the application of the architecture. The schematic has simulated by the cadence specter and layout has drawn by the virtuoso. The simulated transient and ac analysis waveforms are shown in the Figure 8.



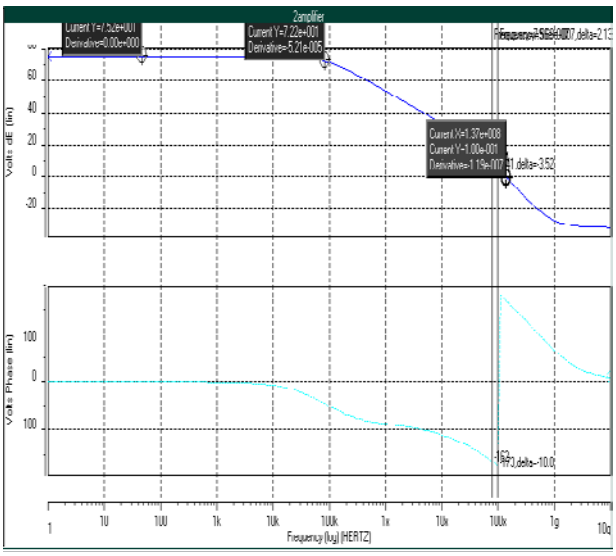


Fig. 8 : Wideband opamp schematic diagram and AC analysis

d) 1-Bit ADC design using CMOS Inverter

In this paper however a new approach the Threshold Inverter Quantizer (TIQ) based on systematic transistor sizing of a CMOS inverter in a full-flash scheme eliminates the resistor array implementation of conventional Comparator array flash designs. Therefore no static power consumption is required for quantizing the analog input signal making the idea very attractive for battery-powered applications. We can estimate safe analog input rage as follows:

Analog range = *Vdd* - (V_{TN} + | V_{TP}|), where V_{TN} and V_{TP} are the threshold voltages for large NMOS and PMOS devices, namely the V_{THO} value from the model parameter data set used during the entire design process.

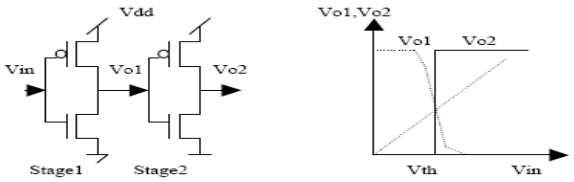


Fig. 9 : Schematic Diagram of Comparator

e) 1-Bit DAC Design

For the design of one bit DAC we have used pass transistors The CMOS transmission gate consist of one NMOS and one PMOS transistor connected in parallel. The gate voltages applied to these transistors are also set to be complementary signals. As such the CMOS TG operates as a bidirectional switch between the nodes in and out this is controlled by clock signal.

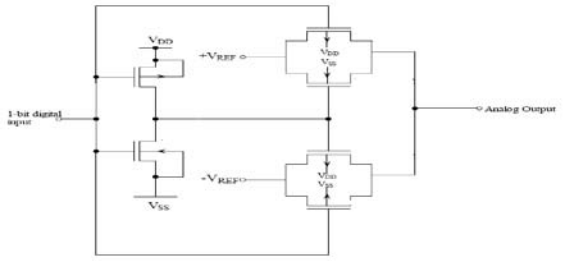


Fig. 10 : Schematic Diagram of 1-Bit DAC

f) Buffer Designing

This buffer stage is consist of number of Dffs, these Dff are designed using Tx-gates and NAND gates. The Schematics and Layout are shown in Figure 11. Through the practical calculations, I got the average rise and fall time is 0.18ns, and Setup Time is 154ps.

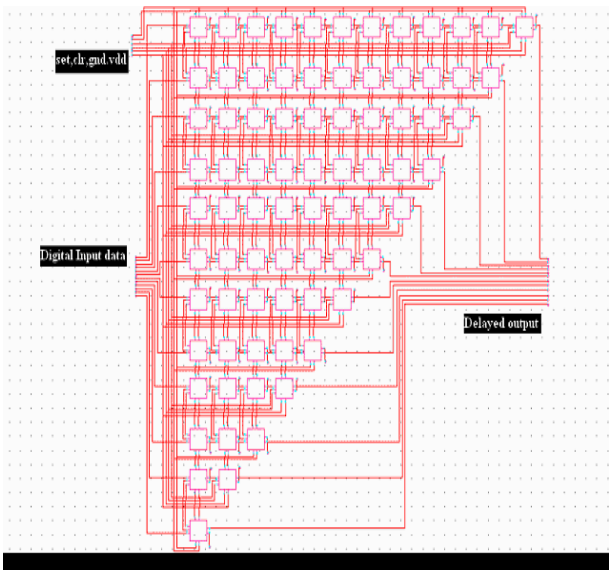


Fig. 11 : Schematic Diagram of 12-Bit Buffer

The digital outputs for a given input analog sample are not generated at the same time. MSB comes first and LSB last. The time delay between adjacent bits is one half clock cycle. All bits need to be synchronized. The 1-bit digital output from the first stage is delayed by 12 half cycles and the output from the second stage is delayed by 11 half cycles and so on. The output from the last stage is delayed by a half cycle. The delay block is made of D flip-flops (DFF) implemented with transmission gate and static NAND gates. Since sampling rate is only 100 MS/s and the word length is 12 bits the carry ripple is not an issue under 0.13μm process.

g) 1-Bit Single stage of Pipelined Architecture

This stage is consist of sample and hold circuit followed by 1-bit ADC, 1-bit DAC, subtracted and multiplier. The analog signal will be sampled and fed to the comparator acts as the 1-bit ADC that would give the 1-bit digital output. Before giving to the comparator the sample signal should lift to the 0.9V of the DC voltage, so that the comparator can compare the value to the threshold voltage and give the output.

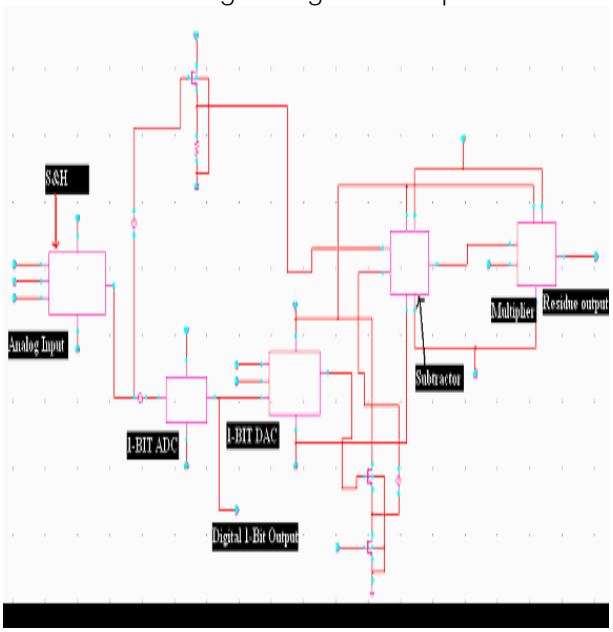


Fig. 12 : Schematic Diagram of 1-Bit Conversion Stage

The digital output again converted to the analog value through the 1-bit DAC, Uses two reference voltage levels. This converted value will be subtracted from actual sampled signal to produce an error signal using a difference circuit this signal often called as residue signal. This residue signal again multiplied by two with an open loop amplifier. The difference and the multiplier are working at 100 MS/s and input rage of +/-250mV.

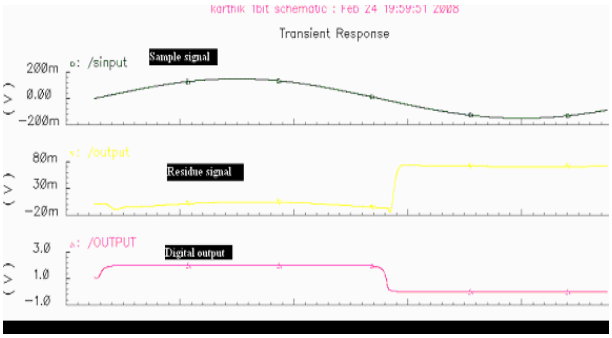


Fig. 13 : Output Wave Form of 1-Bit Conversion Stage

III. Result Analysis

The first signal on the above shown wave figure is the input sine wave having voltage rage of +/- 200mV. Last signal is the digital output from the single stage of pipelined ADC. The second signal is the residue output signal which is going to input of the next stage of the pipelined ADC. Since This residue signal is being affected by the loads at different stages we should amplify this signal before giving to the next stage.

a) Top-Level Schematic

The layout of the wide band two stage operational amplifiers is shown. The area occupied by the amplifier layout is 30um*36um.To implement layout fingering and inter digitized technique are used.

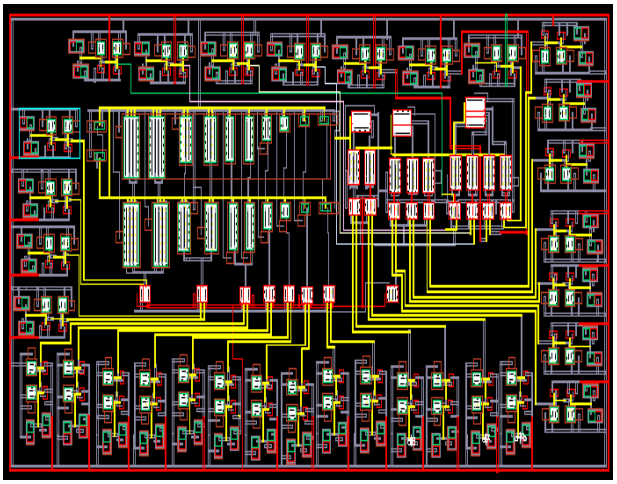


Fig. 14 : Top-Level Schematic of pipelined ADC

Figure 15 shows the frequency domain analysis of pipelined ADC. The output of ADC is captured and is processed using FFT processor to convert the time domain discrete samples to frequency domain samples. The frequency domain samples obtained are plotted and SNR is measured. In order to estimate the performance of ADC, a known input with single frequency is used as test vector. The frequency spectrum obtained is analyzed for the number of harmonics. The first five harmonics are considered to compute SNR.

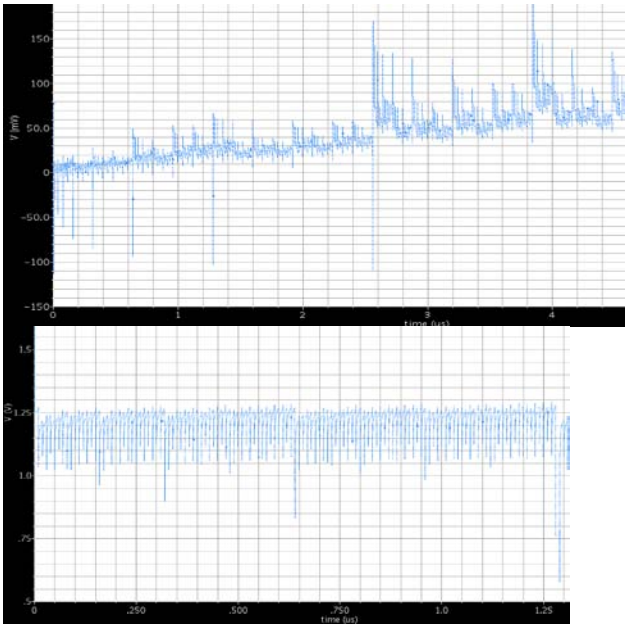


Fig. 15 : Frequency domain response of pipelined ADC.

The power consumption at a clock frequency of 100 MHz was 70 mW from a 1.8 V supply. Below Table 1 summarizes the measured results.

	Previous work	Present Work
Technology	CMOS 0.35um	CMOS0.13um
Power Supply	3V	± 1.8V
Input Signal Freq	200kHz	up to 10 MHz
Input voltage range	---	+/-250mV
Power dissipation	290uW	70mW
Area	7.9 mm2	6.5 mm2
Sampling freq	75MHz	100 MHz

Table 1 : Results comparison

IV. Conclusion

The goals of this paper is First different ADC architectures were analyzed to determine the optimal topology for the given performance specifications with minimum power consumption. Second the exact implementation of the chosen architecture was investigated in an effort to use the minimum amount of power. This Paper involved designing an integrated CMOS Analog-to-Digital converter for communication and video applications. The performance specifications were 12-bits, power dissipation less than 70 mW, area should be less than 6.5mm^2 and static performance parameters such as INL and DNL should be less than 1

LSB and 0.5 LSB in order to make a monotonic ADC. This pipelined ADC has been met the performance requirements. The ADC was designed in 0.13um technology at an operating voltage of ±1.8 V. Sample and hold circuit is designed by the switched-capacitor implementation. We can use the rail to rail op amp to increase the input voltage range of the ADC but by increasing the input voltage swing the resolution will be affected. Common-mode drift issue Since there is no common-mode feedback inside the loop the common-mode drift caused by the mismatch of capacitors, offset of op amp and charge injection will accumulate stage by stage. Careful design and layout are supposed to minimize the total drift within 100 mV such that the residue output signal will not be out of saturation. But this problem is likely to cause trouble if the common-mode signal is not controlled well as expected.

References Références Referencias

1. S. H. Lewis and P. R. Gray, "A pipelined 5-Msample/s 9-bit analog-todigital converter," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 954–961, Dec. 1987.
2. S.-M. Yoo *et al.*, "A 10 b 150 MS/s 123 mW 0.18 _m CMOS Pipelined ADC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2003, pp. 326–327.
3. T. Cho and P. R. Gray, "A10 b, 20 MSample/s, 35mWpipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 166–172, Mar. 1995.
4. D. W. Cline and P. R. Gray, "A power optimized 13-b 5 Msamples/s pipelined analog to- digital converter in 1.2-_m CMOS," *IEEE J. Solid-State Circuits*, vol. 31, pp. 294–303, Mar. 1996.
5. S. H. Lewis, "Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications," *IEEE Trans.Circuits Syst. II*, vol. 39, pp. 516–523, Aug. 1992.
6. J. Goes, J. C. Vital, and J. E. Franca, "Systematic design for optimization of high-speed self-calibrated pipelined A/D converters," *IEEE Trans.Circuits Syst. II*, vol. 45, pp. 1513–1526, Dec. 1998.
7. L. A. Singer and T. L. Brooks, "A 14-bit 10-MHz calibration-free CMOS pipelined A/D converter," in *Symp. VLSI Circuits Dig. Tech. Papers*, June 1996, pp. 94–95.
8. P. C. Yu and H.-S. Lee, "A 2.5-V, 12-b, 5-Msample/s pipeline CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1854–1861, Dec. 1996.
9. B.-M. Min, P. Kim, and D. Boisvert, "A 69 mW 10 b 80 MS/s pipelined CMOS ADC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2003, pp. 324–325.
10. J. Ming and S. H. Lewis, "An 8 b 80 MSample/s pipelined ADC with background calibration," in *IEEE Int. Solid-State Circuits Conf. Dig.Tech. Papers*, Feb. 2000, pp. 42–43.
11. E. B. Blecker, O. E. Erdogan, P. J. Hurst, and S. H. Lewis, "An 8-bit 13-MSamples/s digital-background-calibrated algorithmic ADC," in *Proc. Eur. Solid-State Circuits Conf.*, Stockholm, Sweden, Sept. 2000, pp. 372–375.
12. A.-J. Annema, "Analog circuit performance and process scaling," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 711–725, June 1999.
13. Boris Murmann and Bernhard E. Boser, "*A 12-Bit 75-MS/s Pipelined ADC Using Open-loop Residue Amplification*", IEEE Journal of Solid-State Circuits, vol. 38, no. 12, pp. 1-4, Dec. 2003.
14. A. Varzaghani and C. K. K. Yang, *"A 600 MS/s 5-bit pipelined analog-to-digital converter using Digital reference Calibration",* IEEE Journal of Solid-State Circuits, vol. 41, no. 2, pp. 1-4, Feb. 2006.
15. J. Arias, V. Boccuzzi, L. Quintanilla, L. Enríquez, D. Bisbal, M. Banu, and J. Barbolla, *"Low-Power Pipeline ADC for Wireless LANs",* IEEE Journal of Solid-State Circuits, vol. 39, no. 8, pp. 1-3, Aug. 2004.
16. J. Ming and S. H. Lewis, *"An 8 b 80 MSample/s pipelined ADC with background calibration",* in IEEE Int. Solid-State Circuits Conference, pp. 42-43, Feb. 2000.
17. Ali TANGEL and Kyusun CHOI, *"The CMOS Inverter as a comparator in ADC designs"*, The Pennsylvania State University, University Park, PA16802 USA.
18. Maysam Ghovanloo, "*A Classic Wide Band Operational Amplifier Design"*, University of Michigan, Ann Arbor, MI, 48109-2122.
19. Arash Loloee, Alfio Zanchi, Huawen jin, Shereef Shehata, Eduardo Bartolome,*" A 12 bit 80 Msps Pipelined ADC Core with 190mw consumption from 3v in 0.18um Digital CMOS",* Texas Instruments, Inc.-Wireless Infrastructure Data Converters 12500 TI Boulevard, MS8755-75243 Dallas, TX(U.S.A), 2002.
20. J. M. Rabaey, *"Digital Integrated Circuits- A design Perspective",* Prentice Hall India, 1996.
21. D. Johns and K. Martin, *"Analog Integrated Circuit Design",* John Wiley, New York, 1997.
22. Phillip E. Allen & Holberg, "CMOS *Analog Circuit Design*", Oxford University Press, Second edition, 2002. R. Jacob Baker, "*CMOS Mixed Signal Circuit Design",* IEEE Series on Microelectronic systems, NJ, 2002.

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