Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 4 Version 1.0 March 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Gate Level Design of a Digital Clock with Asynchronous-Synchronous Logic

By Sheikh Md. Rabiul Islam & Md. Jobayer Hossain
Khulna University of Engineering and Technology, Bangladesh

Abstract - A digital clock has been designed at gate level and is being presented in this paper. The clock architecture consists of three major blocks SECOND,MINUTE and HOUR. The architecture is the amalgam both of synchronous and asynchronous logic. All the flip-flops at each block run synchronously. The triggering operation of a block is asynchronous in nature. It serves the design requiring lower power consumption, provides lesser noise and electromagnetic interference, lower delay and greater throughput. The clock is designed at Xilinx System Generator, synthesized with Xilinx Synthesis Tool (XST) and Simulated by Vegilogger Pro 6.5.

Keywords : *Counter, asynchronous counter, synchronous counter, system level design, gate level design, GALS.*

GJRE-F Classification : *FOR Code: 090601*

Strictly as per the compliance and regulations of:

Gate Level Design of a Digital Clock with Asynchronous-Synchronous Logic

Sheikh Md. Rabiul Islam [α] & Md. Jobayer Hossain [α]

Abstract - A digital clock has been designed at gate level and is being presented in this paper. The clock architecture consists of three major blocks SECOND,MINUTE and HOUR. The architecture is the amalgam both of synchronous and asynchronous logic. All the flip-flops at each block run synchronously. The triggering operation of a block is asynchronous in nature. It serves the design requiring lower power consumption, provides lesser noise and electromagnetic interference, lower delay and greater throughput. The clock is designed at Xilinx System Generator, synthesized with Xilinx Synthesis Tool (XST) and Simulated by Vegilogger Pro 6.5.

Keywords : Counter, asynchronous counter, synchronous counter, system level design, gate level design, GALS.

I. Introduction

A digital clock is a type of clock that displays the time digitally. Instead of the rotary mechanism of electromechanical clock, it uses digital counters that count second, minute and hours. Each sixty seconds make a minute and each sixty minutes an hour. After twenty four hours the clock resets and starts from initial condition. The functional unit of a digital clock is a counter that represents a second, minute or hour block. A counter [7] may be defined as a register i.e. a group of flip-flops that goes through a predetermined sequence of states upon the application of input pulses. The logic gates in a counter are connected in such a way as to produce a prescribed sequence of binary states in the register.

There are two types of input/output (I/O) synchronization technique to design a counter [10]: synchronous and asynchronous technique. In an asynchronous counter, the flip-flop output transition serves as a source for triggering other flip-flops. In otherwords, the CP inputs of all flip-flops (except the first) are triggered not only by the incoming pulses but rather by the transitions that occur in other flip-flops. The asynchronous counter is also referred to as overlapped counter. A problem [7] in designing an asynchronous logic is that it cannot be described by Boolean equations developed for describing clocked sequential circuits. Again as output of one flip-flop acts as the input of another one, the system designed at asynchronous logic faces considerable delay. On the other hand, a synchronous circuit [13] is a digital circuit in which the parts are synchronized by a single clock signal. In an ideal synchronous circuit, every change in the logical levels of its storage components is simultaneous. These transitions follow the level change of a special clock signal. Ideally, the input to each storage element has reached its final value before the next clock occurs, so the behavior of the whole circuit can be predicted exactly. Practically, some delay is required for each logical operation, resulting in a maximum speed at which each synchronous system can run [13]. Thus in a synchronous counter [7] all the flip-flops are clocked simultaneously. The decision whether a flip-flop is to be complemented or not is determined from the values of the T inputs at the time of pulse. If T=0, the flip-flop remains unchanged. If T=1, the flip flop complements. Thus the states of the counters get changed. Synchronous logic suffers from some disadvantages: As the clock is usually a high-frequency signal, this distribution consumes a relatively large amount of power and dissipates much heat. Even the flip-flops that are doing nothing consume a small amount of power, thereby generating waste heat in the chip [12]. Again the maximum possible clock rate is determined by the slowest logic path in the circuit, otherwise known as the critical path. This means that every logical calculation, from the simplest to the most complex, must complete in one clock cycle. In spite of these drawbacks synchronous counters are more suited for some reasons.

At an asynchronous counter [11], [14] the output of any flip-flop (except the first) depends solely upon the output of the previous T flip-flop. Due to the RC time delay at each transistor there occurs a large aggregation of delay time after several flip-flops [8]. So to design asynchronous counter is impractical. For this reason synchronous logic has been adopted to construct counter blocks. In addition to this the synchronous technique serves greater throughput and much lower overhead for its design simplicity [9].

In the way to integrated circuit implementation process way can notice two major steps [3]: Design stage and fabrication stage. Design stage includes system design, logic design and mask layout preparation. At the system level design [4] the architecture is checked against the system specification to ensure that all required hardware features and data paths have been included. At the next level of hierarchy, the architectural blocks are expanded into logic

Author α : Dept. of Electronics and Communication Engineering Khulna University of Engineering and Technology,Bangladesh.
E-mail : robi@ece.kuet.ac.bd, jobayer.ece@gmail.com

diagrams. In this stage the whole system is transferred into aggregation of registers [9]. Here each item represents a particular logic function. If that particular logic functions are represented by logic gates such as AND, OR or XOR, then it is called Gate level design [6]. Gate level design realizes intensive aggregation of elements at much lower area. To solve the problems associated both with synchronous and asynchronous logic the author adopted a recently emerged logic structure GALS [1], [2]. Globally Asynchronous Locally Synchronous logic is the amalgam of the two logics. It not only removes the drawbacks but also provides more advantages [16]. The advantages include lower power consumption and electromagnetic interferences.

II. Overview of the Architecture

The digital clock designed as shown in Fig.1 assumes three functional blocks: second, minute and hour. The second and minute block count from 0 to 59. So six T flip-flops are required to construct either second or minute block (2^6=64). The hour block counts from 0 to 23. So it requires five T flip-flops (2^5=32).

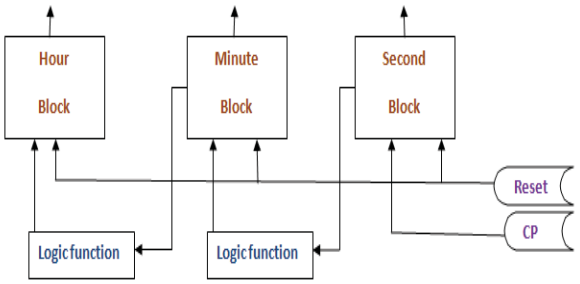

Fig.1 : simplified architecture of the design clock.

The flip-flops inside a block (second, minute or hour) run simultaneously as they are triggered by same clock pulse. But the clock pulse of minute block is a function of the outputs of the second block. Again the clock pulse of the hour block is also a function of the outputs of the minute block. So the block to block logical relation is asynchronous in nature. Thus the design architecture is a combination both of asynchronous and synchronous logic.

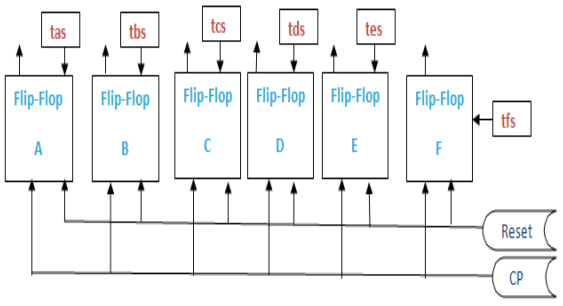

Fig.2 : Logic diagram of SECOND and MINUTE block

III. Model Development

There are three asynchronously operating blocks at the architectural design of the digital clock. But flip-flops at each block are energised synchronously. The SECOND and MINUTE block have six T flip-flops each. When they operate synchronously they are projected to have 64 distinct states. But we want them to go to their primary state after counting 60 states. So we need to modify the input and output relationships of flip-flops. Representing the input as Ta, Tb, Tc etc and A, B, C etc for flip-flops a, b, c respectively as shown in Fig.2, the relations for SECOND and MINUTE blocks are:

Ta=BCEF (A'D+AD')

Tb= ABCD'EF+CDEF (A'+B')

Tc =ABEFCD'+ DEF (A'+B'+C')

Td=EF (A'+C'+B')

Te= F (A'+B'+C'+D')

Tf =1

Similarly we want to make the flip-flops of HOUR block to go to its primary state after counting 24 states instead of 32 states. For this case the input-output relationships of the flip-flops are simplified as follows:

Ta= CDE (A'B+AB')

Tb=A'CDE

Tc=DE (A'+B')

Td=E (A'+B')

Te=1

Thus in the designed architecture sixty seconds make a minute and sixty minute an hour. After twenty four hour the clock resets and starts counting from initial states at another day. It is customary to keep a RESET button so that the user can reset the clock at any time.

IV. Operation

The individual block of the design is an aggregate of several synchronous binary counters. Therefore, the flip-flop in the lowest order position is complemented with every pulse. This means that its T input must be maintained at logic 1. A flip flop in any other position is complemented with a pulse provided all the bits in the lower order positions are equal to 1. As the input functions T's of the flip flops are configured, after the desired sequence (111011 for second and minute block) comes, all the outputs of the flip flops will be 0.

When the second block reaches to 59 (111011 in binary), all the flip flops of this second block resets. Then clock signal of minute block becomes 1. As Tfm =1 now logically, minute block state is increased by one at the next clock pulse. Thus each time second block faces state 111011, minute increases by one. The same thing occurs from minute to hour interaction. After

counting 23 hour (10111), 59 minute and 59 seconds all the flip-flops resets. As shown in Fig.3. Flow chart explaining the operation of digital clock.

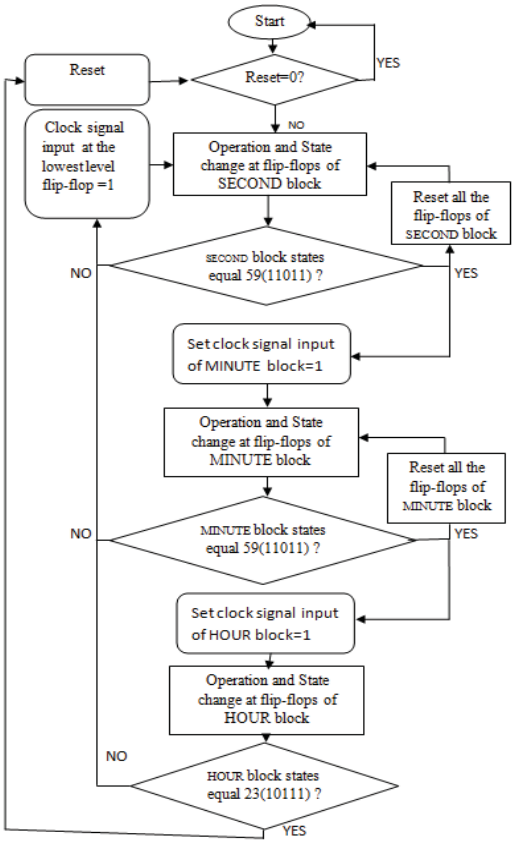

Fig.3 : Flowchart explaining the operation of digital clock.

V. Synthesis

The model is designed at Xilinx System Generator. Then it is synthesized with Xilinx Synthesis Tool (XST) as shown in Fig.4&5.

The outcomes include a IC package with two input ports: RESET and CLOCK PULSE and seventeen output ports. The RTL(Register Transfer Level) schematic of the design is provided as in Fig.6(a),(b),(c)&(d).It assembles logic gates which meet the systems requirements [6]. The details description of Pin numbers for the design of clock is given in Table.1.

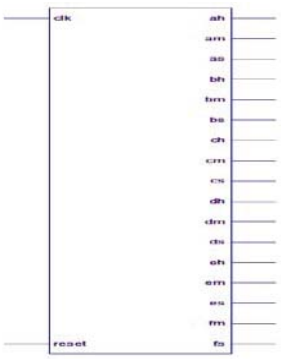

Fig.4 : RTL schematic diagrams found from XST (system level).

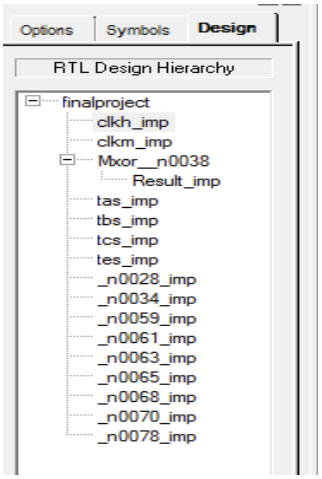

Fig. 6(a) : RTL Design hierarchy

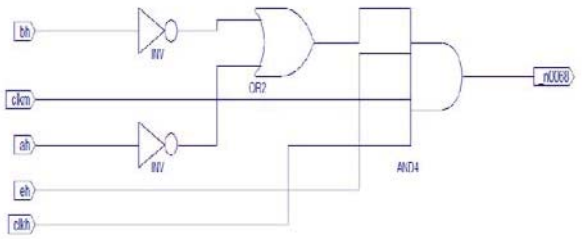

Fig. 6(b) : Gate level logic diagram showing net _n0068

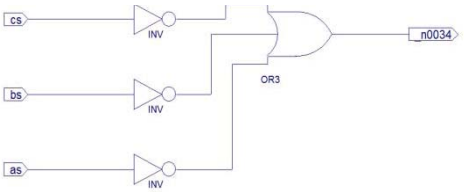

Fig.6(c) : Gate level representation of block FDRE.

Table.1 : Detail Description of the Pin Number Specification

Pin type	Pin name	Pin no.	Description	Function
Input	clk, reset	1,2	Single bit binary	clk is the line with input signal period=1second resets resets the clock to zero state
Output (Hour block)	ah,bh,ch, dh,eh	3,6,9,12, 15,	Single bit binary	Pins that jointly show time in hour
Output (Minute block)	am,bm,c m,dm, em,fm	4,7,10,13, 16,18	Single bit binary	Pins that jointly show time in minute
Output (Second block	as,bs,cs,d s,es,fs	5,8,11,14, 17,19	Single bit binary	Pins that jointly show time in second

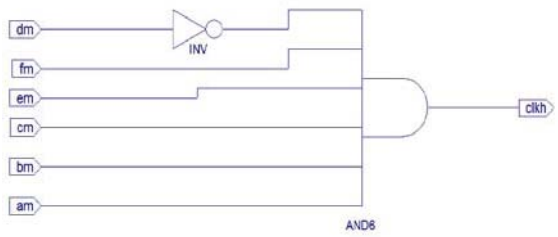

Fig.6(d) : Gate level logic diagram forming *clkh* signal.

A few portion of the total gate level representation is demonstrated in Fig.6(b), 6(c) and 6(d). It shows that all the components of the RTL schematic diagram are at gate level including AND, OR, INVERTER, XOR etc both at single and multiple inputs. The figure clearly demonstrates the interrelation among inputs and outputs.

VI. Simulation

The simulation of the design was run at verilolgger pro 6.5. The result was the exact replica of our expectation. From the timing diagram at Fig.7 we can notice that initially all the flip-flops are at initial state (zero state) when RESET is at state 0. The rest part of the circuitry remains inactive until RESET is at state 1. When RESET is at state 1 the flip-flops are allowed to follow counting. The state of SECOND block changes as 000000, 000001, 000010, 000011 and so on. When it reaches state 111011 (i.e. 59 in decimal), a clock pulse goes to MINUTE block and its state changes from 000000 to 000001 and the SECOND block starts counting again from 000000 state. Thus after 60 minutes when state 111011 appears at MINUTE block it resets and the state of HOUR block changes from 00000 to 00001. After counting 23 hour 59 minutes and 59 seconds, all the flip flops of the system get reseted (i.e. zero state) when the next clock pulse appears at the SECOND block.

VII. Limitations

The digital clock that is designed can count seconds, minutes and hours only. But at the real world people are not satisfied at this. They are interested in having notified other information such as date, month, year etc. It is also expected that the clock will serve some other facilities such as alarm, reminder etc. These features can be added just extending the design a little bit further. Again the design includes lesser number of gates. So it will be cost-inefficient to design on an entire chip. The author wishes to design a complete package of digital clock at the near future that will overcome the remaining drawbacks.

VIII. Conclusion

Logic gate level design of a digital clock has been presented. The design comprises the amalgam of synchronous and asynchronous techniques to attain its purpose. The Gate level design realizes intensive aggregation of components at smaller size of the chip. Again the combinational structure assumes lower power requirement, electromagnetic interference and greater throughput. The designed structure was synthesized using XST and simulated at verilogger pro 6.5. The design was successfully loaded at Xilinx FPGA device, MDA-ASIC2 (XC25150). In spite of having some limitations the design has been found to be useful enough.

References Références Referencias

1. A. Hemaini, T. Meincke, S. Kumar, A. Postula, T. Olsson, P. Nilson, J. Oberrg, P. Ellervee, "Lowering Power Consumpsion in Clock by using Globally Asynchronous Locally Synchronous Design Style". DAC 99, New Orleans, Louisiana (c) 1999 ACM 1-58113-109-7/99/06.
2. Jonas Carlson, Kent Palmnvist, Lars Wanhammar, "Synchronous Design Flow for Globally Asynchronous Locally Synchronous Systems". *www.es.isy.liu.se/publications/papers*

3. F.E. Barber, T. J. Bartoli, R. L. Freyman, J.A. Grand, J. Kane and Kershaw, "An Overview of the Silicon Very-Large-Scale-Integration Implementation". ©1981 American Telephone and Telegraph Company, The Bell System Technical Journal, vol. 60, No.7, September 1981, printed in USA.
4. Gordon M. Jacobs, Robert W. Brodersen, "A fully Asynchronous Digital Signal Processor using Self-timed Circuit" *Solid-State ircuits Conference, 1990. Digest of Technical Papers. 37th ISSCC., 1990 IEEE International* ***Issue Date:*** *14-16 Feb. 1990 . August 2002 .*
5. Mark E. Dean, David L.Dill and Mark Horowitz, "Self Timed Logic using Current-Sensing Completion Detection CSCD)", Journal of VLSI Signal Processing, 7, 7-16 (1994) © 1994Kluwer Academic Publisher, Boston, Manufactured in Netherland.
6. "Basic Logic Design with Verilog HDL: Gate Level Design on Combinational Circuits", lecture note by Chen-han Tsai, Chih-hao-Chao, Xin_Yu Shi, Bo-Yuan Peng and Bo-Yuan Peng.
7. M. Moris Mano, Digital Logic and Computer design. ©1979 by Prentice Hall.
8. Linda E. M. Brackenbury, "Design of VLSI Systems-A Practical Introduction".
9. Neil H. E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI design", third edition.
10. *en.wikipedia.org/.../Comparison_of_**synchronous**_and_asynchrono.*
11. *net.educause.edu/ir/library/pdf/EQM0848.pdf*
12. *en. wikipedia.org/wiki/Sequential logic*
13. *en. wikipedia.org/wiki/Synchronous_circuit*
14. *en. wikipedia.org/wiki/asynchronous _circuit*
15. *javascript.about.com/od/ajax/a/ajaxasyn.htm*
16. *en.wikipedia.org/wiki/Globally_asynchronous_logically_synchronous*
17. *www.educause.edu*
18. *javascript.about.com/od/ajax/a/ajaxasyn.ht*

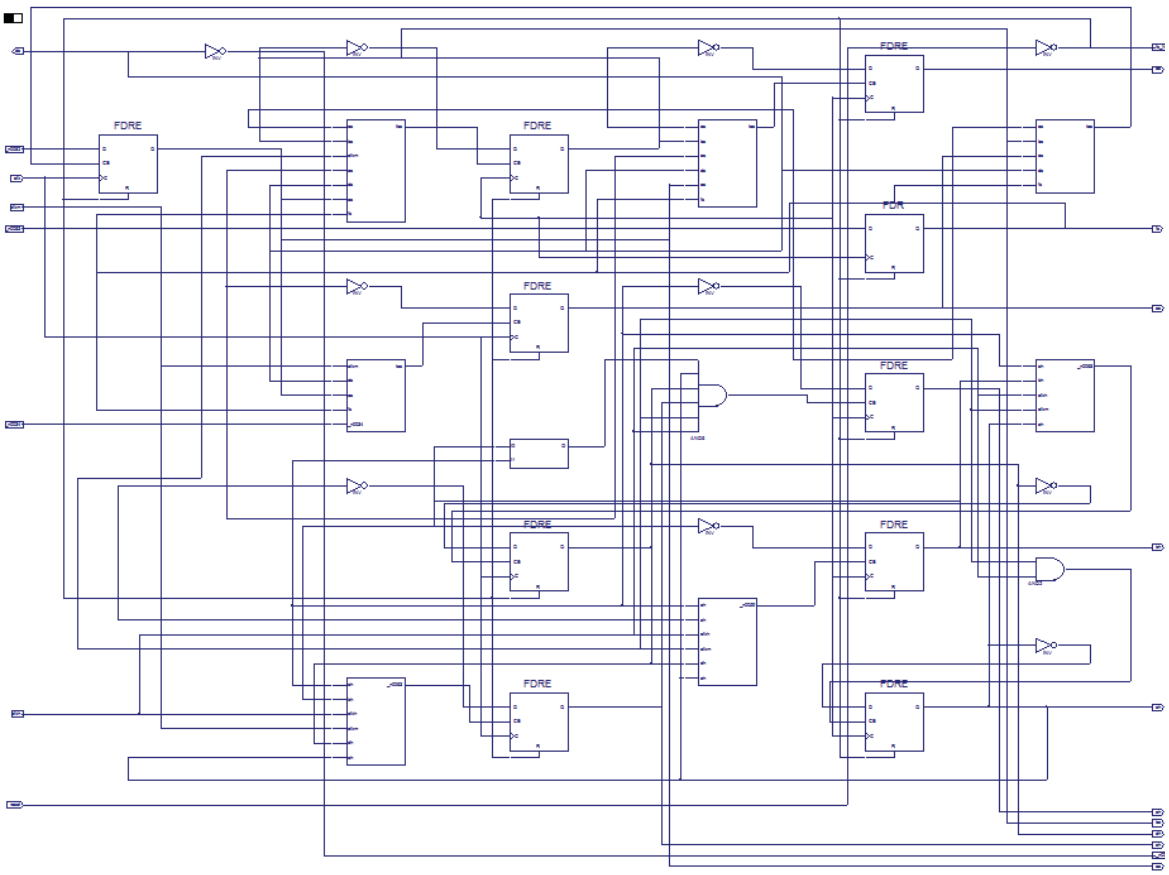

Fig.5 : RTL schematic diagrams found from XST (showing block level)

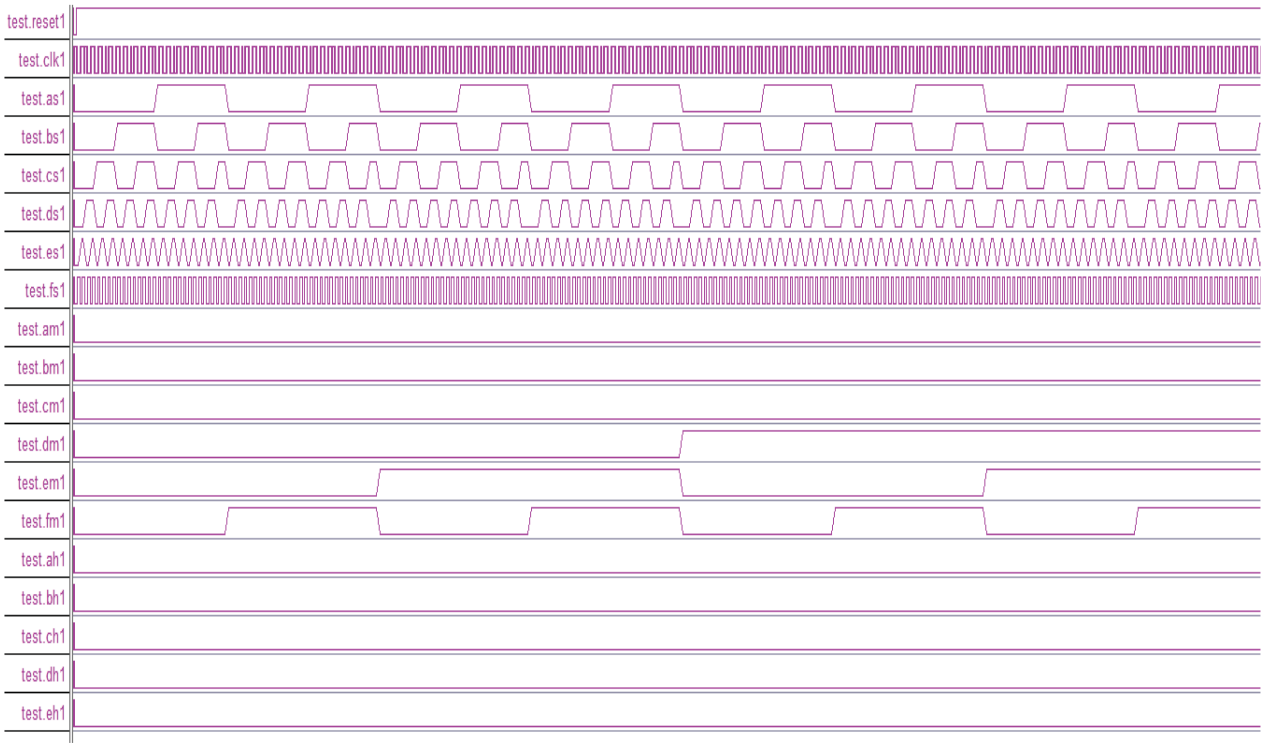

Fig.7 : Timing diagram simulated at Test bench.