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Electrical and Electronic Engineering

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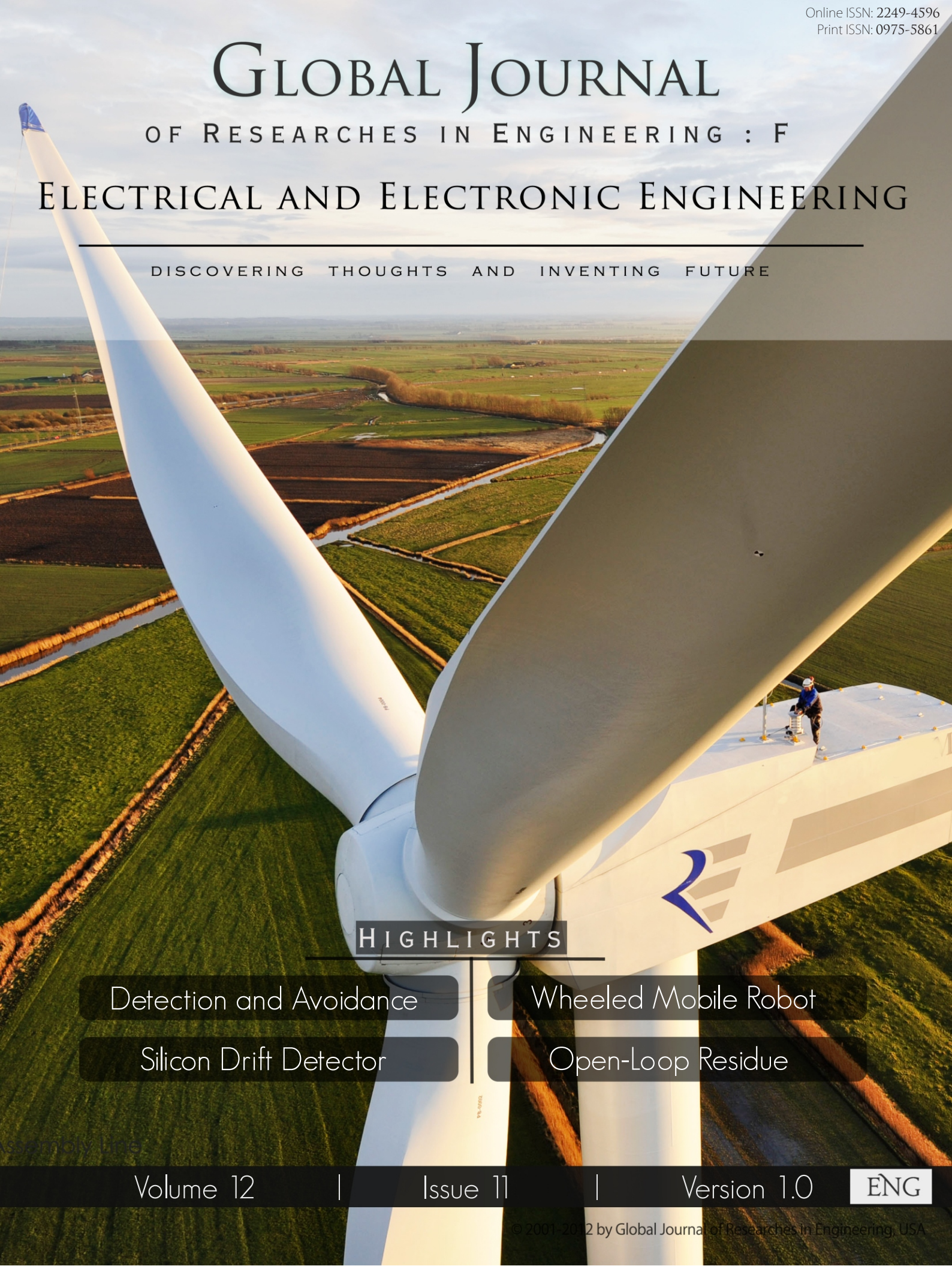

HIGHLIGHTS

- Detection and Avoidance
- Wheeled Mobile Robot
- Silicon Drift Detector
- Open-Loop Residue

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A First Principle's Approach to Study of the Silicon Drift Detector with Embedded JFET: Noise Analysis, Simulations & Analytical Modeling

By Pourus Mehta
Bhabha Atomic Research Centre

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GJRE-F Classification : *PACS : 85.30.-z, 85.30.De & 85.30.Tv*

Strictly as per the compliance and regulations of :

A First Principle's Approach to Study of the Silicon Drift Detector with Embedded JFET: Noise Analysis, Simulations & Analytical Modeling

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I. Introduction

Silicon drift detector (SDD) is a detector based on the principle of lateral charge transport within the bulk of a fully depleted detector, as proposed by Gatti and Rehak (Reference-1). SDDs are fabricated over high resistivity *n*-type substrate with *p-n* junctions on both top and bottom sides of the substrate. PN junctions on the top-side are segmented field shaping cathodes whereas the back-cathode is a uniform *p-n* junction. A reverse bias gradient is applied to the field shaping cathodes, which results in creation of a potential energy distribution in the shape of a "Potential Gutter" with its ultimate electron potential energy minimum at the anode. Electron-hole pairs are created by passage of ionizing radiation and get swept vertically across the parabolic potential along the depth and are focused at the local potential minima. They then get drifted along the lateral drift channel towards the anode. The noteworthy feature of the SDD is that its small output (anode) capacitance is independent of its large detector active area. SDDs are suitable for high resolution (127eV @ 5.9 keV for Mn-Kα line; Ketek Vitus SDD) and high count rate (~1x10^6 cps) X-ray spectroscopy applications. These detectors have found wide application in high-energy physics for tracking applications. SDDs have been incorporated in the ALICE detector experiment along the Large Hadron Collider at CERN. SDD's high-resolution capability can be further augmented by integrating the input device of the pre-amplifier (JFET) within the detector so as to avoid stray capacitance and microphonism. The integration of JFET onto the detector also facilitates better matching between detector and transistor capacitances/ impedances. The proto-typing stage fabrication of SDDs at IIT-B has been successfully completed (Ref. 5). Commercial grade SDDs have already been fabricated at BEL and have yielded satisfactory performance (Ref. 8). This paper gives a broad outline on the noise analysis, dc and dynamic TCAD simulations of the SDDs fabricated at BEL. An attempt has been made to model the static current-voltage characteristics of the SDD to predict the electrical behavior for various other kinds of SDDs fabricated at BEL.

II. Detector Design

Fig. 1(b) shows the 2D cross-section of the SDD of circular geometry with a cathode pitch of 120 µm {p+ cathode width (70µm) + Inter-strip gap (50µm)}. An n-type high resistivity (4 kΩ.cm) <111> orientation substrate of 300 µm thickness is employed to fabricate the SDD-JFET composite device. The peak concentration in p+ cathode region is approximated to be 1x10^{18} cm^{-3} with a gaussian distribution profile. Similarly, the back junction is also having the same concentration and profile. This version of SDD had an on-chip poly-resistor network for biasing the intermediate p+ strips together with an on-chip JFET for first level amplification [Fig. 1(a)]. This device had 20 p+ cathodes with two guard rings encircling its outer perimeter. The first, fifth, tenth, fifteenth, twentieth, and last p+ strips were individually biased whereas

Author : Bhabha Atomic Research Centre, Electronics Division, MOD Lab, Trombay, Mumbai 400085, India.
E-mails : pdmehta@barc.gov.in, pourus@cern.ch & pourus_m@yahoo.com

intermediate cathodes got biased through an on-chip poly-resistor network. Each poly resistor was designed to present a resistance of 102.4 kΩ (R_S=138.88 kΩ/□). The anode being an annular ring (radius = 50 μm) having area of 7.7 x 10^4 μm^2 which fetched an analytical full depletion anode capacitance of 27 fF for 300 μm thick fully depleted silicon wafer. The total detector active area of the detector was 2.31 x 10^7 μm^2. The embedded lownoise JFET (named as JFET-10) for this SDD design had the smallest channel length (15 μm) possible with BEL process [Fig. 1(c)]. For a designed channel length of 15 μm and the channel width of 172 μm, the analytical Transconductance (g_m) worked out to be 0.247 mS.

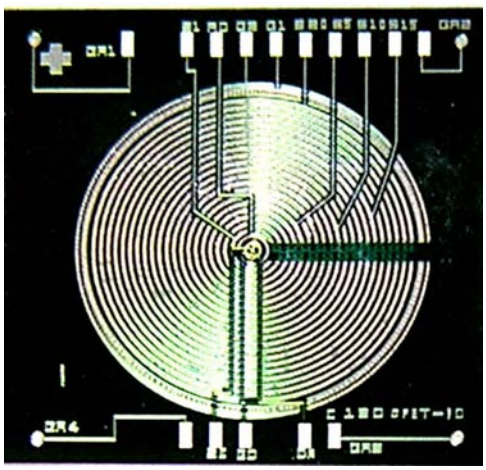

Fig. 1 (a) : Photograph of the completely fabricated SDD with in-built JFET.

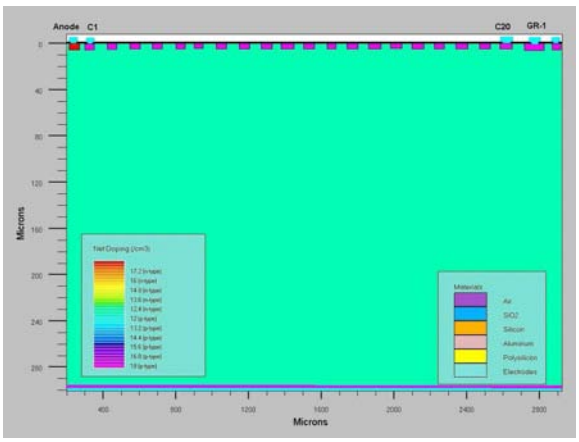

Fig. 1 (b) : 2-dimensional doping contours of the SDD (Pitch=120 μm).

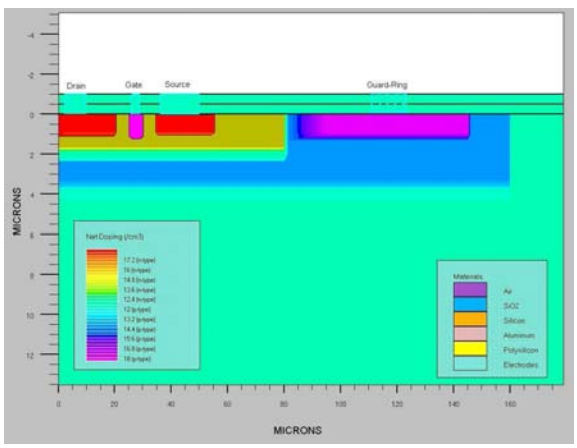

Fig. 1 (c) : 2-dimensional doping contours of the embedded JFET.

III. Noise Analysis

The Equivalent Noise Charge (ENC) has a strong dependence on the optimum shaping time (TM) (Equations 1-5) (Refer Spieler notes). It can be inferred from equations 1-5 that TM should be as small as possible to reduce the components of noise playing a critical role in the SDD & JFET system. It was found that for a particular value of Transconductance g_m and detector leakage current I_D, the optimum shaping time was least for a capacitance mismatch factor (h) of ~1. This means that the detector capacitance and JFET gate capacitance should not only be small but also nearly equal to each other. To prove this argument, a numerical simulation has been performed using values obtained from simulation of the JFET & SDD together. The plot in figure 2 shows the graphical representation of the relationship between optimum shaping time and mismatch factor. Figure 3 shows the mathematical relationship of the ENC on mismatch factor for the SDD-JFET system.

$$T_M = 0.65 \times \frac{1}{2} \times \left(\sqrt{h} + \frac{1}{\sqrt{h}} \right) \times \sqrt[3]{\frac{C_{FET}}{g_m}} \times \sqrt[3]{\frac{C_D}{I_{leak}}}$$

$$\text{Where } h = \frac{C_D}{C_{FET}} \quad \text{(Mismatch Factor)}$$

---- Eq. 1

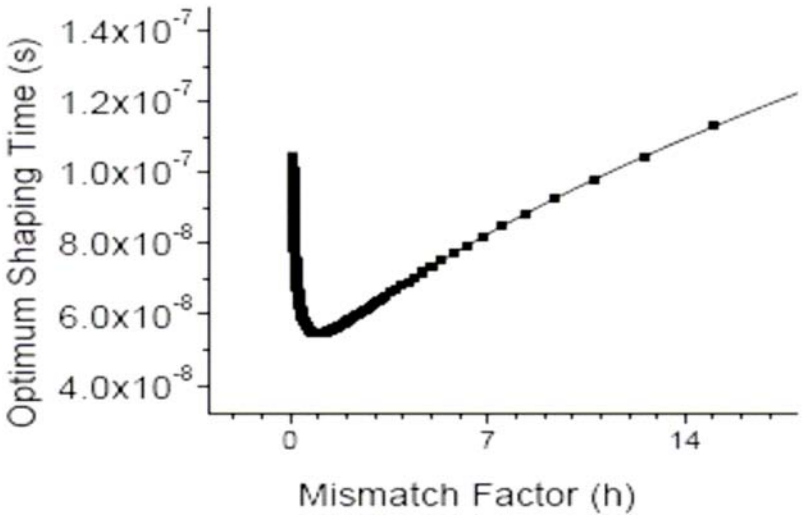

Fig. 2 : Optimum shaping time versus Capacitance mismatch factor.

a) Equivalent Noise Charge for Gate Current Noise (Ig)

As stated earlier the gate current is a source of noise in the JFET and its relationship with ENC is shown in equation 2. From the equation 2 it is also inferred that the gate current should be as small as possible to reduce the ENC_1 component of noise.

$$ENC_1 = \frac{e}{2q}\sqrt{q \times T_M \times I_g} \quad \mathbf{e} = 2.718,\ \mathbf{q} = \text{electron charge}$$

---- Eq. 2

b) Equivalent Noise Charge for Detector Leakage Current Noise (ID)

Similarly, it is seen from equation 3 that the detector leakage current should be minimum for reduction of ENC_2 component.

$$ENC_2 = \frac{e}{2q}\sqrt{q \times T_M \times I_D}$$

--- Eq. 3

c) Equivalent Noise Charge for feedback circuit

The noise due to feedback circuit can be minimized by choosing a very high value of feedback and bias resistors so as to make the effective parallel combination R_P large.

$$ENC_3 = \frac{e}{2q}\sqrt{\frac{2\times K\times T\times T_M}{R_P}}$$ --- Eq. 4

Where $R_P = \frac{R_B \times R_f}{R_B \oplus R_f}$

$R_P = R_B \parallel R_f$

R_B = Bias resistor

R_f = Feedback resistor

d) Equivalent Noise Charge due to JFET drain shot noise

This component can be minimized by having a small value for capacitances together with a high g_m.

$$ENC_4 = \frac{e}{2q}\times(C_D + C_F + C_{GS})\times\sqrt{\frac{4\times K\times T}{3\times T_M \times g_m}}$$ --- Eq. 5

Where C_D = Detector Capacitance

C_f = Feedback capacitor

C_{GS} = JFET gate-source capacitance

e) Net effective Equivalent Noise Charge

$$ENC^2 = ENC_1^2 + ENC_2^2 + ENC_3^2 + ENC_4^2$$

$$ENC = \sqrt{ENC_1^2 + ENC_2^2 + ENC_3^2 + ENC_4^2}$$ ----- Eq. 6

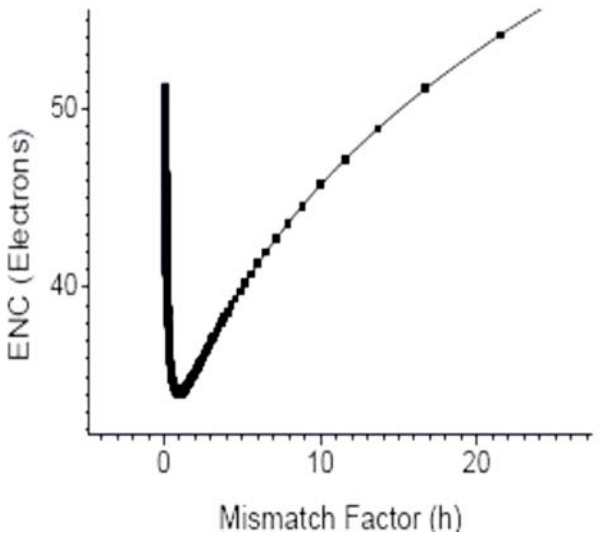

Fig. 3 : Equivalent Noise Charge versus Capacitance mismatch factor.

IV. Device Simulations

Three Dimensional device simulations have been carried out keeping a two fold approach in mind. Firstly, device simulations carried out for the static case (without application of any radiation) on the SDD-JFET composite device system. Secondly, to study the effect of application of incident radiation (X-ray photons; λ = 2 A°) on the performance curves of the SDD.

a) Static Case Simulations (Without application of Incident Radiation)

i. *Silicon Drift Detector*

The 2D cross-section of the SDD-JFET system [Fig. 1(b)] has been used as input to run a static case current voltage simulation. The 2D cross-section in figure 1(b) has been subjected to application of appropriate voltages and suitable boundary conditions were added to ensure that the solution to the poisson & continuity equations would converge. The biases were applied such that the anode was at a zero potential, cathode-1 was given -5 volts potential and cathode-20 at -100 V. The intermediate cathodes got biased through the on-chip poly-resistor network. This peculiar biasing develops a potential distribution resembling a gutter (Ref. 4). The one dimensional potential along the depth is parabolic in nature. This leads to confinement of electrons generated by photo-electric absorption of incident photons. The photoelectrons are first concentrated within the minima along the depth and then drifted along the horizontal channel towards the anode where they ultimately get collected. The above biasing scheme results in an electric field of 370 V/cm. Corresponding to the field strength & an Electron Mobility of 1350 cm^2/ V.s at 300°K, Electron Drift Velocity works out to be 5 × 10^5 cm/s. This implies a detector response time (Drift Time) of around 100 nano seconds for a drift distance of around ~500 µm. Value of resistance of poly-resistor was fixed at 100 kΩ for *W* = 120 *µ*m & L = 80 *µ*m, which corresponds to a total resistor chain current of around 65 *µ*A under these biasing conditions. The simulated detector anode (output) capacitance at full depletion is around 200 femto Farad which is flexible enough to play with and tune with the integrated transistor's capacitance.

Fig. 4 shows the leakage current of the detector as a function of reverse bias applied to cathode C-20 whereas figure 5 gives the C-V characteristics of the simulated SDD structure respectively. As the reverse bias is increased, the depletion region extends as function of $\sqrt{V}$ from both sides of the device. The capacitance decreases to significant low value during initial reverse bias of -5 V when the depletion region from first strip touches the n^+ anode. Further increase in reverse bias continues to deplete the bulk (and reduce the capacitance) till full depletion is reached at -30 V. Beyond this bias anode capacitance saturates to a low value corresponding to a parallel plate capacitor of area that of anode and spacing between the plates being the detector thickness.

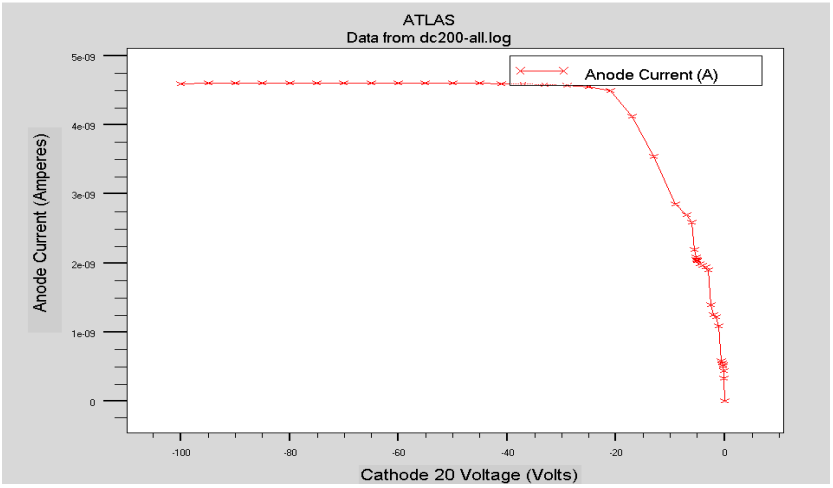

Fig. 4 : Anode current versus last cathode (C-20) voltage.

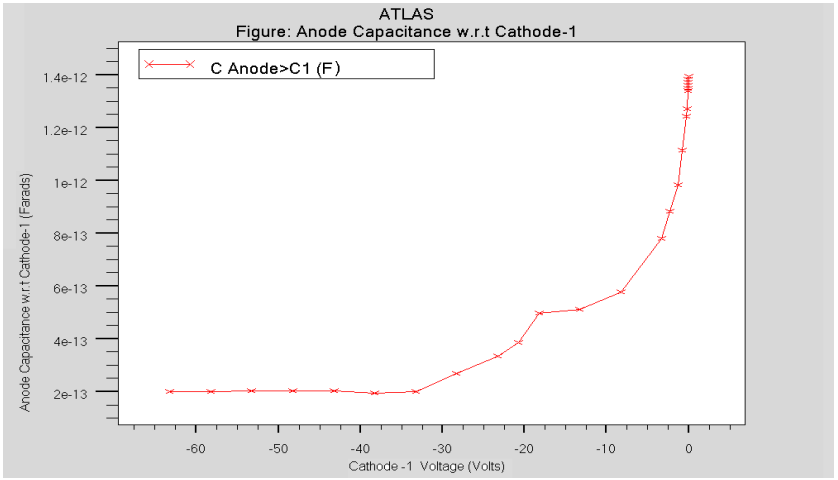

Fig. 5 : Anode Capacitance versus Cathode-1 voltage.

ii. *Junction field effect transistor (JFET)*

The virtual SDD-JFET detection system was again ported to the device simulator and device characteristics of the JFET alone were studied. The JFET was biased in common source configuration with the source at 0V and drain voltage of 30.5V and gate voltage varied from 0V to –20V (Transfer characteristics illustrated in figure 7). Fig. 6 shows the I_D-V_{DS} (Drain) of the JFET having gate width of 172 μm. The gate pinch-off voltage is V_{GSOFF} = -6 V with a saturation drain current of ~6 mA (Fig. 6). The extracted Transconductance at I_D = 5 mA and V_{DS} =30 V is g_m = 1.7 mS. The slope of the I_D-V_{DS} curve in the saturation region corresponds to an output resistance of 18 kΩ. The extracted gate leakage current was 1 pA at operating conditions, which would be significantly small as compared to leakage current of the detector (4.5 nA). This ensures that the shot noise contribution due to gate current is negligibly small as compared to the one associated with the detector leakage current. It was observed that the transistor does not breakdown even at V_{DS} = 42 V. The gate capacitance is in such a range that output capacitance of the SDD can be matched to get optimal results.

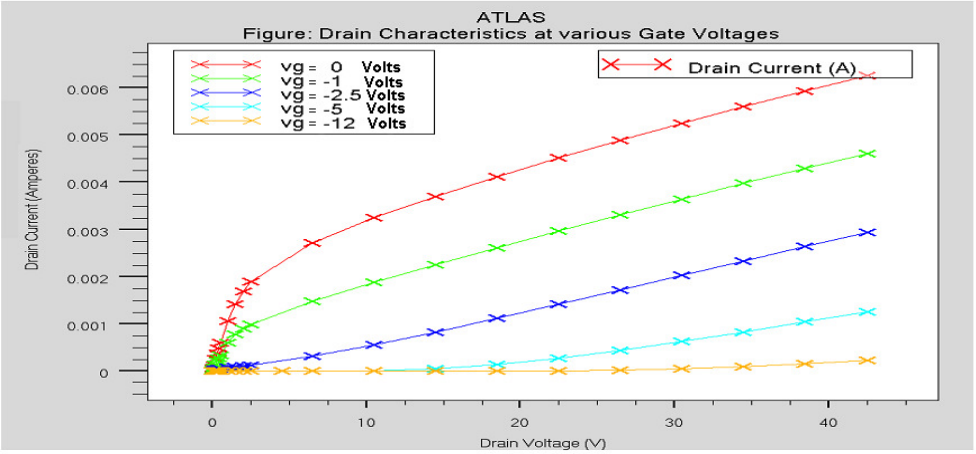

Fig. 6 : Drain Characteristics of embedded JFET.

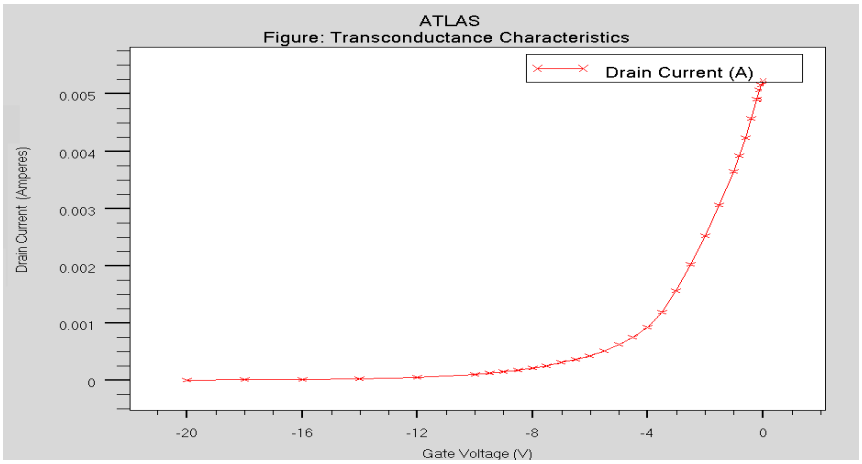

Fig. 7 : Transfer Characteristics of embedded JFET.

b) Dynamic Case Simulations of SDD-JFET composite system (with application of incident radiation)

The SDD - JFET system described in fig 7 has been subjected to an X-ray beam ($\lambda = 2$ A°) through a 10 μm wide slit. This was done to emulate a point source of light instead of a uniform shower to accurately estimate the drift time. Since the nuclear pulses are of short duration (nano seconds say) the simulated X-ray beam was a Gaussian with rise time of 0.1 ns and fall time of 0.4 ns. The beam intensity was fixed at 1 W/cm^2 as the beam aperture was only 10 μm wide, the actual optical power in this case turns out to be only 1 μWatt for an incidence area of 10 x 10 μm^2. The resultant anode current was extracted as a function of transient time, which gave a Gaussian current pulse (Equation-7) with the rise time depending upon the distance from the point of incidence on the detector. Simulations were performed for X-ray incidence distances of 500, 1000, 1500, 2000 and 2200 μm from the anode, and the current pulses at the anode were extracted. It was found that the current at the anode was delayed and rise times increased with increase in the distance of the X-ray incidence point from the anode. Drift times varied proportionately with the drift distance thus maintaining drift time to drift distance linearity. Alternatively, it was also found that the current pulse at the anode experienced significant broadening due to diffusion of the charge cloud. This effect is incremental with increase in drift distance from the anode. The net deposited charge (0.24 femto-Coulomb) always remains conserved in all cases. This dynamic simulation helped in accurate estimation of pulse timing and height characteristics. This helped in designing the latter end of the instrumentation chain like pre-Amplifier, shaper etc.

Additionally, a simulation was also performed in which both the SDD and JFET were biased in such a way that the anode of the SDD was shorted to the gate of the JFET and the combined node was connected to a resistor of 100 k Ohm and the other end of the resistor was connected to ground potential. This ensured that the anode current would be dropped across the resistor and this voltage drop would be fed to the gate of the JFET, which in turn would result in a dynamical change in the drain current (ref. Fig. 8). This ensures that the small change in the anode current would be amplified by the transistor to give a large change in the drain

current. In this simulation the rest of the SDD biasing remained same and the drain bias was fixed at 30 Volts through a bias resistor of 10 kΩ for a source bias of zero volts (common source configuration).

$$I = \frac{I_o}{\sigma\sqrt{2\pi}} e^{\frac{-(x-x_o)^2}{2\sigma^2}} \quad \text{--- Eq. 7}$$

Where

I_o = Maximum anode leakage current

x_o = Drift distance

σ = Width of current pulse

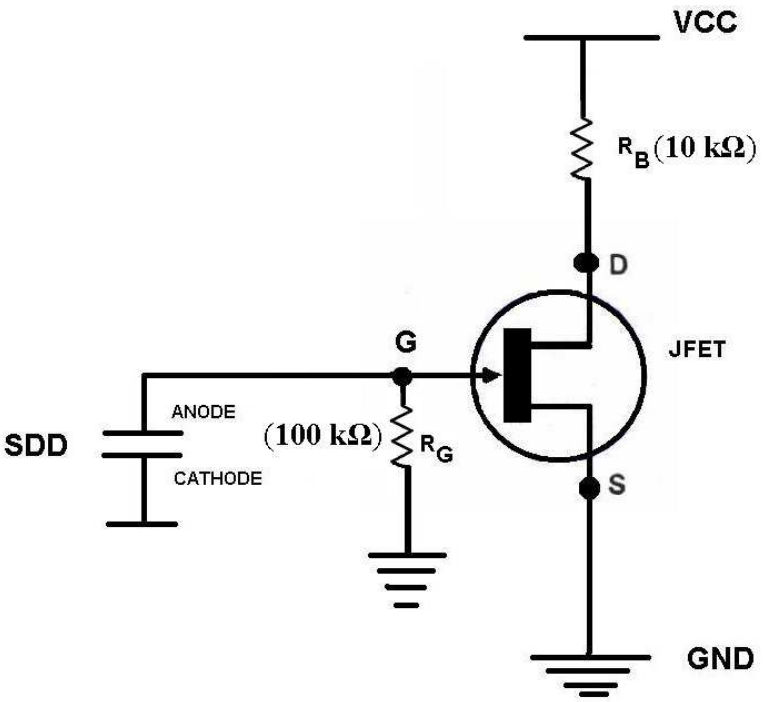

Fig. 8 : Circuit showing parasitics modeled in simulation.

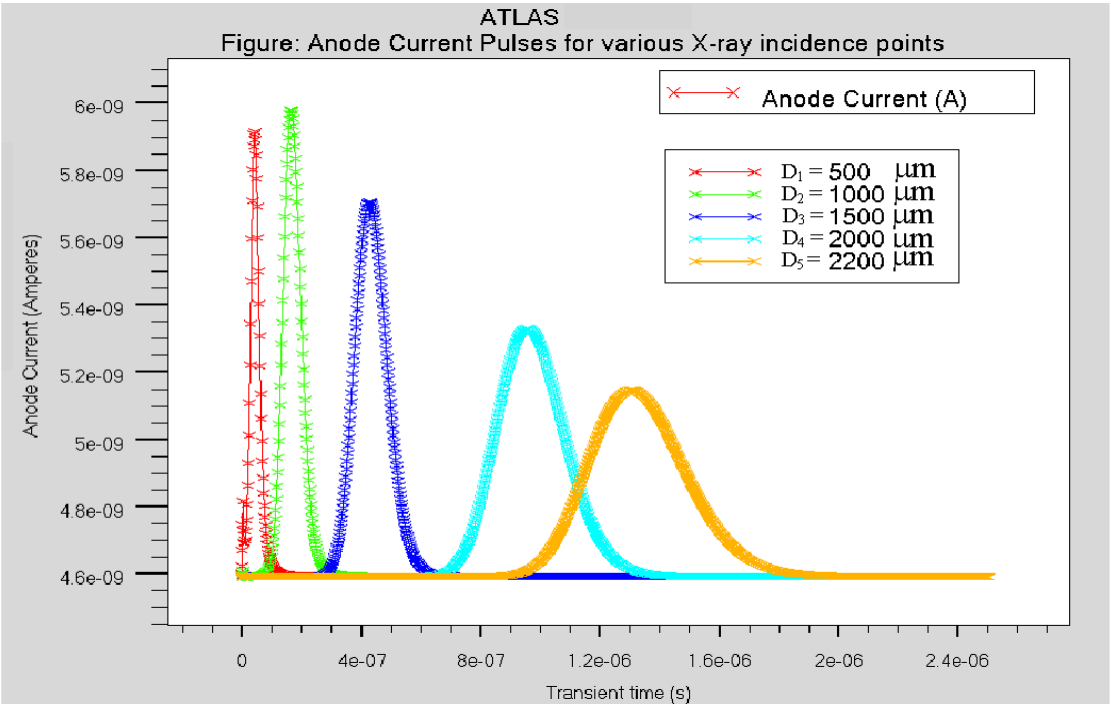

Fig. 9 : Dynamic current characteristics of the SDD.

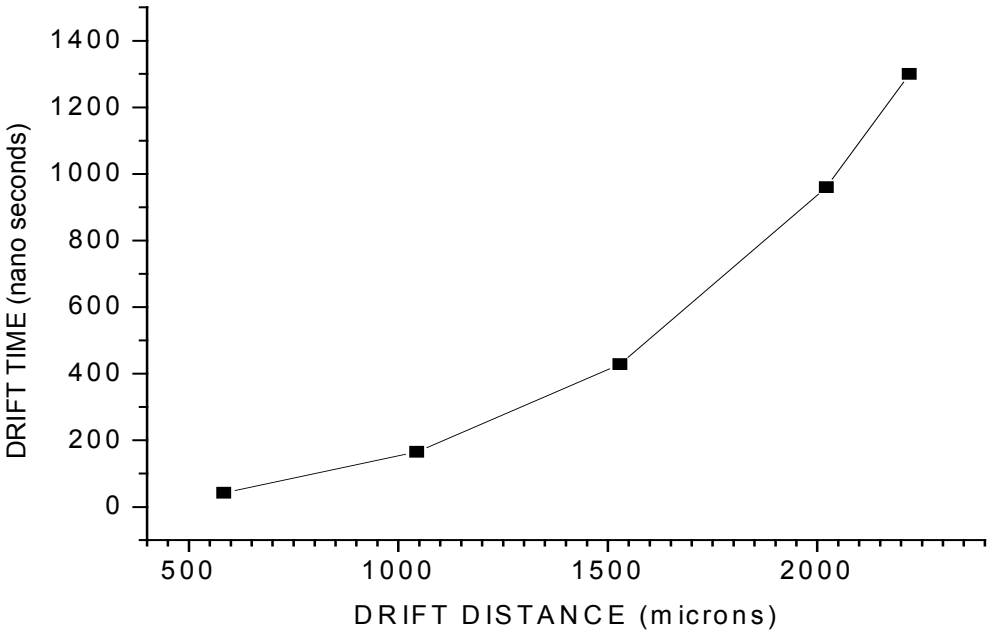

Fig. 10 : Drift time versus drift distance relationship in SDD.

V. Analytical Modeling Of SDD I-V Characteristics (Static Case)

I-V characteristics of the SDD have been analytically deduced to predict the leakage current behavior for various other designs fabricated at BEL. The values of the constituent parameters of equations 8 & 9 have been enlisted below in Table-1. The I-V curve resulting from the equations 8 & 9 has been illustrated in figure 11. As seen from the curve, the saturation behavior is similar to the one derived from simulation. The deviation of the saturation anode current derived from simulation from that achieved from I-V model is merely 4.8 %. This small value of deviation in saturation current shows that the model is fairly successful in predicting the behavior of the SDD's I-V characteristics.

$$I_R = J_s A\left|\left(1-e^{\left(\frac{qV}{\alpha KT}\right)}\right)*\left(e^{\frac{qV}{KT}}-1\right)\right| \text{------Amperes}$$

---- Eq. 8

α = Constant = 200 (depends on surface recombination velocity)

$$J_s = q\left(\sqrt{\frac{D_p}{\tau_p}}\frac{ni^2}{N_D}+\sqrt{\frac{D_n}{\tau_n}}\frac{ni^2}{N_A}\right);\ \text{Js} = 1.75\ \text{x}10^{-8}\ \text{Amperes/cm}^2$$

----- Eq. 9

Table 1 : Tabular form listing the values of constituent parameters of the Equations 8 & 9.

Sr. No.	Parameter	Symbol	Value
1	Total leakage current at anode	I_R	
2	Leakage current density	J_S	$1.75\ \text{x}10^{-8}$ Amperes/cm^2
3	Detector Active Area	A	0.27 cm^2
4	Boltzmann constant	K	$1.38\ \text{x}10^{-23}$ J/^{o}K
5	Electronic charge	q	$1.6\ \text{x}10^{-19}$ Coulombs
6	Ambient Temperature	T	300 ^{o}K
7	Applied reverse bias	V	0 to -100 Volts
8	Constant	α	200
9	Diffusion coefficient for Holes	D_P	12 cm^2/s
10	Diffusion coefficient for Electrons	D_n	36 cm^2/s
11	Hole Lifetime	τ_P	$1\text{x}10^{-5}$ s
12	Electron Lifetime	τ_n	$2\text{x}10^{-3}$ s

13	Intrinsic carrier concentration (300 ^{o}K)	n_i	$1x10^{10}$ cm^{-3}
14	Donor concentration	N_D	$1x10^{12}$ cm^{-3}
15	Acceptor concentration	N_A	$1x10^{18}$ cm^{-3}

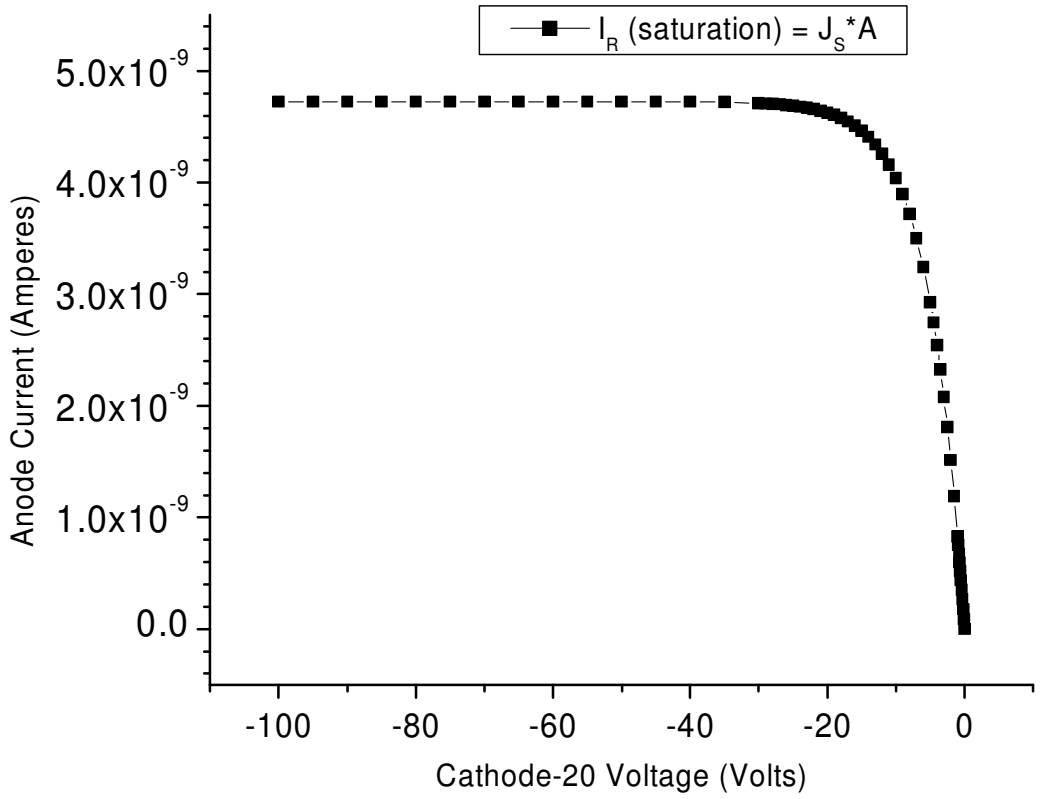

Fig. 11 : I-V Characteristics of SDD derived using I-V model.

VI. Conclusions

Noise analysis revealed the optimum value of capacitance mismatch factor (h) between SDD and JFET capacitances to be ~ 1. The relationship of shaping time with mismatch factor was found to be parabolic with minima at the optimum mismatch value. The net ENC too was found to be minimum at the optimum mismatch value. The full depletion anode capacitance derived from simulation was 200 fF for a full depletion voltage of -30V. The saturation value of anode leakage current was 4.5 nA. The transconductance derived from I-V simulation of the embedded JFET was 1.7mS for a gate pinchoff voltage of -6V. Dynamic simulations revealed the near linear dependence of drift time on drift distance within the SDD. Analytical modeling of the SDD's I-V characteristics showed a deviation of 4.8% in saturation anode current values achieved from simulation and analysis.

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Building Algorithm for Obstacle Detection and Avoidance System for Wheeled Mobile Robot

By Chigulla Leela Kumari
Raipur Institute of Technology, Raipur

Abstract - Nowadays, Wheeled Mobile Robots (WMRs) are built and the control system that used to control them are made by Electronic Engineers. Depend on their desire design of WMR, Technicians made used of Microcontrollers as controlling machines and DC Motors for motion control. Autonomous robotic vehicle guidance for indoor navigation has been developed for Mobile Industrial Robot model. The resulting design will navigate the environs in a building without the need of human intervention. The guidance system consists of infrared sensors for obstacle detection, range determination and avoidance. It can detect the obstacles within the range 10 to 30 cm. This paper represents mainly on software implementation of obstacle detection and avoidance system for Wheeled Mobile Robot. This system consists of infrared sensors and microcontroller. In this system three infrared sensors are used for left, front and right. In this robot system, the input signal is received from sensor circuit and Atmega 32 microcontroller is operated according to the received sensor's signal. The infrared sensor reading is taken and processed to avoid the obstacles. The 12V power supply is used to operate Atmega 32 board and sensor circuit board.

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I. Introduction

ROBOTS are now widely used in many industries due to the high level of performance and reliability. All mobile robots feature some kind of obstacle avoidance. Designing autonomous robot requires the integration of many sensors and actuators according to their task. Obstacle detection is primary requirement for any autonomous robot. The robot acquires information from its surrounding through sensors mounted on the robot. Various types of sensors can be used for obstacle avoiding. Methods of obstacle avoiding are distinct according to the use of sensor. Some robots use single sensing device to detect the object. But some other robots use multiple sensing devices. The common used sensing devices for obstacle avoiding are bump sensor, infrared sensor, ultrasonic sensor, laser range finder; charge-coupled device (CCD) camera web cam and so on can be used as the detection device. Among them infrared sensor is most suitable for this obstacle avoiding robot because of its low cost and ranging capability. The IR object detection system consists of LM358N operational amplifier with a pair of infrared led and photodiode. This system is a compact, self-containedIR ranging system incorporating an IR transmitter, receiver, detection, and amplification circuitry. The unit is highly resistant to ambient light and nearly impervious to variations in the surface reflectivity of the detected object. The paper is mentioned on the basic research of "Development of an Intelligent Wheeled Mobile Robot (WMR)". This is a type of IR Sensors based Wheeled Mobile Robot and it mainly function as an Obstacle Avoidance Vehicle. It is mainly focus to software implementation of this WMR.

II. System Overview

This mobile robot is designed to explore in the environment by detecting obstacles and avoiding collision base on the distance measurement information obtained from the infrared sensors. This robot system is obstacle avoiding robot using infrared sensors. Infrared sensor senses the obstacle along its path. In this system three infrared sensors are used for left, right and front. The Infrared sensors, used for obstacle avoidance, are connected to the processor via analog ports. The input signal is received from sensor circuit and ATMEGA32 is operated according to the received sensor's signal.

The reason to choose IR sensors as Obstacle detected device is that to determine the range of object and by this data, to control the Obstacles avoiding process. Analog to Digital Converting (ADC) process is done in ATMEGA32 by software and these data used to control the require outputs that will effect to the second Module, Navigated Control System. The basic circuit that makes these processes is shown in Figure 2.

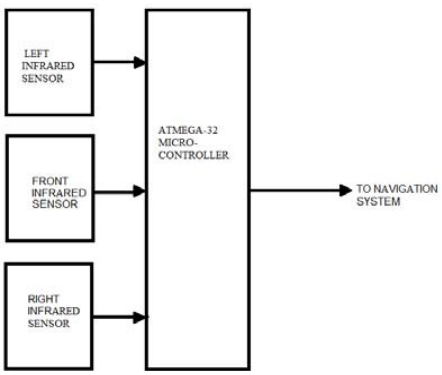

Fig.1 : Block Diagram of Obstacle Detection and Avoidance System for Wheeled Mobile Robot

Author : M.E, Power Electronics, Raipur Institute of Technology, Raipur. E-mail : leelakumari01@yahoo.in

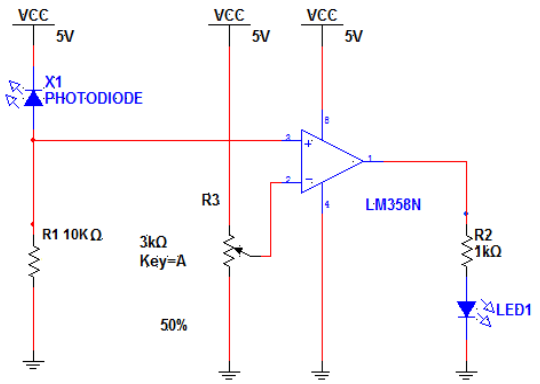

Fig. 2 : Infra red sensor circuit applied to ATMEGA32

Using the input signals from sensor circuit, the navigation system determines a direction to avoid the obstacle. After turning a suitable angle, the navigation system negotiates the robot to the desired direction and check whether there is an obstacle along its way. According to the sensing information, microcontroller controls the driver unit. And then, the driver unit drives the robot's wheels individually.

III. Infra Red Sensor

In this paper, three infrared sensors are utilized for distance measurements. The infrared sensor consists of a LED emitting the infrared light and a photo diode. This sensor enables to detect objects without any influence on the color of reflective objects, reflectivity, the lights of surroundings. Maximum range that can be detected is from 10 to 30 cm. It generates an analog voltage that is a function of range. The output voltage can be measured by an analog-to-digital ADC input line. It has three wires, positive (+5V), negative (ground), and data output.

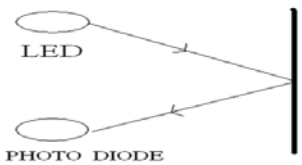

Fig. 3 : IR Sensor

IV. Analog-To-Digital Converter and Sensor Accuracy

Distance sensors are typically not read at a rate of more than a few samples per second, so the performance characteristics of most ADCs will be sufficient. Assuming that the noise on the Vout input signal has been kept to a minimum, the main concern is to ensure that the number of bits used for the ADC output is sufficient for the desired resolution. The change in voltage from 70 cm to 80 cm is only about 0.06 V, which corresponds to 0.006 V/cm. If the 8-bit ADC with a reference voltage of 5V is used, each bit of the ADC output represents 0.0195 V which means a one bit swing in the ADC output will result in a distance swing of about 3 cm. The maximum voltage output from a IR sensor is about 3V. If the reference voltage for the 8-bit ADC is changed to 3V, each bit of the ADC output represents 0.0117 V, which means a one bit swing in the ADC output will still result in a distance swing of about 2 cm. The resolution is better at shorter distances because there is a larger voltage change.

V. Circuit Operation Of Obstacle Detection And Avoiding System

This IR range sensor produces voltage signal when the photo diode conducts due to reflection of IR rays. The emitter emits a pulse of IR light. This light travels out in the field of view and either hits an object or just keeps on going. In the case of no object, the light is never reflected and the reading shows no object. If the light reflects off an object, it turns to the detector and creates a triangle between the point of reflection, the emitter, and the detector. The angles in this triangle vary based on the distance to the object. The triangle described above. It is an analog infrared proximity sensor. It can be used to detect obstacles. This sensor has a LED that emits infrared light. Infrared light has the interesting property that it bounces on obstacles. On the front of the sensor, beside the LED that emits the infrareds, there is a photodiode that is sensible to infrared light. It will vary the output voltage based on the amount of infrared light that bounces back to the sensor. The more infrared light it sees, the closer is the object and the higher the output voltage generated by the photodiode. This sensor will provide an analog output voltage that is promotional to the distance of the object it senses. It's analog output will then be fed into the analog-to-digital converter of the microcontroller, via its pin.

If the voltage output is connected to a microcontroller with analog to digital conversion capability (such as a ATMEGA32 microcontroller), it is possible to translate this voltage to a numerical value. This value can be used to determine whether or not there are obstacles close to the sensor and how far these obstacles are. Figure 4 shows how to interface a microcontroller to a sensor.

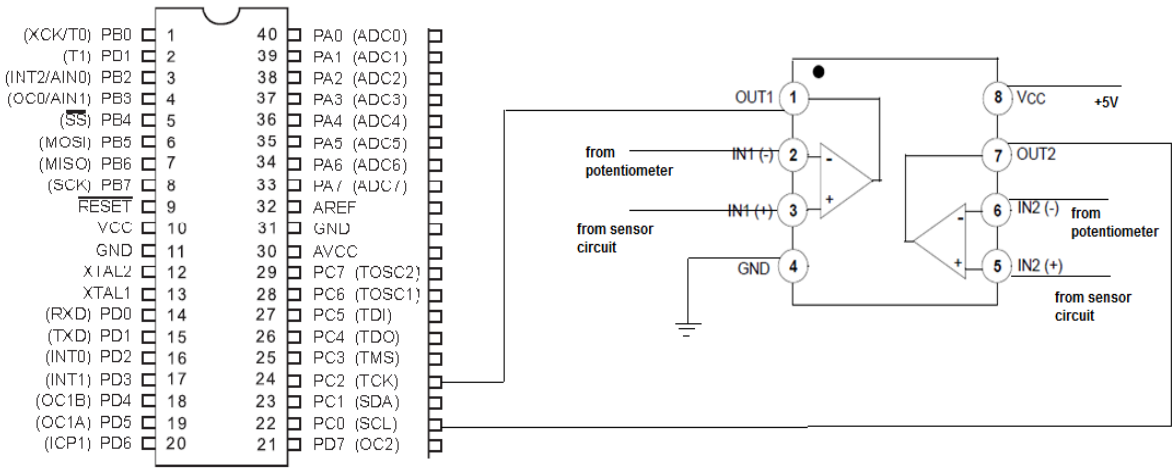

Fig. 4 : Interfacing ATMEGA32 with sensor circuit.

VI. Sensing Statements

The sensing in mobile industrial robot relies mostly on infra-red light (IR) detectors, either for obstacle and goal area detection, although a few robots used ultrasound distance detectors. Obstacles are detected with proximity sensors. To detect obstacles teams usually use IR sensors, although a few robots used ultrasound sensors operating as sonar's, based on pulse reflection and time of flight.

Obstacle detection is active in the sense that the robot emits IR light, and looks at the reflection received by the detectors. This allows a gross measure of the distance of a given obstacle, as the output voltage increases with the intensity of the modulated IR light (at 40KHz) received by the detector, which is inversely proportional to the distance between the robot and the obstacle. The voltage/distance relationship is approximately quadratic. Obstacle detection typically uses 3 of infrared sensors. To improve detection efficiency, the use of more than one IR LED/sensor is in order to better illuminate the detection area. In some robots the obstacle detection was also improved using more than 3 sensors. It uses the triangulation principle to compute the distance between the sensor and the obstacle being useful in the range 10-30 cm. Reliable obstacle avoidance is an essential feature. The simplest way to avoid obstacles is to use at least two noncontact (IR or ultra-sound) proximity sensors looking left and right. Detecting an object on the left side of the robot makes it turn right and vice-versa. This can be done by simple proportional control, using directly the output of the sensor, or by quantizing the sensor value in a few discrete levels (close, medium-range and far). However, most of the robots used at least 3 obstacle sensors with one facing the robot front. This improves obstacle detection area while maintaining the capability to detect obstacles in front. In this case, use of randomization can also be useful. By not turning always to the same side when facing a frontal obstacle, chances of developing vicious cyclic behaviors are reduced.

VII. Software Consideration Of Obstacle Detection And Avoiding System

The consideration data of IR Sensor that mentioned the graph comparing between its voltages depend on the distance of the detected object is shown in Figure 6. For assembly software program consideration for microcontroller, the following step by step consideration should be made.

- Three inputs from three sensors are to be converted as digital data of microcontroller input.
- These data must be represented as input bits of control system that can determine which sensors are detected and which position of Robot is require rotating.

a) Software Consideration of Navigated Control System

The input and output consideration of this Module can be seen clearly as shown in Table I.

STATE NUMBER	INPUT DATA	DETECTED SENSORS	DECISION TO WMR	OUTPUT DATA
1	000	NONE	straight	1001
2	001	3	Left	0001
3	010	2	Right	1000
4	011	2,3	Left	0001
5	100	1	Right	1000
6	101	1,3	straight	1001
7	110	1,2	Right	1000
8	111	1,2,3	Back	0110

Table 1

b) Consideration of Rules for Obstacle Avoiding and Navigating

i. *Path predetermining state*

The system must be pre-limited for going straight distance, turning left or right and returning back straight to the starting point for no obstacles condition.

ii. *Obstacle avoiding state (obstacle is detected at the front)*

Table I Outputs from Navigation System depend on its Inputs. The system must be stop for a while. It must turn to the left and check if there is any obstacle or not in this turning state. And then it will return to right and go straight at normal line.

c) Obstacle is detected at the left

Stop for a while whether one or both left sensors are detected. The system must turn to right and check if there is any obstacle or not in this turning state. It must return to left and go straight at normal line.

d) Obstacle is detected at the right

The system must be stop for a while whether one or both right sensors are detected. It must turn to left and check if there is any obstacle or not in this turning state. And then it will return to right and go straight at normal line.

VIII. Experimental Results

For Obstacle detection part, the result of data confirming of IR sensor is shown in Figure 2.The main consideration result of this Control System, Navigational Consideration is made as shown in Table I. The experimental results of the Modeling and SIMULNK procedures of Motor Drive System are shown in Figure 5 and Figure 6. This Figure shows the result of analyzing the DC Motor internal circuit that it is suitable to use or not using MATLAB. And the Experimental results of Control System testing circuit for this process are shown in Figure 6.

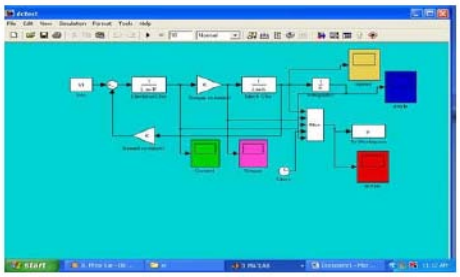

Fig. 5 : DC motor model created in MATLABSIMULINK

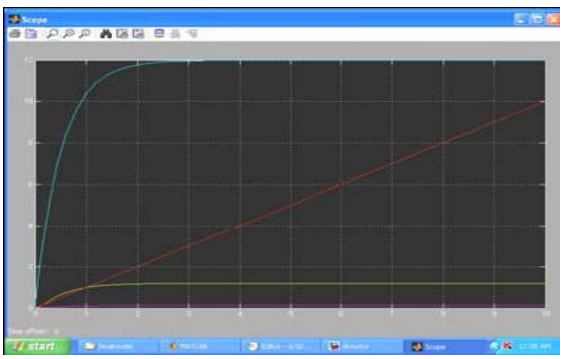

Fig. 6 : Output of all ratings

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Firstly the author would like to thank her parents: ***Chigulla V.K. Rao and Chigulla Padma Vati*** from R***aipur***, C.G. for their best wishes. **Ms.Dh*aneshwari Sahu,*** *her guide* will also get the author's great thanks for her special guidance to pay chances. The author greatly expresses her thanks to all persons whom will concern to support in preparing this paper.

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Design and Implementation of Low Power 12-Bit 100-MS/s Pipelined ADC Using Open-Loop Residue Amplification

By Appa Rao M., Dr. Ramana Reddy P. & Cyril Prasanna Raj P.
JNTUA College of Engineering. Ananthapur

Abstract - In this paper a high speed, low power 12-bit, analog-to-digital converter in CMOS 0.13 micron technology that makes it suitable for UWB is designed and implemented. For designing the particular ADC a bottom up hierarchical method is adopted. First according to the specification, the design of aspect ratio of the transistors used in our design is done. There were many challenges throughout the design process, including determining the matching requirements of the devices, investigating what percentage of segmentation to be used to design the whole system. For checking the functionality of the whole system a spice code is written using HSPICE by defining all blocks in the circuit as sub circuits. Then a schematic capture is done using schematic composer from virtuoso stating from bottom level to top level. Finally the layout for the complete ADC is done using Electric Layout editor. A 12-bit pipelined ADC that can operate at maximum frequency of 100 MSPS, and power consumption less than 70mW is designed and implemented.

Keywords : *Multi-stage, high Speed, high Accuracy, Low power, low voltage, ADC, CMOS.*

GJRE-F Classification : *FOR Code: 090699*

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I. Introduction

Many and the communication systems today digital signal processing (DSP) to resolve the transmitted information. Therefore between the received analog signal and DSP system an analog-to-digital interface is necessary. This interface achieves the digitization of received waveform subject to a sampling rate requirement of the system. Being a part of communication system, the low power constraint mentioned above the A/D interface also needs to address to the low power constraint. There are many ADC architectures; pipelined ADCs are advantageous and widely used in applications with signal bandwidths that are too high for oversampling delta-sigma ADCs and resolution requirements that are too high for flash ADCs. Nevertheless they are sensitive to distortion introduced by the residue amplifiers in their first few stages, and residue amplifier distortion tends to be inversely related to both power supply voltage and power consumption. Therefore, the residue amplifiers are usually the dominant consumers of power in high-resolution pipelined ADCs, particularly in low supply voltage designs [1]–[6]. Among the key building blocks in pipelined ADCs are the residue amplifiers that interface successive converter stages. Especially in the converter front-end, these gain elements have to meet very stringent speed, noise, and linearity requirements and tend to dominate overall power dissipation. To address this issue, a variety of techniques have been developed to minimize amplifier power in pipelined ADCs. Among them, stage scaling [3], [4], optimization of the per-stage resolution [5]–[7], and amplifier sharing techniques [8], [9] are commonly used. In addition to their dominance in power consumption, it has also been recognized that residue amplifiers are most susceptible to complications that arise from continuing integrated circuit technology scaling [10], [11]. For implementations in future deep submicron processes, it is often predicted that limited supply headroom and low intrinsic device gain may lead to a relative power increase in such noise-limited precision analog circuit blocks [12], [13]. In this paper, a pipelined ADC is designed that achieves superior SNR, and operates at 100Msps, with power dissipation less than 70mW. Section II discusses pipelined ADC architecture, section III discusses design of software model for proposed pipelined ADC. Section IV discusses the schematic design of pipelined ADC and layout design. Section V presents conclusion.

a) Architecture of Pipelined ADC

The purpose of analog to digital converts is to sample and digitize an analog signal. The more precisely the analog signal is converted to digital, the more information can be obtained from it. It is also desirable to convert high bandwidth or high frequency analog signals; thus, ADCs must be capable of a fast sampling rate as well being accurate. The pipeline ADC is the architecture of choice for applications that require both speed and accuracy and where latency is not concern. The basic idea behind the pipeline ADC is that each stage will first sample and hold the input then it is compared with *VREF*/2. If the input is greater than

Author α : Research Scholar, JNTUA college of Engineering, Anantapur & Associate Professor in PACE Institute of Technology and Sciences, Ongole. E-mail : dsajvrao@gmail.com

Author σ : Associate Professor & Head, JNTUA College of Engineering, Anantapur. E-mail : prrjntu @gmail.com

Author ρ : Professor & Course Manager, MSRSAS, Bangalore. E-mail : cyrilyahoo@gmail.com

VREF/2, output a 1 for that stage and pass the input voltage directly to the next stage. If the input is less than *VREF*/2, output a 0 for that stage and multiply the input voltage by 2 before passing it to the next stage. Figure 1 shows the block diagram for this basic operation.

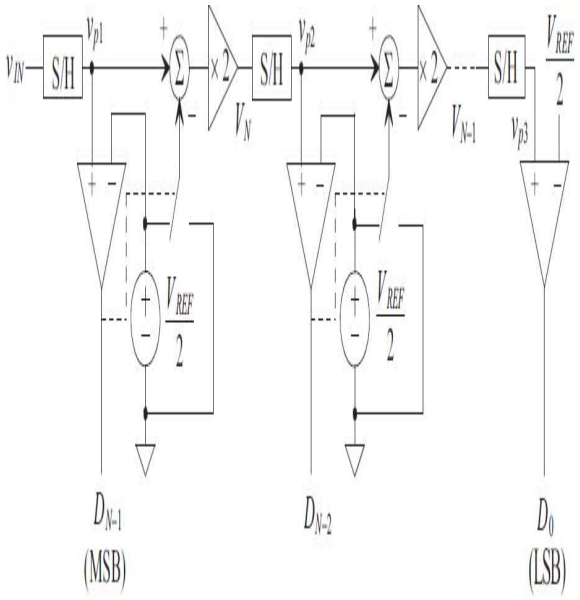


Fig. 1 : Pipeline ADC Block Diagram [1]

There are a few challenges with the basic pipeline ADC architecture that this project will attempt to address. Before looking at the sources of error, it is worth noting that an error in the early stages of the pipeline will propagate through the pipeline affectively being amplified by 2 by each successive stage. Errors can be created by the comparators not switching at the correct point. This means that the comparator may have some offset which will result in it making the wrong decision. The sample and hold may also have some offset causing the wrong voltage to be passed to the comparator which will result in the same problem of the comparator making a wrong decision. The other source of error is the multiply by 2 function, because it is difficult to multiply by a gain of exactly 2. These limitations with real op-amps and comparators will result in integral nonlinearity (INL) and differential nonlinearity (DNL) errors. This design requires 12-bit resolution. This means that there will be 2^{12} or 4096 possible output bit combinations. Assuming a *VREF* of 1V, 1LSB or the level of analog resolution is given by

$$1LSB = \frac{V_{REF}}{2^N} = \frac{1}{4096} = 244\mu V$$

To correct the errors caused by the offsets in the comparators and the sample and hold op-amps, a technique called 1.5 bits/stage will be used. The name 1.5 bits/stage is based on the fact that each stage has an output with three possible cases consisting of *a* and *b* signals, where *ab* can be 00, 01, or 11. The ideal transfer curve for the 1.5 bits/stage of *vin* versus *vout* is shown in Figure 2. And, the relationship between *vin* and *vout* can be expressed as:

$$v_{out} = 2 \cdot \left(v_{in} + \overline{ab}\frac{V_{CM}}{2} - \bar{a}b\frac{V_{CM}}{2} - ab\frac{3V_{CM}}{2}\right).$$

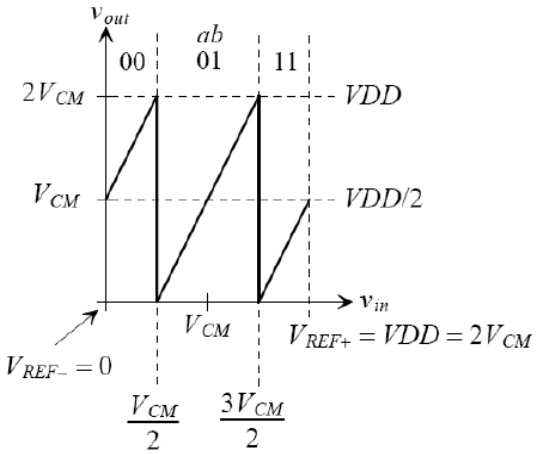


Fig. 2 : 1.5 Bits/Stage Transfer Curve (Single-ended) [1]

b) Software reference model design of Pipelined ADC

The functional block diagram of the pipelined ADC is simulated using Simulink in MATLAB. The 1-bit single stage converter behavioural block has been designed and simulated. The behaviour of the block has been developed using the equations given below.

- If Vin > Vmid Vresidue=2(Vin-Vref)
- If Vin < Vmid Vresidue=2(Vin)

Using a reference value this single stage block would act as a comparator and gives a bit as output. Again that bit will be converted in to analog value that value again compared with the actual input signal and the difference signal will be produced. The difference signal will be in the range of half of the actual input range. Since the total pipelined architecture has been developed using these similar types of 1-bit single stage blocks should give the same input rage to all stages. To get that voltage range we should multiply the error signal with 2 then we can give output of one stage to input of next stage. Every stage has its own sample and hold circuit operating at 100 MS/s. the output of the sample and hold stage will be consider as the input to the 1-bit converter. Figure 3 shows the software reference model of 1-bit conversion.

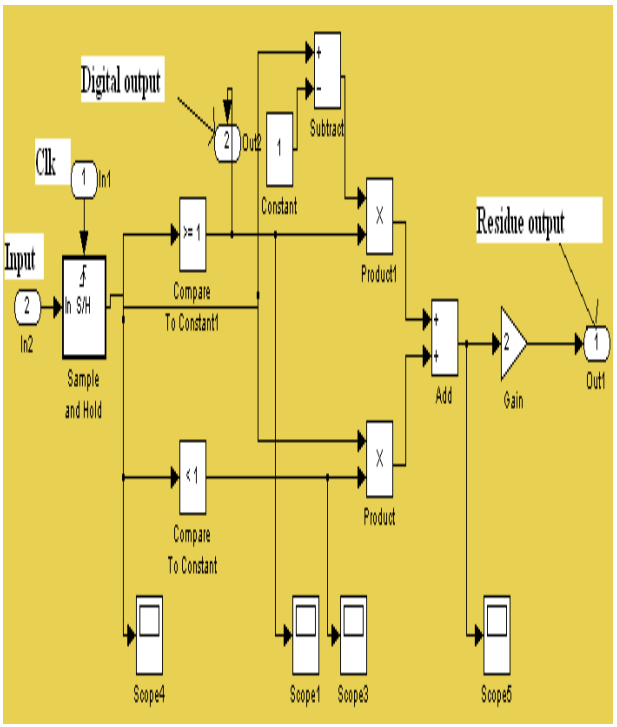


Fig. 3 : Simulink model for the 1-bit conversion stage

The input and output waveforms of this single stage are shown in Figure 4. The 1 MHz input sine wave has been sampled by the 100 MHz clock signal. Theoretically we can estimate the signal to noise ratio (SNR). SNR (worst case) = 6.02 n+4.24 dB Hence we have established the boundary conditions for the choice of the resolution of the converter based upon a desired level of SNR. Based on this calculation the 12-bit pipelined ADC having (SNR) 68 dB.

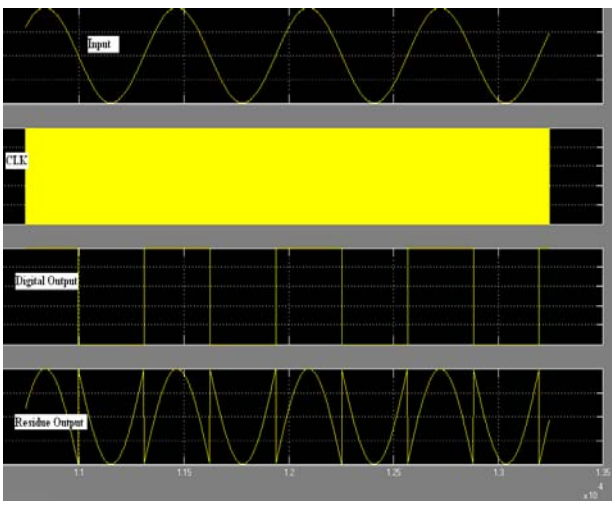


Fig 4 : Digital and Residue output waveforms of the single stage pipelined ADC

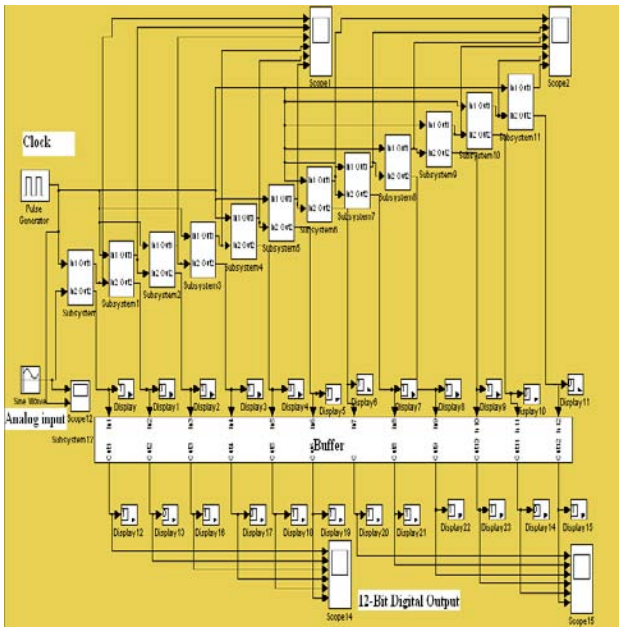


Fig. 5 : Matlab simulink model for the 12-bit pipelined ADC

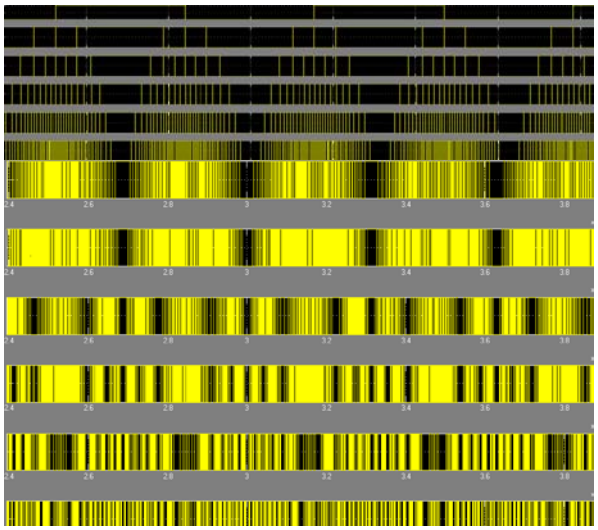


Fig. 6 : Digital output from the 12-bit pipelined ADC for sine wave

II. VLSI Implementation Of The 12-Bit Pipe Lined ADC

a) Bit Single Stage of Pipelined architecture

This stage is consist of sample and hold circuit followed by 1-bit ADC, 1-bit DAC, subtracted and multiplier. The analog signal will be sampled and fed to the comparator acts as the 1-bit ADC that would give the 1-bit digital output. Before giving to the comparator the sample signal should lift to the .9V of the DC voltage so that the comparator can compare the value to the threshold voltage and give the output. The digital output again converted to the analog value through the 1-bit DAC Uses two reference voltage levels. This converted value will be subtracted from actual sampled signal to

produce an error signal using a difference circuit. This signal often called as residue signal. This residue signal again multiplied by two with an open loop amplifier. The sub tractor and the multiplier are working at 100 MS/s and input rage of +/-300mV. The sub tractor and the multiplier are designed based on Op amp this op amp should work at 100 MHz by using normal op amps it is difficult to reach 100 MHz frequency.

b) Sample& Hold Circuit

In this paper work sampled hold circuits are implemented by the transmission gates and capacitors. The switched capacitor technique has been implemented to reduce the power. The input to the sample and hold circuit is sine wave having bandwidth of 1MHz and the sampled signal frequency is 100MHz. The delay between in out and output that will be offered by this sample and hold signal is 17ns. The output of the sample Hold signal is sampling signal having frequency of 100MHz

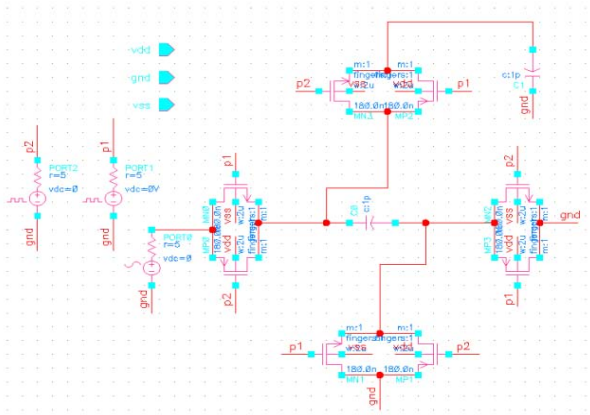


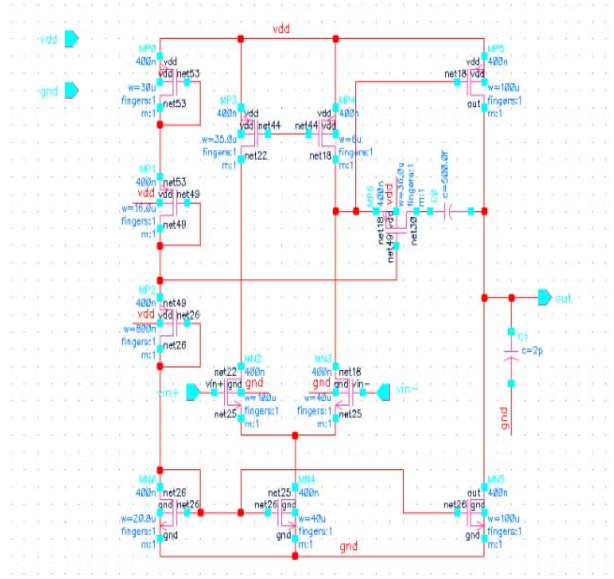
Fig. 7 : Schematic diagram and output results of the sample and hold circuit

c) Wideband Operational Amplifier Design

Subtraction and multiplier circuits are designed using the wideband op amp. The specifications of the amplifier identified from the top level simulation of 12-bit pipelined ADC by the MATLAB Simulink. The achieved parameters from the operational amplifier simulation are

DC Gain =75dB
Unity Gain Freq=160 MHz
Slew Rate=9.8e6 V/Sec
Phase Margin=57°
Input swing= +/- 0.35mV
Output swing= +/- 1.15V

The 3dB Bandwidth of the op- amp is selected as 100 MHz to meet the application of the architecture. The schematic has simulated by the cadence specter and layout has drawn by the virtuoso. The simulated transient and ac analysis waveforms are shown in the Figure 8.



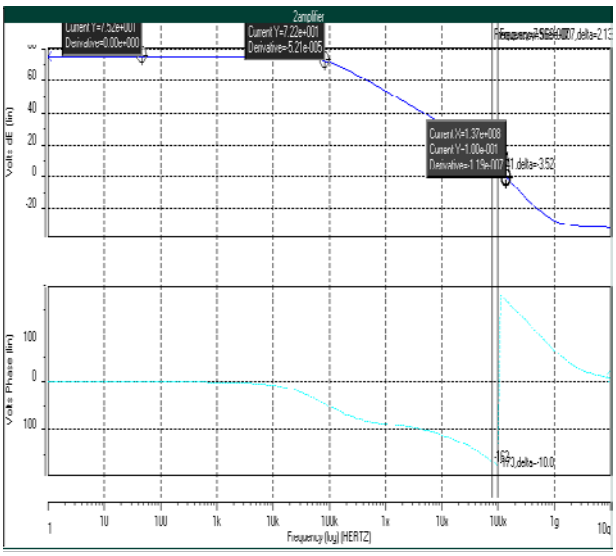


Fig. 8 : Wideband opamp schematic diagram and AC analysis

d) 1-Bit ADC design using CMOS Inverter

In this paper however a new approach the Threshold Inverter Quantizer (TIQ) based on systematic transistor sizing of a CMOS inverter in a full-flash scheme eliminates the resistor array implementation of conventional Comparator array flash designs. Therefore no static power consumption is required for quantizing the analog input signal making the idea very attractive for battery-powered applications. We can estimate safe analog input rage as follows:

Analog range = *Vdd* - (V_{TN} + | V_{TP}|), where V_{TN} and V_{TP} are the threshold voltages for large NMOS and PMOS devices, namely the V_{THO} value from the model parameter data set used during the entire design process.

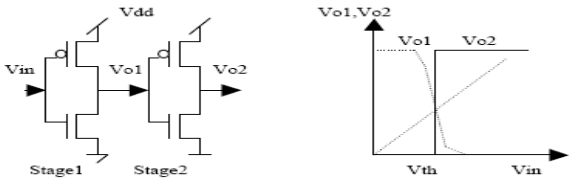


Fig. 9 : Schematic Diagram of Comparator

e) 1-Bit DAC Design

For the design of one bit DAC we have used pass transistors The CMOS transmission gate consist of one NMOS and one PMOS transistor connected in parallel. The gate voltages applied to these transistors are also set to be complementary signals. As such the CMOS TG operates as a bidirectional switch between the nodes in and out this is controlled by clock signal.

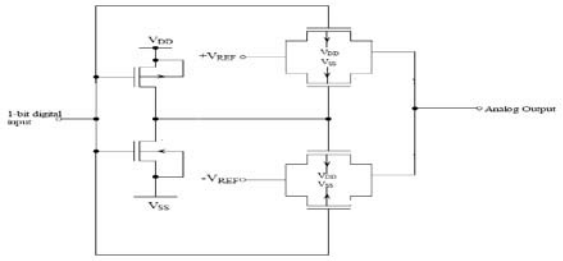


Fig. 10 : Schematic Diagram of 1-Bit DAC

f) Buffer Designing

This buffer stage is consist of number of Dffs, these Dff are designed using Tx-gates and NAND gates. The Schematics and Layout are shown in Figure 11. Through the practical calculations, I got the average rise and fall time is 0.18ns, and Setup Time is 154ps.

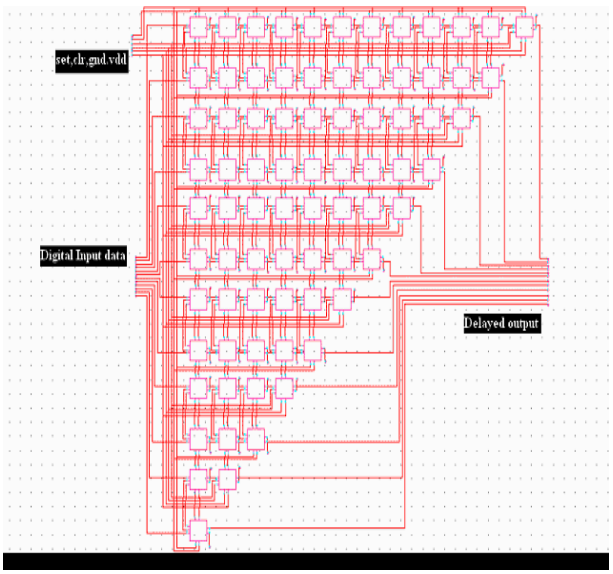


Fig. 11 : Schematic Diagram of 12-Bit Buffer

The digital outputs for a given input analog sample are not generated at the same time. MSB comes first and LSB last. The time delay between adjacent bits is one half clock cycle. All bits need to be synchronized. The 1-bit digital output from the first stage is delayed by 12 half cycles and the output from the second stage is delayed by 11 half cycles and so on. The output from the last stage is delayed by a half cycle. The delay block is made of D flip-flops (DFF) implemented with transmission gate and static NAND gates. Since sampling rate is only 100 MS/s and the word length is 12 bits the carry ripple is not an issue under 0.13µm process.

g) 1-Bit Single stage of Pipelined Architecture

This stage is consist of sample and hold circuit followed by 1-bit ADC, 1-bit DAC, subtracted and multiplier. The analog signal will be sampled and fed to the comparator acts as the 1-bit ADC that would give the 1-bit digital output. Before giving to the comparator the sample signal should lift to the 0.9V of the DC voltage, so that the comparator can compare the value to the threshold voltage and give the output.

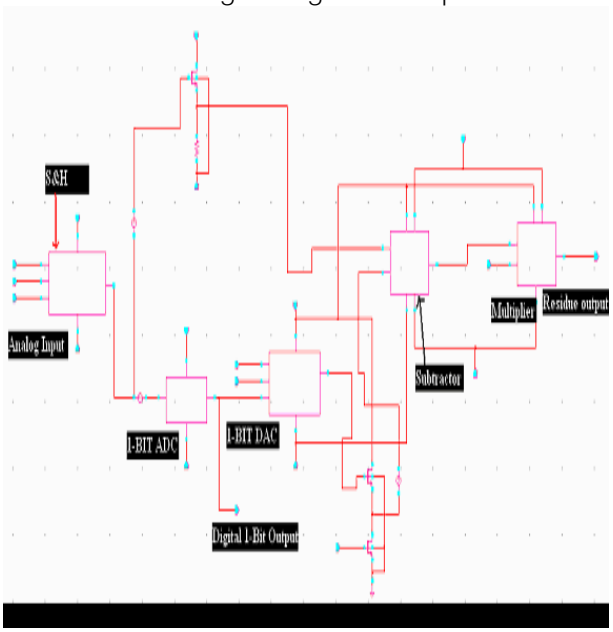


Fig. 12 : Schematic Diagram of 1-Bit Conversion Stage

The digital output again converted to the analog value through the 1-bit DAC, Uses two reference voltage levels. This converted value will be subtracted from actual sampled signal to produce an error signal using a difference circuit this signal often called as residue signal. This residue signal again multiplied by two with an open loop amplifier. The difference and the multiplier are working at 100 MS/s and input rage of +/-250mV.

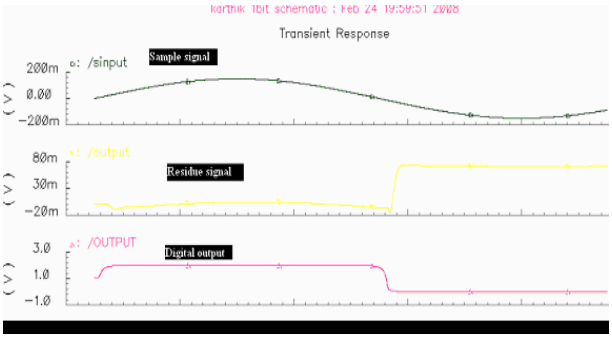


Fig. 13 : Output Wave Form of 1-Bit Conversion Stage

III. Result Analysis

The first signal on the above shown wave figure is the input sine wave having voltage rage of +/- 200mV. Last signal is the digital output from the single stage of pipelined ADC. The second signal is the residue output signal which is going to input of the next stage of the pipelined ADC. Since This residue signal is being affected by the loads at different stages we should amplify this signal before giving to the next stage.

a) Top-Level Schematic

The layout of the wide band two stage operational amplifiers is shown. The area occupied by the amplifier layout is 30um*36um.To implement layout fingering and inter digitized technique are used.

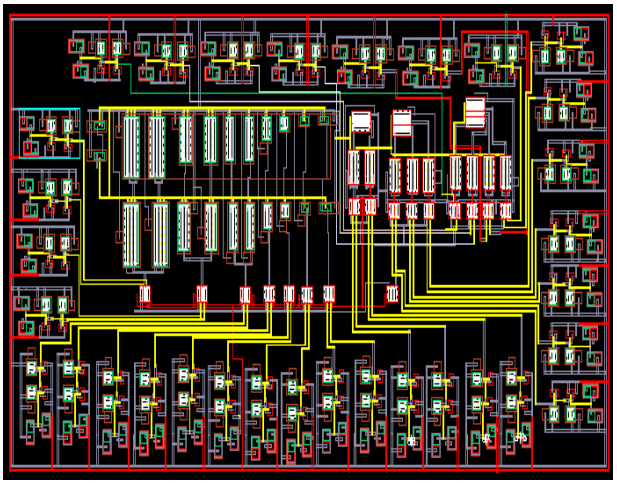


Fig. 14 : Top-Level Schematic of pipelined ADC

Figure 15 shows the frequency domain analysis of pipelined ADC. The output of ADC is captured and is processed using FFT processor to convert the time domain discrete samples to frequency domain samples. The frequency domain samples obtained are plotted and SNR is measured. In order to estimate the performance of ADC, a known input with single frequency is used as test vector. The frequency spectrum obtained is analyzed for the number of harmonics. The first five harmonics are considered to compute SNR.

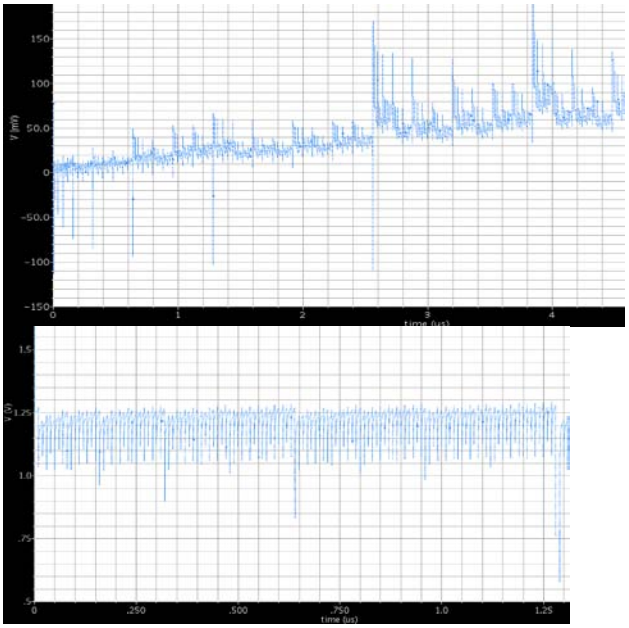


Fig. 15 : Frequency domain response of pipelined ADC.

The power consumption at a clock frequency of 100 MHz was 70 mW from a 1.8 V supply. Below Table 1 summarizes the measured results.

	Previous work	Present Work
Technology	CMOS 0.35um	CMOS0.13um
Power Supply	3V	± 1.8V
Input Signal Freq	200kHz	up to 10 MHz
Input voltage range	---	+/-250mV
Power dissipation	290uW	70mW
Area	7.9 mm2	6.5 mm2
Sampling freq	75MHz	100 MHz

Table 1 : Results comparison

IV. Conclusion

The goals of this paper is First different ADC architectures were analyzed to determine the optimal topology for the given performance specifications with minimum power consumption. Second the exact implementation of the chosen architecture was investigated in an effort to use the minimum amount of power. This Paper involved designing an integrated CMOS Analog-to-Digital converter for communication and video applications. The performance specifications were 12-bits, power dissipation less than 70 mW, area should be less than 6.5mm^2 and static performance parameters such as INL and DNL should be less than 1

LSB and 0.5 LSB in order to make a monotonic ADC. This pipelined ADC has been met the performance requirements. The ADC was designed in 0.13um technology at an operating voltage of ±1.8 V. Sample and hold circuit is designed by the switched-capacitor implementation. We can use the rail to rail op amp to increase the input voltage range of the ADC but by increasing the input voltage swing the resolution will be affected. Common-mode drift issue Since there is no common-mode feedback inside the loop the common-mode drift caused by the mismatch of capacitors, offset of op amp and charge injection will accumulate stage by stage. Careful design and layout are supposed to minimize the total drift within 100 mV such that the residue output signal will not be out of saturation. But this problem is likely to cause trouble if the common-mode signal is not controlled well as expected.

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Development of Commercial Grade Silicon Drift Detector with On-Chip JFET: Device Design, Technology & Characterization

By Pourus Mehta, Sudheer K.M, V.D. Srivastava, Rejeena Rani, Y.P. Prabhakara Rao & C.K. Pithawa

Bhabha Atomic Research Centre

Abstract - Proto-type Silicon Drift Detectors (SDDs) have been realized through a pilot stage fabrication run at the Micro-fabrication facility at Indian Institute of Technology - Bombay (IIT-B). Taking precedence from the fabrication run at IIT-B, commercial grade SDDs with on-chip low noise JFETs are being developed for low energy X-ray spectroscopy and position sensing applications using silicon bipolar technology available with Bharat Electronics Ltd (BEL), Bangalore. This paper presents a detailed illustrative view on the design; fabrication and characterization of the SDDs & in-built JFETs fabricated at BEL. Traditionally, detectors are fabricated over high resistivity silicon substrates whereas JFETs are fabricated over low-resistivity silicon. To design a process for fabrication of both SDD and JFET over high resistivity silicon posed a sufficient technological challenge.

Keywords : *Silicon Drift Detector, Junction Field Effect Transistor, Technology Computer aided Design & I-V characterization.*

GJRE-F Classification : *PACS: 85.30.-z, 85.30.De & 85.30.Tv*

Strictly as per the compliance and regulations of :

Development of Commercial Grade Silicon Drift Detector with On-Chip JFET: Device Design, Technology & Characterization

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Keywords : Silicon Drift Detector, Junction Field Effect Transistor, Technology Computer aided Design & I-V characterization.

PACS : 85.30.-z, 85.30.De & 85.30.Tv

I. Introduction

Silicon drift detector (SDD) is a device based on the principle of lateral charge transport within the bulk of a fully depleted detector, as proposed by Gatti and Rehak (Reference-1). SDD is essentially detector in which a high resistivity *n*-type silicon substrate is employed to fabricate *p-n* junctions on both sides of the substrate. PN junctions on the front side form segmented field shaping cathodes whereas a uniform, *p-n* junction forms the back-cathode. A reverse bias gradient when applied to the field shaping cathodes together with a constant back-contact voltage creates a potential distribution in the shape of a "Potential Gutter" with the ultimate electron potential energy minimum at the anode. Electron-hole pairs created by passage of ionizing radiation are swept vertically by the parabolic potential along the depth and focused at the local potential minima from where they get drifted along the lateral drift channel towards the anode. The distinguishing feature of the SDD is that its small output (anode) capacitance is independent of its large detector active area.

Thus SDDs are suitable for high resolution (127eV @ 5.9 keV for Mn-Kα line; Ketek Vitus SDD) and high count rate (~$1x10^6$ cps) X-ray spectroscopy applications. These detectors have found wide application in high-energy physics for tracking applications. SDDs have been incorporated in the ALICE detector along the Large Hadron Collider at CERN.

This high-resolution capability of SDDs can be further augmented by integrating the input device of the pre-amplifier (JFET) with the detector so as to avoid stray capacitance and microphonism arising due to wire bonding between them. The integration of JFET onto the detector also facilitates better matching between detector and transistor capacitances.

The proto-typing stage fabrication of SDDs at IIT-B has been successfully completed. The first run of the fabrication of the commercial grade SDDs and JFETs has yielded satisfactorily good results.

SDDs fabricated at BEL were aimed at both X-ray Spectroscopy and position sensing applications. Circular geometry SDDs with in-built low noise JFETs were designed for X-ray Spectroscopy applications. Linear geometry SDDs with on-chip poly-silicon resistors were designed for 1D & 2D position sensing applications. Additionally, high transconductance JFETs were also designed together with various different kinds of SDDs over the 4-inch silicon wafer.

II. Detector Design

This particular version of SDD has an on-chip Poly-Resistor network for biasing the intermediate p+ strips together with an on-chip JFET for first level

Author α : Bhabha Atomic Research Centre, Electronics Division, MOD Lab, Trombay, Mumbai 400085, India. (Corresponding Author)
E-mails : pdmehta@barc.gov.in, pourus@cern.ch & pourus_m@yahoo.com
Author σ ρ ¥ χ : Electronics Division, Bhabha Atomic Research Centre, Trombay, Mumbai 400 085, India.
Author ω § : Bharat Electronics Limited, Banglore, India.

amplification [Fig. 1(b)]. The anode is in geometry of an annular ring having 50 μm radii with an area of 7.7 x 10^4 μm^2 that fetched an analytical full depletion capacitance of 27 fF for 300 μm thick fully depleted silicon wafer. The total active area of the detector was 2.31 x 10^7 μm^2. This device had 20 p+ strips with two guard rings encircling its outer perimeter. The first, fifth, tenth, fifteenth, twentieth, and last p+ strips were individually biased whereas the of rest p+ strips got biased by the on-chip resistor. Each poly resistor was designed to present a resistance of 102.4 kΩ (R_S=138.88 kΩ/□). The embedded lownoise JFET (named as JFET-10) for this SDD design had the smallest channel length (15 μm) possible with BEL process [Fig. 1(b)]. For a designed channel length of 15 μm and the channel width of 172 μm, the analytical Transconductance (g_m) works out to be **0.247 mS.**

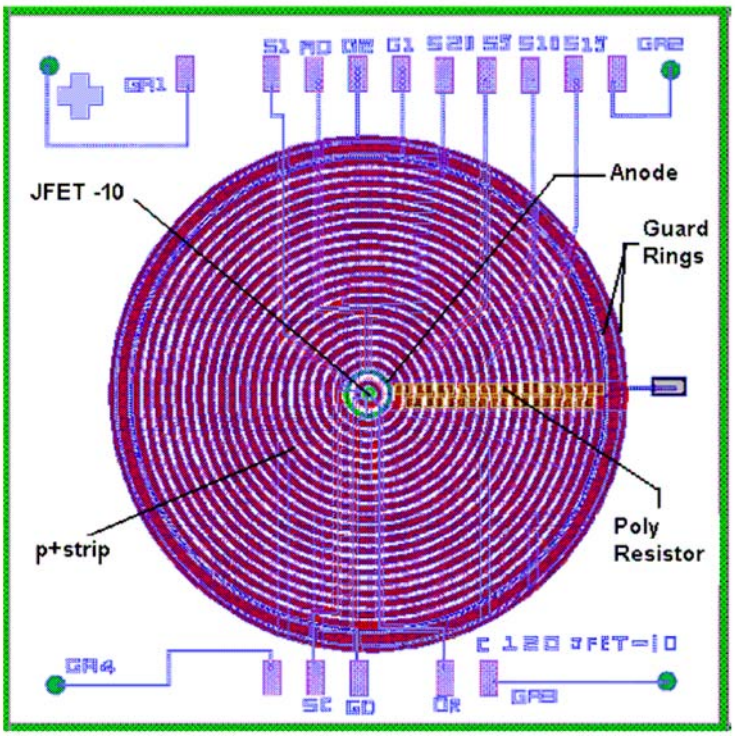

Fig. 1 (a) : Composite layout of Circular SDD (Pitch-120µm) with in-built JFET.

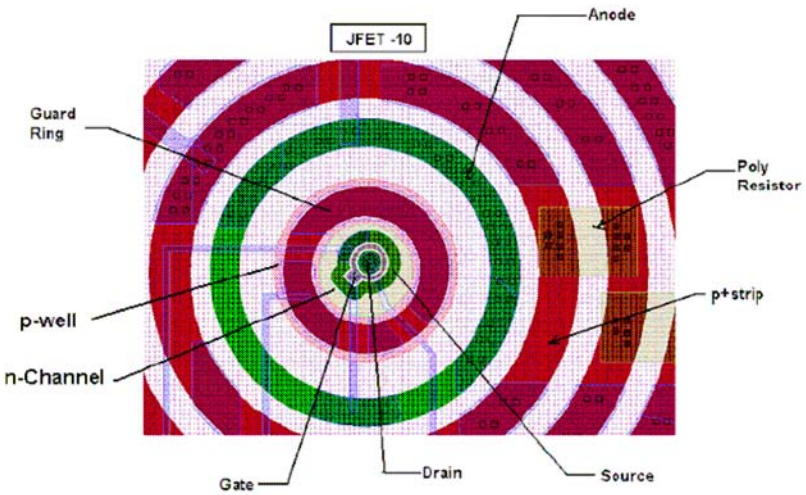

Fig. 1 (b) : Zoomed view of the embedded JFET (JFET-10) showing all mask layers.

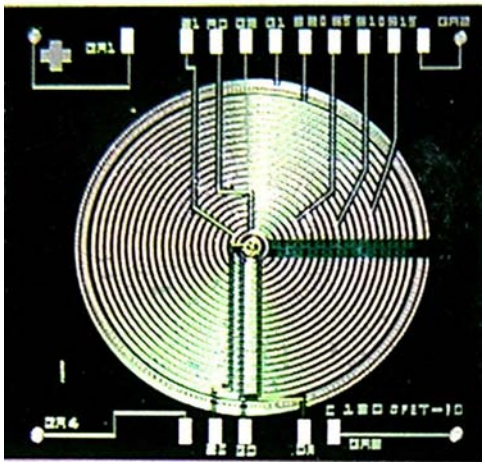

Fig. 1 (c) : Photograph of the completely fabricated SDD with in-built JFET.

III. Fabrication Of Sdds & Low-Noise Jfets

a) Fabrication Objectives

On the basis of the success of the fabrication effort at IIT-B, the process for the BEL effort was formulated. Formulation of a process for fabrication of SDD and JFET over high resistivity silicon substrate was a significant technological challenge. The process for the fabrication of SDD with integrated JFET was formulated with a view of achieving a high breakdown voltage of >100V, and achieving as low leakage current as possible using the existing fabrication setup at BEL. The process employed at BEL involved all the standard unit processes like oxidation, lithography, etching, and implantation, metallization etc. employed in a bipolar fabrication line. The process parameters have been fine tuned and frozen after a thorough TCAD process simulation study in order to achieve the desired doping profiles for both SDD & JFET. The highest standards of cleanliness and care in planning the unit processes have been maintained to achieve the objectives of low leakage currents together with admissibly high breakdown voltages. Moreover, the process had to be compliant with the technological constraints of the BEL foundry. Additionally, Polysilicon process has been employed for fabrication of on-chip resistor network. The distinguishing feature of this process was the employment of a double-sided processing for back to front alignment of cathode implants. Thus making double sided SDDs a reality, which are far more superior to single sided SDDs. The lithographic quality was again a challenge as the fabrication process involved 14 lithographic steps.

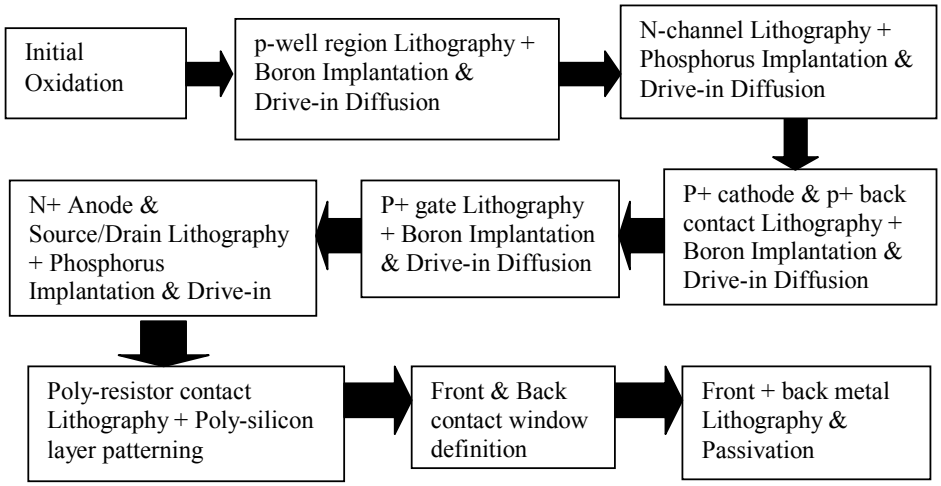

Fig. 2 : Block Diagrammatic illustration of the process flow.

b) Fabrication Process and TCAD Simulations

Starting with a 4-inch n-type, high resistivity (3-5 kΩ.cm) compensated silicon wafer of <111> orientation, an initial oxide was grown employing the Dry-Wet-Dry regime (Thickness = 0.6μm). The bulk comprising of the wet oxide (t = 0.4μm) was sandwiched between two high quality dry oxide layers (t = 0.1 μm) each. The next step was the lithographic

definition of the p-type isolation well (**Mask-1**) within the center of the SDD for housing the embedded JFET. This was followed by an oxide etch step to expose the substrate for boron implantation (E = **80 keV**; Dose = **$5x10^{11}$ cm^{-2}**). Subsequent dopant activation and drive-in diffusion of boron species was performed employing the Drive-in cycle as illustrated in the Fig. 4. The simulated doping profile for the p-well implant showed a peak boron concentration of $3.39x10^{14}$ cm^{-3} for a junction depth of **3.19 μm** and an extracted sheet resistance of **102.705 kΩ/□**. Subsequently, the n-channel within the p-well region was lithographically defined **(Mask-2)** and phosphorus implantation (E = **150 keV**; Dose = **$5x10^{12}$ cm^{-2}**) was performed followed by a drive-in cycle (Fig. 6) to form the n-channel. The simulated doping profile (Fig. 7) for the n-channel showed a peak phosphorus concentration of **$3.24x10^{16}$ cm^{-3}** for a junction depth of **2 μm** and an extracted sheet resistance of **2.703 kΩ/□**. Going ahead from here, the p+ cathodes & p+ guard ring (**Mask-3**) were lithographically defined on the top-surface whereas the p+ backcontact (**Mask-4**) was defined on the bottom surface of the wafer employing back to front double-sided alignment lithography. A thin screen-oxide (Fig. 8) was grown over the exposed silicon to create shallow junctions and prevent implantation damage. Boron Implantation (Dose = **$1x10^{15}$ cm^{-2}**; Energy = **80 keV**) followed by dopant activation and drive-in (Fig. 9) was performed to create p+ strips, p+ guard ring and p+ back-contact regions. The simulated doping profile showed a peak boron concentration of **$2.24x10^{18}$ cm^{-3}** for a junction depth of **1.5 μm** and extracted sheet resistance of **181.93 Ω/□**. The 5th lithographic (**Mask-5**) step was performed for definition of p+ type Gate region of the JFET. Boron Implantation (Dose = **$1x10^{15}$ cm^{-2}**; E = **80keV**), followed by Drive-in (Fig. 12) was performed to realize the p+ gate region. In the p+ Gate Drive-in case, the analytical value of sheet resistance was **181.93 Ω/□**, for a junction depth of **1.1 micron** and the extracted peak Boron concentration of **$1x10^{19}$ cm^{-3}**. Subsequently, n+ Anode, Source & Drain were defined (**Mask-6**) followed by Phosphorus Implantation (Dose = **$1x10^{15}$ cm^{-2}**; E = **80 keV**) forms the n+ regions. The dopant activation and drive-in was performed as per schedule in figure 14. The simulated analytical sheet resistance was **79.3 Ω/□**, for a characteristic depth of **1 micron** and the extracted peak Phosphorus concentration was **$1.1x10^{20}$ cm^{-3}**. Following this, oxide openings (Poly-contact: **Mask-7**) were defined over the p+ strips region to facilitate the poly-silicon layer deposited in the next step to make contact with under-lying p+ region. Poly-Silicon was then deposited and boron implantation was performed to form the poly-resistors having a Sheet Resistance of **138.88 kΩ/□**. After lithographically patterning (**Mask-8**) the polysilicon layer a short anneal step (Time = **30 minutes**; Temperature = **900ºC**) was carried out to dopant activation of the species in the poly layer. Proceeding from that, the contact lithography (**Mask-9**) was performed to open windows through the oxide for making contact with Aluminum metal deposited above for purpose of electrical connection with rest of the electronics. The back-contact was defined (**Mask-10**) for contact window openings on the back surface of the wafer. Aluminum metallization (Thickness = 1.5 microns) was carried out over the front-surface and lithography was performed (**Mask-11**) to pattern the metal layer to define the various electrical connections. The back-side was then metalized keeping the front-surface protected and the metal layer was patterned lithographically (**Mask-12**) to form the backelectrodes of the SDD. Lastly, Protective glass was deposited over both the front and back-sides followed by lithography (**Masks-13 & 14**) to open areas over the metal bond pads. The values for sheet resistances, junction depths for various regions have been tabulated in **Table-1**.

Table 1 : Analytical Values of sheet resistance and junction depth for various Process stages.

Sr. No.	Process stage	Junction Depth (μm)	Sheet Resistance (Ω/□)
1	p-well	3.19	102.7 k
2	n-channel	2	2.7 k
3	p-cathode	1.5	181
4	p+ gate	1.1	181.93
5	n+ Source/Drain & Anode	1.0	79

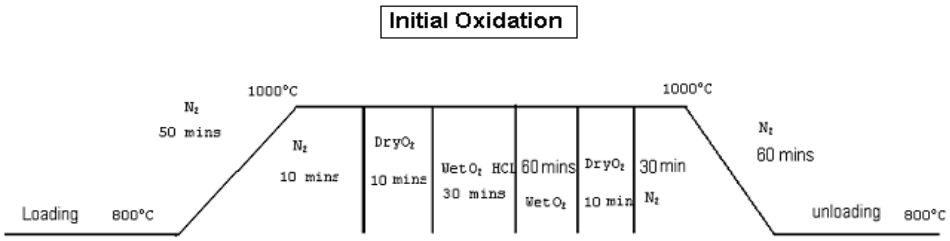

Fig. 3 : Schematic of the Initial Oxidation cycle

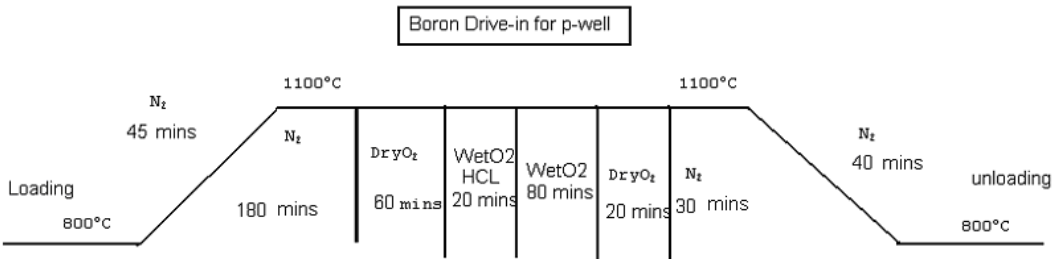

Fig. 4 : Schematic of the Boron Drive-in cycle for p-well.

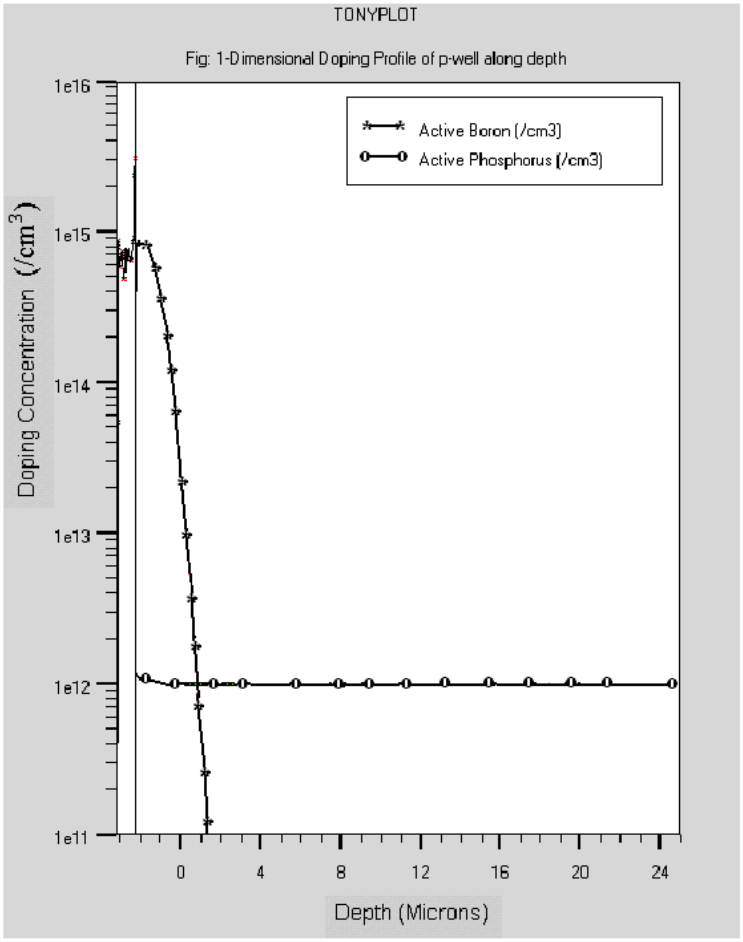

Fig. 5 : One-Dimensional doping profile of p-well region along depth.

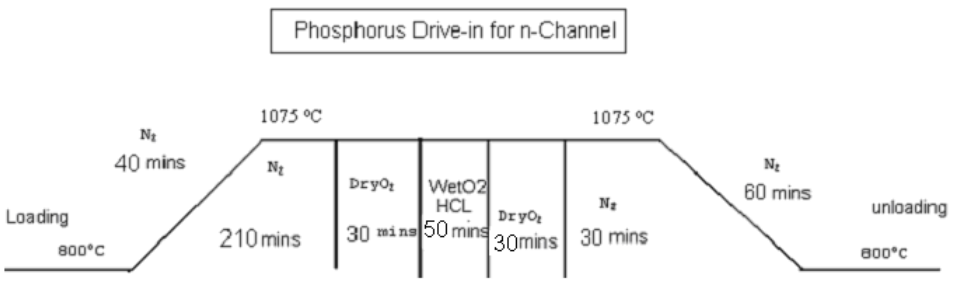

Fig. 6 : Schematic of the Phosphorus Drive-in cycle for n-Channel.

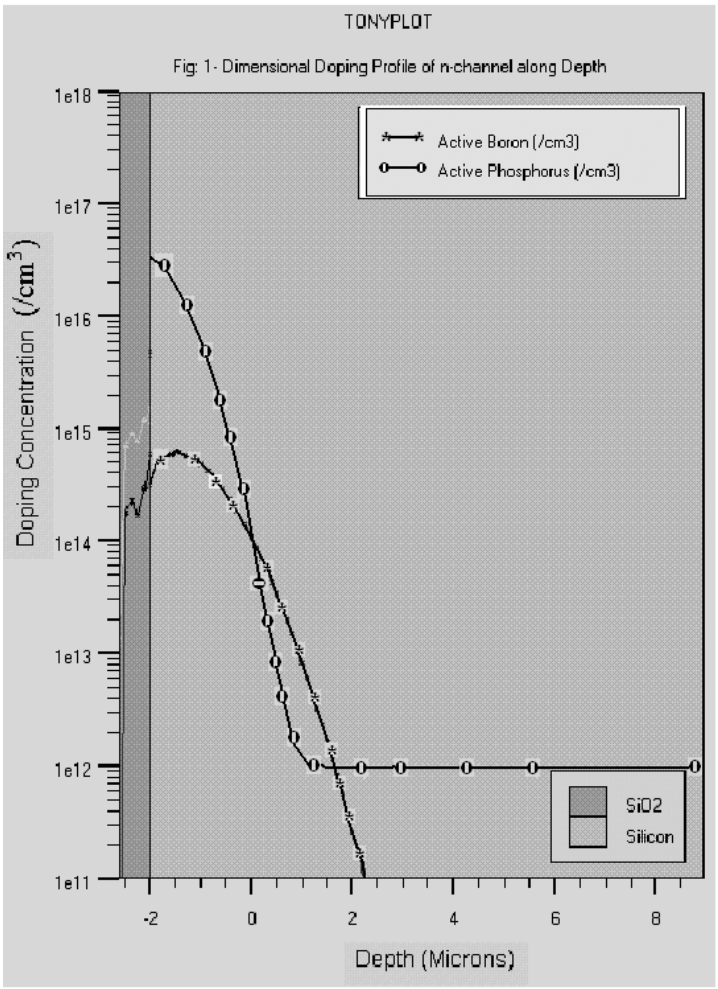

Fig. 7 : One-Dimensional doping profile of n-Channel region along depth.

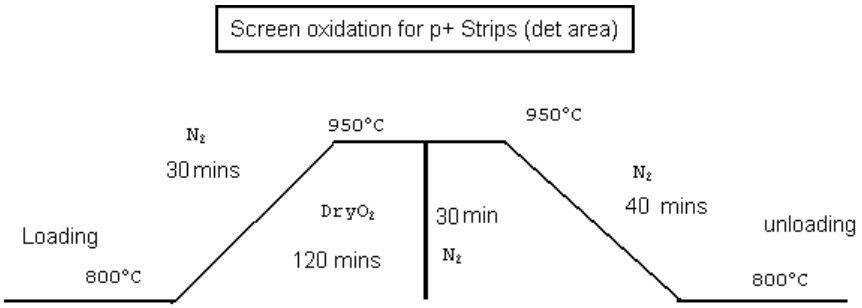

Fig. 8 : Schematic of the Screen Oxidation cycle for p+ Strips.

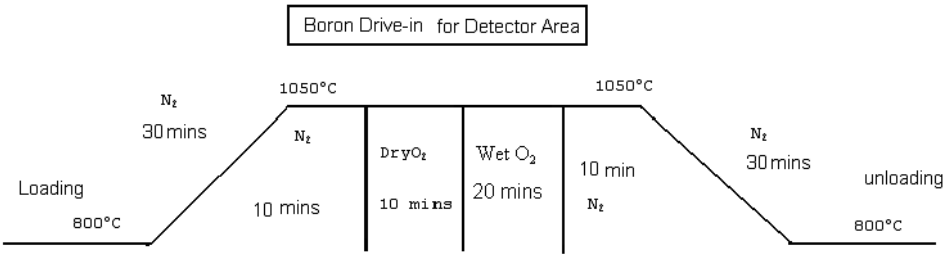

Fig. 9 : Schematic of the Boron Drive-in cycle for p+ Strips and p+ back contact.

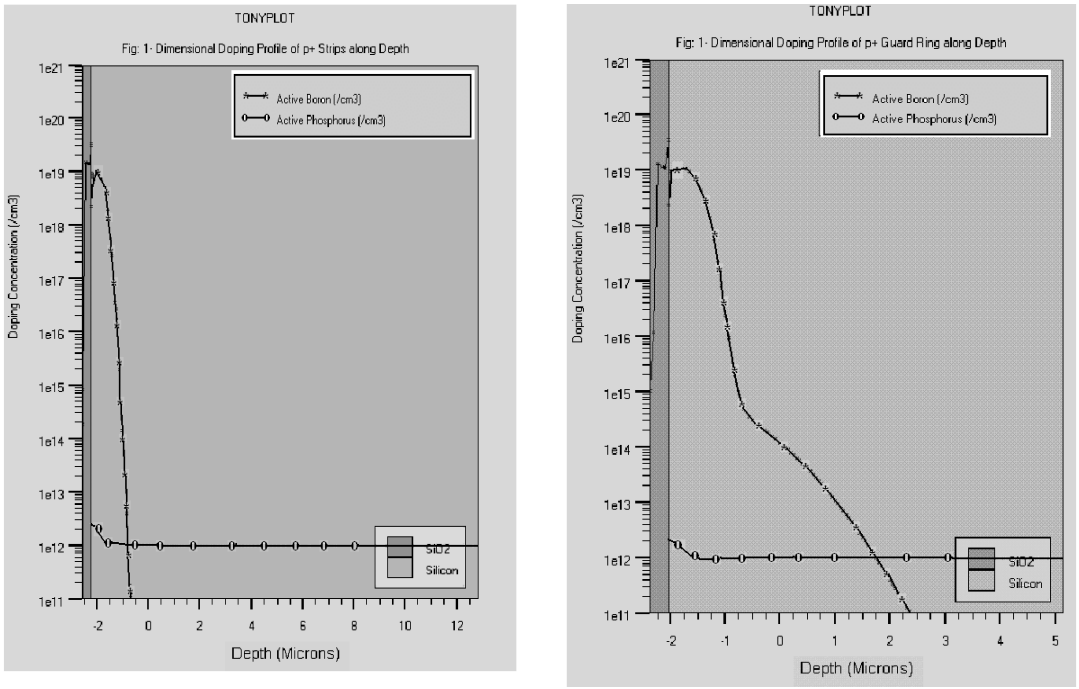

Fig. 10 : One-Dimensional Doping Profile of Annealed Boron Implant for p+ Strips & p+ Guard Ring.

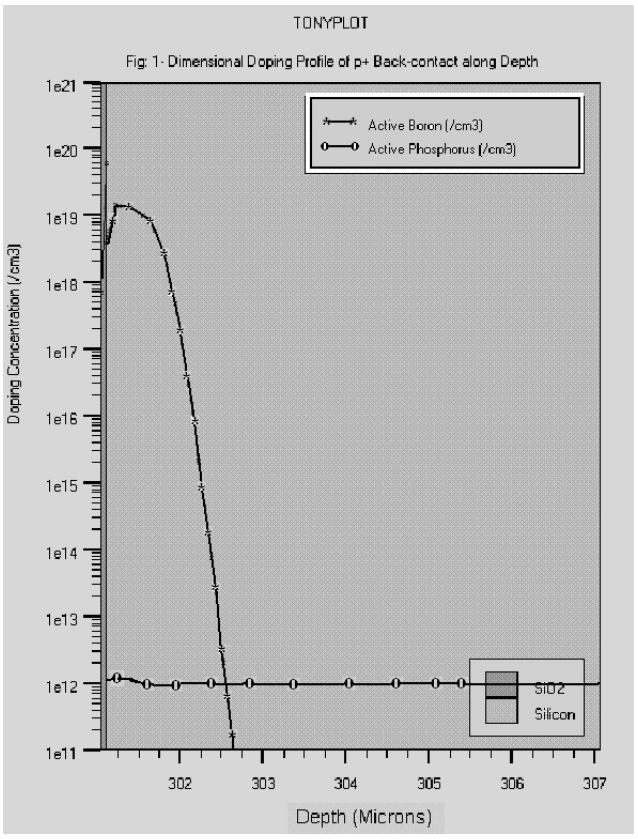

Fig. 11 : One-Dimensional Doping Profile of Annealed Boron Implant for p+ Backcontact.

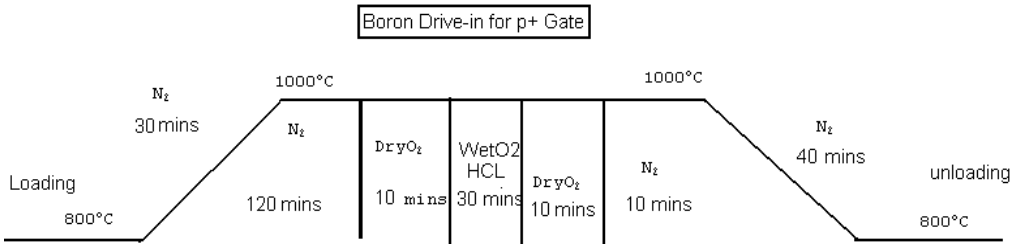

Fig. 12 : Schematic of the Boron Drive-in cycle for p+ Gate.

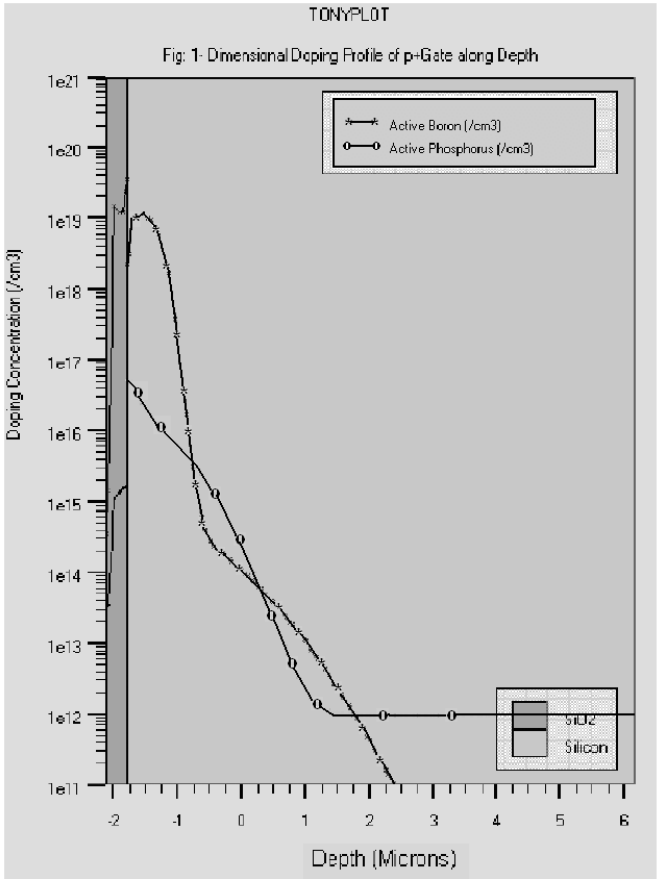

Fig. 13 : One-Dimensional doping profile of Gate region along the depth.

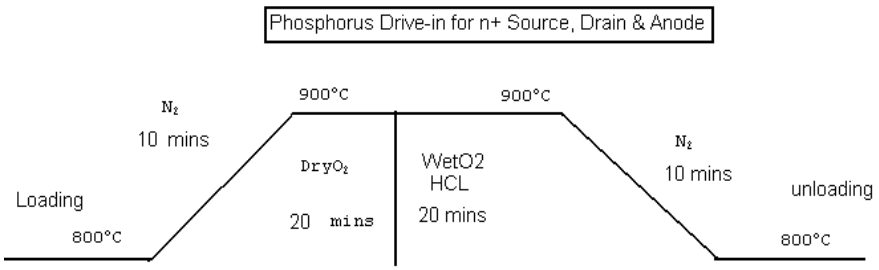

Fig. 14 : Schematic of the Phosphorus Drive-in cycle for n+ Source, Drain & Anode.

IV. I-V Characterization

a) Objectives & Measurement Methodology

I-V characterization of the completely biased SDD was performed to get the total biasing current across all the *p* strips and the total leakage current at the anode for a detector bias of -100V. A single Keithley-2400 source-measure unit was used to supply voltages to all the nodes through an external resistor network consisting of 20 resistors of 100 kΩ each, giving a minimum voltage of 5V at each node. Wafer level characterization was performed for each design of SDD.

The anode was given a zero potential (ultimate potential energy minima for electrons) and the first p+ cathode (Cathode - 1) was given a bias of –5 V. The last p cathode (Cathode-6) was biased at -100V and the back-cathode potential was fixed at -50V. The p cathodes intermediate between the first and last cathodes got biased automatically through onchip poly resistors. The p-well guard ring was kept floating in this case. A C++ program was coded for interfacing and automation of the Keithley meters for the measurement process. I-V was taken by ramping the voltage at the last strip (Cathode-6) from -100 V to 0 V and the anode current was measured through an ammeter (Keithley-2400 SMU used in current sense mode). I-V characteristics were measured for various values of guard-ring voltages (illustrated in Fig. 15). The nature of the I-V curve matched with the nature of I-V curve achieved for the SDDs in IIT case. The embedded low-noise JFET was characterized for its dc performance using the same experimental setup.

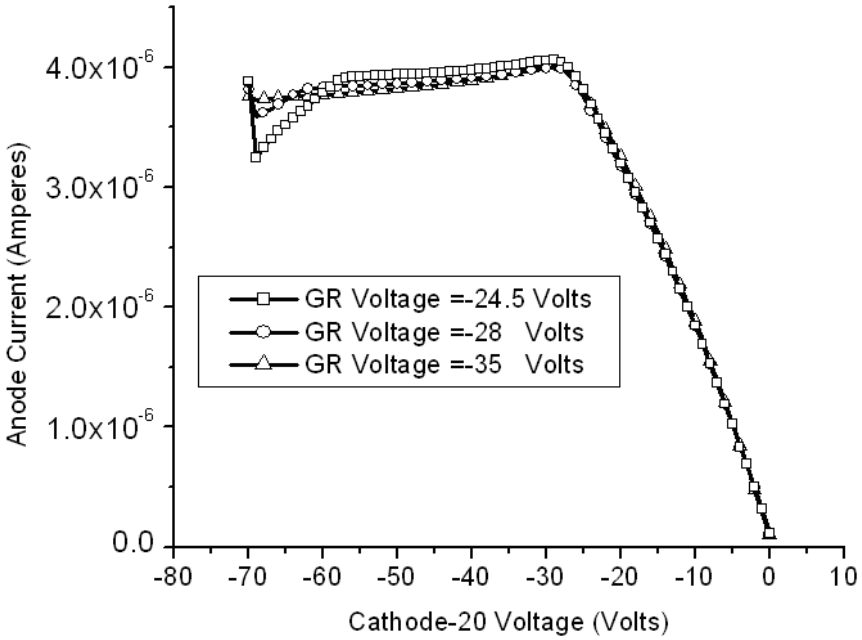

Fig. 15 : I-V Characteristics of Circular SDD (Pitch =120μm).

b) Results & Discussions

The anode current (Fig. 15) rises till above full depletion voltage (~ -25V) and then saturates to a value of ~ 3.7 μA till a cathode voltage of -70 Volts. The embedded low-noise JFET was also characterized for extracting the drain and transfer characteristics (Figs. 16 & 17). The experimentally achieved Transconductance (g_m) was 0.34 mS for a Pinchoff voltage of -7 Volts. The experimentally derived transconductance value was within 30% of the analytical value derived from simulation. The channel resistance value derived from the I-V plot was 20 kΩ and the calculated thermal noise $[(8kT / 3g_m)^{1/2}]$ worked out to be 5.69 nV√Hz. The value of noise figure achieved was good enough to qualify the JFET in the low-noise category.

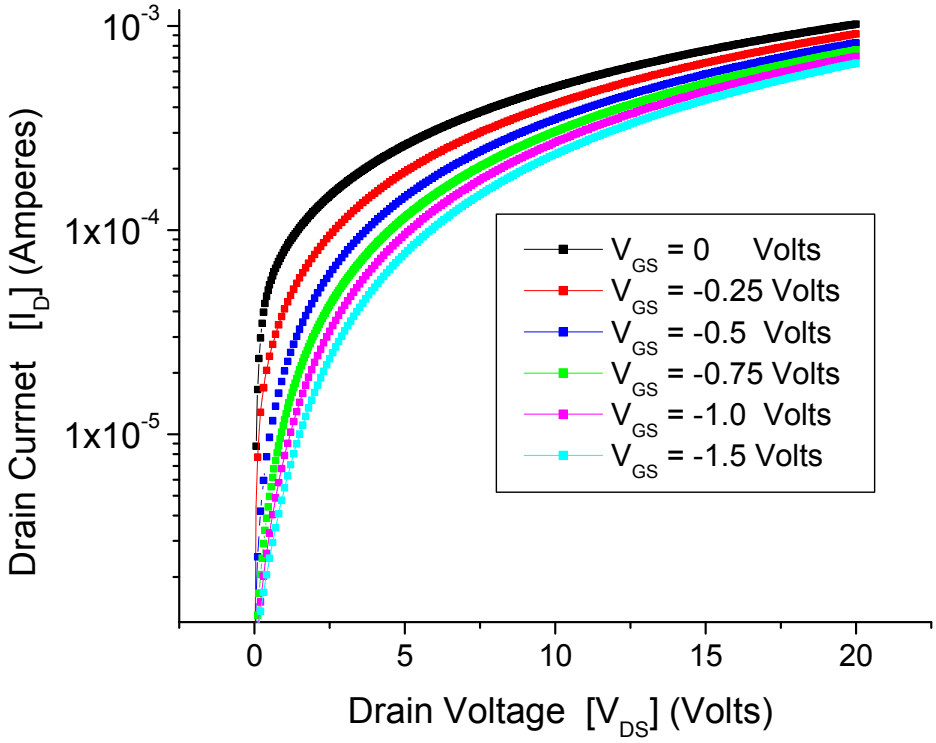

Fig. 16 : Drain Characteristics of embedded JFET.

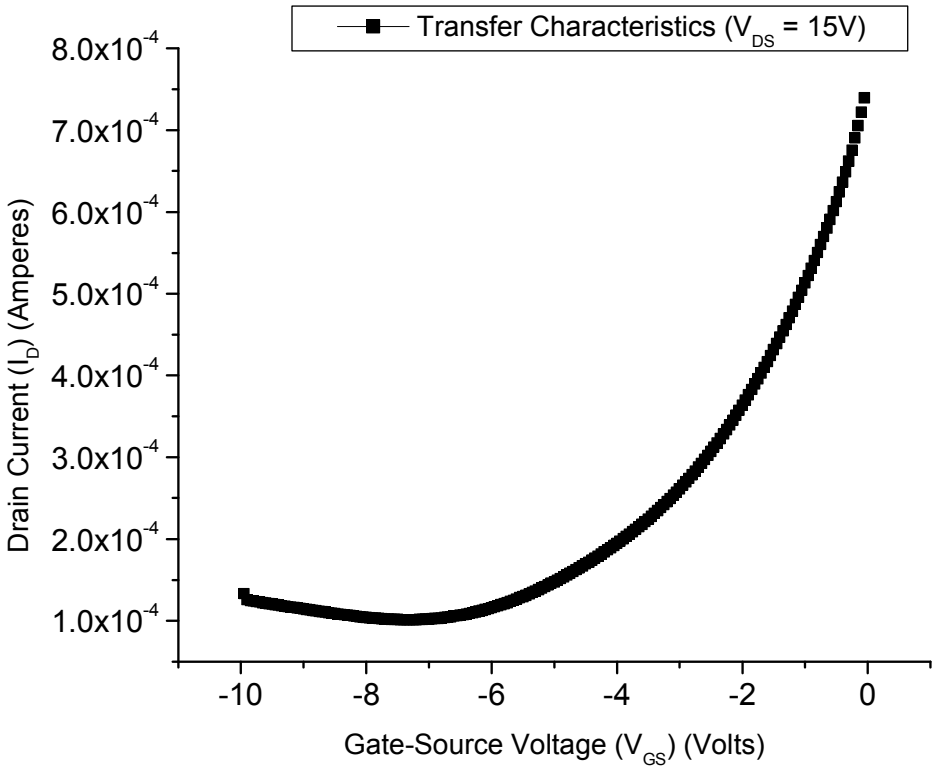

Fig. 17 : Transfer Characteristics of embedded JFET.

V. Conclusions

First prototypes of SDDs with embedded low noise JFETs have been successfully fabricated at BEL, Banglaore. Process technology for fabrication of SDDs and lownoise JFETs has been developed employing simulation studies in TCAD. Dc characterization of SDDs and embedded low-noise JFETs have been successfully carried out. The experimentally achieved values for anode current were higher than expected. Analytical value of transconductance was found to have a

deviation of less than 30% from that achieved from characterization. The value of noise figure (5.69 $nV\sqrt{Hz}$) was within the low noise band.

Acknowledgements

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(g) Discussion should cover the implications and consequences, not just recapitulating the results; conclusions should be summarizing.

(h) Brief Acknowledgements.

(i) References in the proper form.

Authors should very cautiously consider the preparation of papers to ensure that they communicate efficiently. Papers are much more likely to be accepted, if they are cautiously designed and laid out, contain few or no errors, are summarizing, and be conventional to the approach and instructions. They will in addition, be published with much less delays than those that require much technical and editorial correction.

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It is vital, that authors take care in submitting a manuscript that is written in simple language and adheres to published guidelines.

Format

Language: The language of publication is UK English. Authors, for whom English is a second language, must have their manuscript efficiently edited by an English-speaking person before submission to make sure that, the English is of high excellence. It is preferable, that manuscripts should be professionally edited.

Standard Usage, Abbreviations, and Units: Spelling and hyphenation should be conventional to The Concise Oxford English Dictionary. Statistics and measurements should at all times be given in figures, e.g. 16 min, except for when the number begins a sentence. When the number does not refer to a unit of measurement it should be spelt in full unless, it is 160 or greater.

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Abstract, used in Original Papers and Reviews:

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Many researchers searching for information online will use search engines such as Google, Yahoo or similar. By optimizing your paper for search engines, you will amplify the chance of someone finding it. This in turn will make it more likely to be viewed and/or cited in a further work. Global Journals Inc. (US) have compiled these guidelines to facilitate you to maximize the web-friendliness of the most public part of your paper.

Key Words

A major linchpin in research work for the writing research paper is the keyword search, which one will employ to find both library and Internet resources.

One must be persistent and creative in using keywords. An effective keyword search requires a strategy and planning a list of possible keywords and phrases to try.

Search engines for most searches, use Boolean searching, which is somewhat different from Internet searches. The Boolean search uses "operators," words (and, or, not, and near) that enable you to expand or narrow your affords. Tips for research paper while preparing research paper are very helpful guideline of research paper.

Choice of key words is first tool of tips to write research paper. Research paper writing is an art.A few tips for deciding as strategically as possible about keyword search:

- One should start brainstorming lists of possible keywords before even begin searching. Think about the most important concepts related to research work. Ask, "What words would a source have to include to be truly valuable in research paper?" Then consider synonyms for the important words.
- It may take the discovery of only one relevant paper to let steer in the right keyword direction because in most databases, the keywords under which a research paper is abstracted are listed with the paper.
- One should avoid outdated words.

Keywords are the key that opens a door to research work sources. Keyword searching is an art in which researcher's skills are bound to improve with experience and time.

Numerical Methods: Numerical methods used should be clear and, where appropriate, supported by references.

Acknowledgements: Please make these as concise as possible.

References

References follow the Harvard scheme of referencing. References in the text should cite the authors' names followed by the time of their publication, unless there are three or more authors when simply the first author's name is quoted followed by et al. unpublished work has to only be cited where necessary, and only in the text. Copies of references in press in other journals have to be supplied with submitted typescripts. It is necessary that all citations and references be carefully checked before submission, as mistakes or omissions will cause delays.

References to information on the World Wide Web can be given, but only if the information is available without charge to readers on an official site. Wikipedia and Similar websites are not allowed where anyone can change the information. Authors will be asked to make available electronic copies of the cited information for inclusion on the Global Journals Inc. (US) homepage at the judgment of the Editorial Board.

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21. Arrangement of information: Each section of the main body should start with an opening sentence and there should be a changeover at the end of the section. Give only valid and powerful arguments to your topic. You may also maintain your arguments with records.

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23. Multitasking in research is not good: Doing several things at the same time proves bad habit in case of research activity. Research is an area, where everything has a particular time slot. Divide your research work in parts and do particular part in particular time slot.

24. Never copy others' work: Never copy others' work and give it your name because if evaluator has seen it anywhere you will be in trouble.

25. Take proper rest and food: No matter how many hours you spend for your research activity, if you are not taking care of your health then all your efforts will be in vain. For a quality research, study is must, and this can be done by taking proper rest and food.

26. Go for seminars: Attend seminars if the topic is relevant to your research area. Utilize all your resources.

27. Refresh your mind after intervals: Try to give rest to your mind by listening to soft music or by sleeping in intervals. This will also improve your memory.

28. Make colleagues: Always try to make colleagues. No matter how sharper or intelligent you are, if you make colleagues you can have several ideas, which will be helpful for your research.

29. **Think technically:** Always think technically. If anything happens, then search its reasons, its benefits, and demerits.

30. Think and then print: When you will go to print your paper, notice that tables are not be split, headings are not detached from their descriptions, and page sequence is maintained.

31. Adding unnecessary information: Do not add unnecessary information, like, I have used MS Excel to draw graph. Do not add irrelevant and inappropriate material. These all will create superfluous. Foreign terminology and phrases are not apropos. One should NEVER take a broad view. Analogy in script is like feathers on a snake. Not at all use a large word when a very small one would be

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33. Report concluded results: Use concluded results. From raw data, filter the results and then conclude your studies based on measurements and observations taken. Significant figures and appropriate number of decimal places should be used. Parenthetical remarks are prohibitive. Proofread carefully at final stage. In the end give outline to your arguments. Spot out perspectives of further study of this subject. Justify your conclusion by at the bottom of them with sufficient justifications and examples.

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Key points to remember:

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- Write your paper in the form, which is presented in the guidelines using the template.
- Please note the criterion for grading the final paper by peer-reviewers.

Final Points:

A purpose of organizing a research paper is to let people to interpret your effort selectively. The journal requires the following sections, submitted in the order listed, each section to start on a new page.

The introduction will be compiled from reference matter and will reflect the design processes or outline of basis that direct you to make study. As you will carry out the process of study, the method and process section will be constructed as like that. The result segment will show related statistics in nearly sequential order and will direct the reviewers next to the similar intellectual paths throughout the data that you took to carry out your study. The discussion section will provide understanding of the data and projections as to the implication of the results. The use of good quality references all through the paper will give the effort trustworthiness by representing an alertness of prior workings.

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· Present your points in sound order

· Use present tense to report well accepted

· Use past tense to describe specific results

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- Significant conclusions or questions that track from the research(es)

Approach:

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- Present a justification. Status your particular theory (es) or aim(s), and describe the logic that led you to choose them.
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Approach:

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- If use of a definite type of tools.
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Approach:

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- Skip all descriptive information and surroundings - save it for the argument.
- Leave out information that is immaterial to a third party.

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The principle of a results segment is to present and demonstrate your conclusion. Create this part a entirely objective details of the outcome, and save all understanding for the discussion.

The page length of this segment is set by the sum and types of data to be reported. Carry on to be to the point, by means of statistics and tables, if suitable, to present consequences most efficiently.You must obviously differentiate material that would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matter should not be submitted at all except requested by the instructor.

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Approach

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Abstract	Clear and concise with appropriate content, Correct format. 200 words or below	Unclear summary and no specific data, Incorrect form Above 200 words	No specific data with ambiguous information Above 250 words
Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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