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Assessment of Economic Viability for PV Based Hybrid Energy System in West Coast of Turkey

By Mustafa Engin & Dilşad Engin
Ege University

Abstract - In this paper, a pre-feasibility study of using PV-based hybrid energy system to provide electricity to a residential area in west coast of Turkey is examined. The selected case study represents a power demand of 12.6kWh day-1 with a 2.9 kW peak power demand. The power system used in this study contains diesel generator, grid connection and PV modules with backup storage. The energy system was redesigned and optimized as PV based in order to meet the existing user's power demand at a minimum cost of energy. Temperature and solar radiation data obtained from Ege University meteorology station has been used in the simulation process through optimization software, HOMER. Three systems that were considered in this study area are stand-alone PV-diesel, stand-alone PV-battery and grid connected PV system. The proposed systems then were compared regarding on their operational characteristics and cost values. The comparisons prove that grid connected PV energy system had the lowest total net present cost and cost of energy, $53,197 and $0.57/kWh, respectively that makes it the most cost effective system and followed by PV-diesel and stand-alone PV-battery system. It can be concluded that the renewable-based system can become a favorable system without aid from the grid system and bring advantage in technical and economic point of view and also suitable to be applied in the residential application as energy supply if only the current cost of PV arrays and battery system technology have been reduced to its minimum rate.

Keywords : *photovoltaic, renewable energy, hybrid system*

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Assessment of Economic Viability for PV Based Hybrid Energy System in West Coast of Turkey

Mustafa Engin [α] & Dilşad Engin [σ]

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I. Introduction

The technologies for power production from renewable energy sources such as solar are available and reliable. The rapid decrease in the PV module cost during the past few years and the recent escalation in the price of conventional petrochemical fuels used for generating electricity, resulted in the wider usage of PV based energy systems. The advantages of using solar resources to generate electricity include the avoidance of pollutant emissions, silent operation. The amount of annual solar energy reaching the Earth's surface is about 10,000 times more than annual global energy demand [1].

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Recently, in order to reach sustainable development, humankind needs to be steady on the path of low-carbon society. For this reason, in order to make an efficient use of electrical energy there is a growing interest in optimizing the design of urban settlements by means of the exploitation of natural sources of energy and the development of building management systems [2]. Additionally, electrical power nets are in a transition stage where these need to be more flexible and dynamical at all levels, from power generation plant to customer level in order to enable distributed generation, to promote efficient use of energy at customer level, and to reach an intelligent demand response [3], [4]. The generation of electrical energy through of alternative sources such wind and solar, has become more attractive [5], [6] and is widely used for substituting fossil fuels in the process of electrical power energy since 1970s because of the crisis oil [7]. Nevertheless, such alternative energy sources have a slow development [8], and the transition into a new phase of evolution in the electrical power generation sector appears to be a complex task because of the different insights of the problem [9], not only due to environmental, and economic issues, also because of social and psychological impacts on people's behavior [10]. Although PV systems are an expensive option of generating electricity when compared to other systems; this technology has been supported due to its potential benefits, which can be classified as customer-related benefits, electric utility-related benefits and environmental benefits. Earning revenue by selling PV electricity can be given as an example for the customer-related benefits. The examples for the electric utility-related benefits are; reduced transmission and distribution costs and losses, peak shaving, and meeting peak demand. CO2 savings, NOX and SO2 savings can be listed as the environmental benefits of PV systems [11].

At the beginning of 2011, Turkish parliament adopted a new feed-in tariff policy of equally limited duration of 10 years, and equally limited objectives of 600 MW of total capacity. The feed-in tariffs for solar photovoltaic (PV), the most costly of the new renewable technologies, are only US$0.13/kWh. One divergence from previous policy, Turkey will now offer incentives for hardware 'Made in Turkey'. Solar PV systems made in Turkey would qualify for a bonus payment of nearly

US$0.07/kWh [12]. Industry observers have widely penned the new program to be insufficient to create the volume necessary to attract manufacturing.

The present study is proposed to design a PV based hybrid energy system to provide electricity for a residential house in İzmir, Turkey. The system simulation performed to estimate its operational characteristics, such as annual electricity production, annual loads served, excess electricity and capacity shortage. The proposed systems then were compared concerning on their operational characteristics and cost value in order to meet the user's power demand at a minimum cost of energy.

II. Hybrid Power System

A hybrid energy system generally consists of a primary renewable source working in parallel with a standby secondary non-renewable module or grid and storage units. The energy system components are PV module, diesel generator, grid, battery and power converter. Description of these components is given in the following sections.

a) Electrical Loads

The demand for electricity in each area is different and therefore depends on numerous factors, such as the price of electricity, the weather conditions, the time of day, the type of day and the season. The load profiles describe the variation of the electricity demand with time. The hourly load profile provides crucial information on how electricity is used, and thus on where and what demand side management strategies could be potentially effective. Demand side management is the process of managing the consumption of energy to optimize available and planned generation resources.

There are six generic load shape objectives that can be considered during demand-side management planning, namely peak clipping, valley filling, load shifting, strategic conservation, strategic load growth, and flexible load shape. The desired changes in the load shape can be obtained by shifting load to a less expensive time period, or by substituting another resource for delivered electricity such as solar PV/Battery systems. [13].

The data were taken from a small house which is located in Izmir near to solar energy institute building. The electrical load components include fluorescent lamps, ceiling fan, television, refrigerator, air conditioner, and also washing and dish washer machines which are the main components for a small house. The home owner uses demand side management by shifting load to inexpensive hours. The seasonal and daily profiles of household electricity demand which is measured power are presented in (Figure 1) and (Figure 2) respectively.

b) Solar Radiation Resources

Renewable energy sources are intermittent and naturally available due to these factors our first choice to meet household electric demand will be solar energy. Weather data are important factor for pre-feasibility study of PV based hybrid energy system for any particular site [14]. Hourly solar radiation data for year 2010 was collected from solar-wind meteorological station which is located on the roof of the Vocational School Building in Ege University for determining the local potentials of both solar and wind energy [15]. Using this data, the monthly average daily solar radiation and calculated clearness index are plotted in (Figure 3).

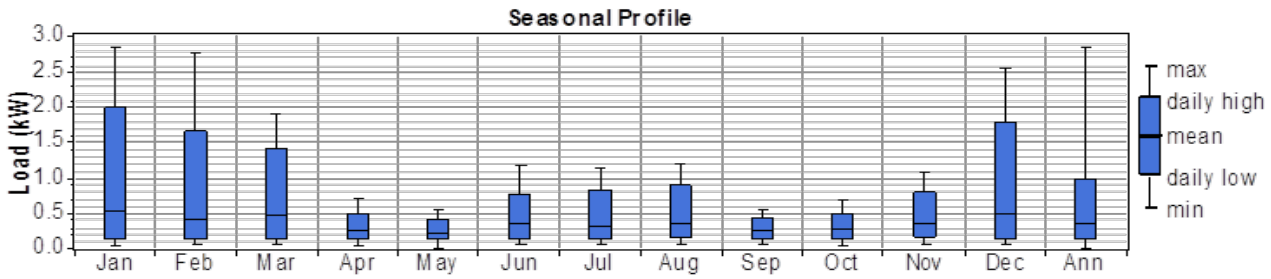


Fig.1 : Seasonal profile of sample household electricity demand.

c) PV based Hybrid System Components

The installation cost of PV arrays may vary from $3.38 - $3.02 /W. A 1 kW solar energy system installation and replacement costs are taken as $3380 and $3000, respectively [16]. In this study, various sizes were considered, ranging from 0-13.5 kW. The lifetime of the PV arrays are taken as 25 years and no tracking system was included in the PV system.

Battery bank is used as a backup system and it also maintains constant voltage across the load. The battery pack consists of 6V, 360 Ah batteries connected in series of 6. For a 1 kWh battery pack, the installation and replacement costs were taken as $213 and $200, respectively [16]. During simulation, different sizes of batteries capacity (0 through 50 kWh) were considered. Lifetime of a unit was considered to be 10 years with an efficiency of 85%.

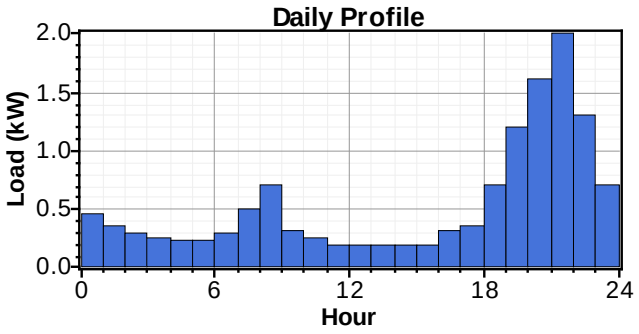


Fig. 2 : Daily profile of sample household electricity demand.

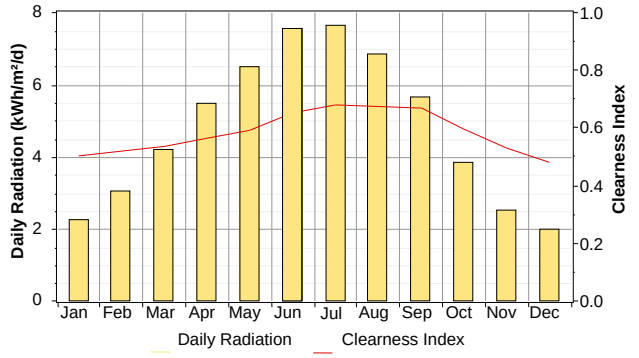


Fig. 3 : Monthly average daily radiation and clearness index.

A power electronic converter needs to maintain flow of energy between the ac and dc components. For a 1 kW system the installation and replacement costs were taken as $715 and $700, respectively [16]. Ten different sizes of converters (0, 1, 2.5, 3, 3.5, 4, 4.5, 5 and 7 kW) were considered for the simulation. Lifetime of a unit was considered to be 15 years with an efficiency of 95%.

d) Homer

HOMER is an optimization software package which simulates varied renewable energy sources system configurations and scales them on the basis of net present cost which is the total cost of installing and operating the system over its lifetime [17]. It firstly assesses the technical feasibility of the RES system. Secondly, it estimates the NPC of the system. HOMER models each individual system configuration by performing an hourly time-step simulation of its operation for one year duration. The available renewable power is calculated and is compared to the required electrical load. Following calculations of one-year duration, any constraints on the system imposed by the user are then assessed; e.g. the fraction of the total electrical demand served or the proportion of power generated by renewable sources. Net present cost (NPC) represents the life cycle cost of the system. The calculation assesses all costs occurring within the project lifetime, including initial set-up costs, component replacements within the project lifetime, maintenance and fuel. Future cash flows are discounted to the present. HOMER assumes that all prices escalate at the same rate, and applies an annual real interest rate rather than a nominal interest rate. NPC estimation in HOMER also takes into account salvage costs, which is the residual value of power system components at the end of the project lifetime.

III. Result and Discussion

Two different PV based hybrid energy systems are investigated. First one is stand-alone PV based hybrid energy system. In this scenario, household load is supplied with solar energy. HOMER model of the system is given in (Figure 4-a). Second one is PV grid-connected hybrid energy system. In this scenario, household load is supplied with solar energy system connected to the grid. HOMER model of the investigated system is given in (Figure 4-b). In this case, if solar energy is not enough to supply the household load, the needed energy is supplied by purchasing energy from the grid. Otherwise, if the energy produced by PV arrays excesses the energy demand of household, the excess electrical energy production is sold to the grid.

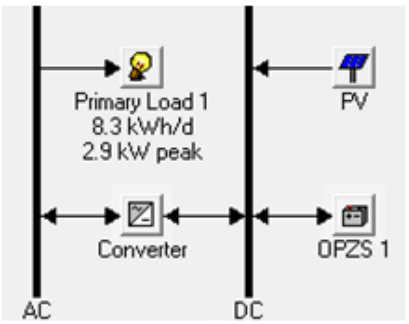
The above proposed PV based hybrid energy systems supply the power to the household continuously throughout the year. For the analysis of these hybrid systems, consider three sensitivity variables: solar irradiation, temperature and renewable energy fraction. For each of the sensitivity values, simulate all the systems in their respective. An hourly time series simulation and configuration for every possible system type is done for a one-year period. A feasible system is defined as a solution for hybrid system configuration that is capable of meeting the load demand of household. It also allows a number of parameters to be displayed against the sensitivity variables for identifying an optimal system type.

According to the first scenario, net present cost values of optimal system solution for stand-alone system components are given Table 1. Monthly average electricity production of stand-alone PV based hybrid energy system for household demand is shown in (Figure 4). From the simulation results, the installation of PV based hybrid system stand-alone configuration is not suitable for power solutions of residential application in İzmir region. Considering present cost analysis of a PV based hybrid system, stand-alone configuration is suitable for loads which stand more than 10 km far away from the grid. Total net present cost (NPC), capital cost and cost of energy (COE) for such a system is $36,150, $27,469 and $0.940/kWh respectively.

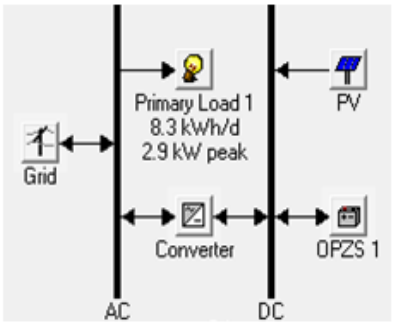
In the second scenario, for the grid connected PV based hybrid energy system, two different solutions are obtained as optimal system configurations. First one is defined according to the lowest energy cost and

second one is defined with the highest renewable energy fraction. During simulation, energy purchase price and sellback prices are used as \$0.198/kWh, \$0.13/kWh [18] respectively. In the first solution, detailed annual electricity production by grid-connected hybrid system components is shown in (Figure 6) and net present cost values of optimal system solution for grid connected configurations are given Table 2. Total net present cost (NPC), capital cost and cost of energy (COE) for grid-connected system is \$8,073, \$3,735 and \$0.208/kWh respectively.

For the second solution, that has the highest renewable fraction with lowest cost of energy, optimal system component size and cost values are given in (table 3) whereas detailed annual electricity production by grid-connected hybrid system components is shown in (figure 7). In this solution, energy cost is obtained as \$0.442/kWh with 87% renewable fraction. If we compare this cost of energy which is obtained from grid connected hybrid systems solution with Turkish utility (\$0.198/kWh) and fed-in tariff prices (\$0.13 kWh), it is relatively high.



(a)



(b)

Fig. 4 : HOMER model of (a) Stand-alone (b) PV-grid connected hybrid energy systems.

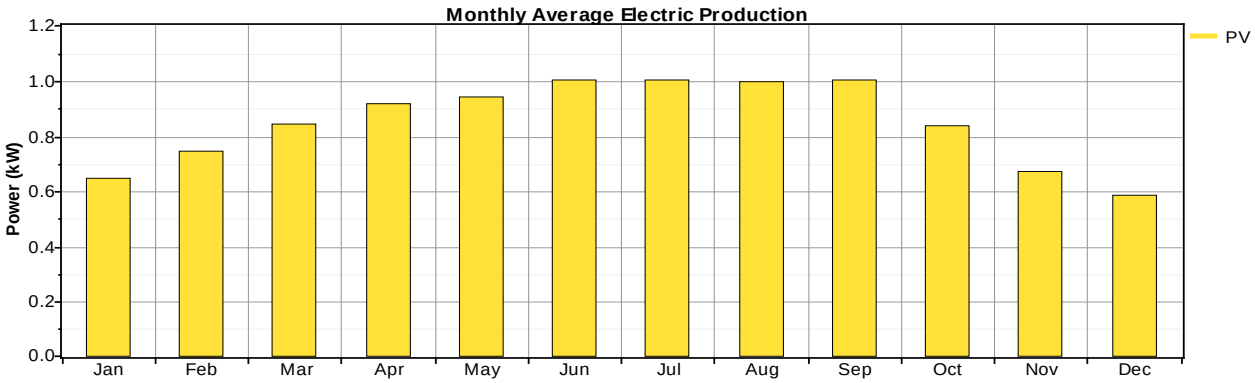


Fig. 5 : Monthly average electricity production of stand-alone PV based hybrid Energy System.

Table 1 : Net present cost of stand-alone system.

Component	Capital ($)	Replacement ($)	O&M ($)	Fuel ($)	Salvage ($)	Total ($)
PV	15,100	0	64	0	0	15,164
STATIONARY BATTERY	10,224	8,772	307	0	-1,174	18,128
Converter	2,145	876	0	0	-163	2,858
System	27,469	9,648	371	0	-1,337	36,150

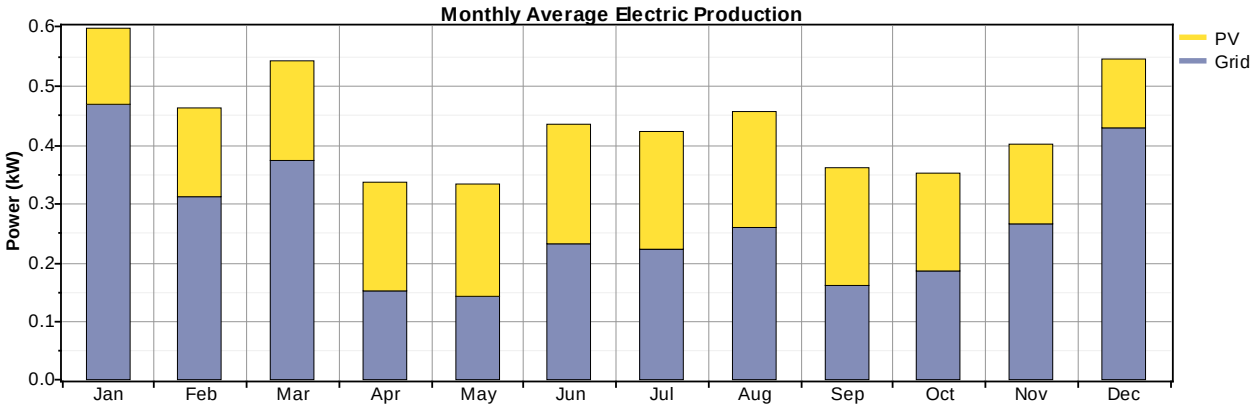


Fig. 6 : Monthly average electricity production of grid-connected PV based hybrid Energy System.

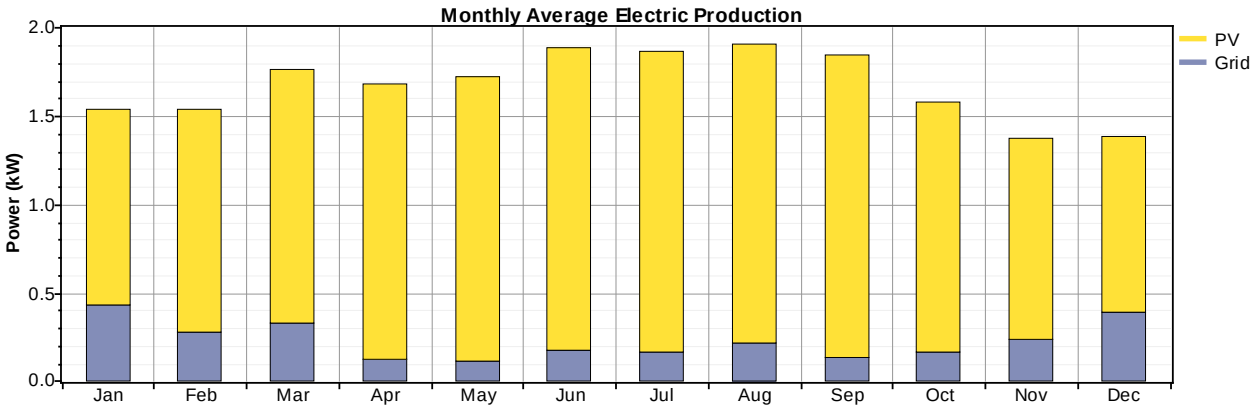


Figure 7 : Monthly average electricity production of grid-connected PV based hybrid Energy System.

Table 2 : System component size and net present cost of grid-connected system with lowest energy cost.

Component	Size	Capital ($)	Replacement ($)	O&M ($)	Fuel ($)	Salvage ($)	Total ($)
PV	1 kW	3,020	0	13	0	0	3,033
Grid	-	0	0	4,087	0	0	4,087
Converter	1 kW	715	292	0	0	-54	953
System		3,735	292	4,100	0	-54	8,073

Table 3 : System component size and net present cost of grid-connected system with highest renewable fraction.

Component	Size	Capital ($)	Replacement ($)	O&M ($)	Fuel ($)	Salvage ($)	Total ($)
PV	9 kW	27,180	0	115	0	0	27,295
Grid	1 kW	0	0	-15,859	0	0	-15,859
Converter	6 kW	4,290	1,753	0	0	-326	5,716
System	-	31,740	1,753	-15,744	0	-326	17,152

II. Conclusion

Alternative power solutions are not commonly used in residential applications in cities today, but are actively used for remote and isolated areas worldwide. The circumstances of each site are studied in order to decide the feasible combination of alternative energy resources. With the aid of above mentioned pre-feasibility study, the PV based hybrid energy system is found to be an inadequate power solution for household electricity demand for the selected site over conventional grid connection. Although the net present cost is high, the running and maintenance costs are low as compared to the grid connection. With decreasing PV module prices, payback times on the PV based hybrid energy system investment are continuously decreasing. Considering operating and maintenance costs, an autonomous site powered by PV based hybrid system pay-off after 6-8 years in a good sunny location. Also newly announced Turkish grid connected PV feed-in tariff prices will descend to a feasible level for investor.

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Matrix Laboratory (MATLAB) as an Efficient Pedagogical Tool for Engineering Education, Teaching and Research

By B.J. Robert, O.I.Okoro, E.I. Igweonu & C.V. Eguzo
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Abstract - Matrix laboratory can assist the teaching and research of engineering and science education. This paper mirrors how the tedious analytical method of arriving at a solution of mechanical systems and electrical transients can be made less burdensome using MATLAB. The simulated results show that velocity changes with displacement and time. It also highlighted the frictional force or air viscosity inherent in the system as a result of acceleration or retardation and further exhibited the effect of transients on circuit charge and current respectively. The values of this pedagogical tool will enhance a better comprehension of mechanical and electrical systems.

Keywords : *MATLAB, Mechanical, System, Transient, Electrical, Analysis.*

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Keywords : MATLAB, Mechanical, System, Transient, Electrical, Analysis.

I. Introduction

The application of science in the design, planning, construction and maintenance of manufactured entity is called Engineering. Engineering education is the training of engineers for the purposes of initiating, facilitating and implementing the technological development of a nation. In Nigeria, the training of engineers has witnessed formidable challenges ranging from poor funding to inadequate facilities, loss of qualified human capacity due to the brain drain syndrome and poor staff training and retention profiles. Other challenges include an almost non-existence of university/industry partnership, defective curricula, traditional approach to teaching, poorly equipped laboratories, and poorly developed local codes and monitoring standards for the training of prospective engineers as well as inadequate ICT environment[1].

Technological advancement serves as a major key to a nation's development. On the other hand, proper engineering knowledge (acquired through appropriate structures) plays a major role in the attainment of a high level of technological advancement. Most developing countries find it difficult to impact adequate knowledge and training to engineers at different levels of training [2].

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Today technology has permeated every aspect of social life and virtually everything revolves around it. For a developing country like Nigeria, engineering education thus assumes vital importance in the development of relevant technology for societal growth. This kind of education is obtained by attendance of a tertiary institution, a university, college or polytechnic. Since technology is constantly being updated and improved in other parts of the world, the challenge of this millennium for engineering education in Nigeria requires our learning systems to undergo changes so that engineering graduates will be equipped to cope with these global changes and societal needs [3].

As part of the changes in the learning system, matrix laboratory (MATLAB) was introduced as it plays an important role in the design, analysis and evaluation of engineering and sciences problems.

MATLAB was designed and developed for engineering and science applications by Math Works Inc and is a widely used simulator. The combination of analysis capabilities, flexibilities, reliability and powerful graphics makes MATLAB the premier software package for engineers and scientists .The most important feature of MATLAB is its programming capability, which is very easy to learn and to use, and which allows user-developed functions.

In the light of the above, MATLAB was applied in steady and transient states thermal analysis of induction machine at blocked rotor operation [4], software simulation techniques for teaching communication systems [5] etc.

The authors hence applied MATLAB as a pedagogical tool in analysis of electrical transients and mechanical systems.

II. Analysis of Mechanical Systems

MATLAB program for handling and improving mechanical systems was developed using the state variable equations which describe the spring-mass system shown in figure 1 and can be written in vector-matrix form as in equation (1).

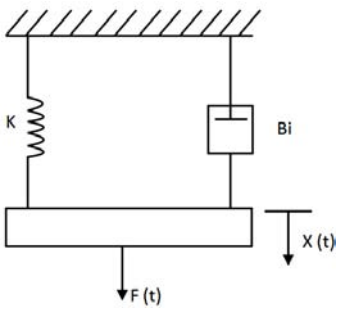

Figure 1 : Spring-Mass System

$$\begin{bmatrix}\dot{X}_1(t)\\ \dot{X}_2(t)\end{bmatrix}=\begin{bmatrix}0 & 1\\ \frac{-K}{M} & \frac{-B_1}{M}\end{bmatrix}\begin{bmatrix}X_1(t)\\ X_2(t)\end{bmatrix}+\begin{bmatrix}0\\ \frac{1}{M}\end{bmatrix}F(t) \quad (1)$$

III. Analysis of Electrical Transients

The most important mathematical operations in electrical transients which gives rise to differential equation is the investigation of when the transient state has passed, giving way to a steady state. MATLAB was applied in figure 2 to solve transient problems in R-L-C electrical circuit. The MATLAB program was developed using the developed equations.

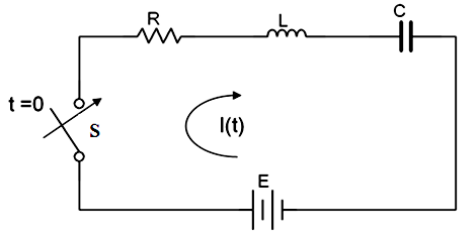

Figure 2 : R-L-C Circuit

$$R_i + L\frac{di}{dt} + \frac{1}{C}\int idt = V(t) \quad (2)$$

With $V(t) = E$ (a DC Voltage) and

Substituting $i = \frac{dQ}{dt}$ and dividing by L,

We can rewrite equation (2) in terms of charge Q as

$$\frac{d^2Q}{dt^2} + \frac{RdQ}{Ldt} + \frac{1}{LC}Q = \frac{E}{L} \quad (3)$$

First, we reduce the given expression:

$$\frac{d^2Q}{dt^2} + \frac{2dQ}{dt} + Q = 0.375 \quad (4)$$

into two first order differential equations:

Let us define $X_1 = Q$

$$X_2 = \dot{Q}$$

$$\dot{X}_2 = \ddot{Q}$$

$$\therefore \dot{X}_1 = \dot{Q} = X_2 \quad (5)$$

The given expression becomes:

$$\dot{X}_2 = 0.375 - X_1 - 2X_2 \quad (6)$$

Where $X_1 = charge$

$X_2 = current$

We now use equations (5) and (6) to develop the MATLAB function program.

IV. Development of Matlab Scripts

Mechanical system and Electrical transient algorithm of a spring-mass system and R-L-C circuit respectively has been developed using the MATLAB package version 7.5.

a) Tutorial 1- Mechanical Systems

MATLAB was applied to the spring-mass system in Figure 1 initially at rest, a force of 40 Newtons is applied at time t=0. Assume that the mass M=2kg, frictional coefficient B1= 2.5N/m/sec and the spring constant K=10N/m. A MATLAB test program to computes the displacement (X1) and velocity(X2) of the system at t=0(0.02) 15.0 with the initial conditions at X1(0) = X2(0) = 0 was developed and shown in Table 1 and Table 2.

Table 1 : MATLAB Function Program

```
%Function file that defines the given function
%save as example 1.m
%represent the function as xDot=Ax+Bu
function xDot=example1(t,x)
xDot=zeros(2,1);
x1=[x(1); x(2)];
B1=2.5;
k=10;
F=40;
M=2;
A=[0 1;-k/M -B1/M];
B=[0; 1/M];
U=F;
xDot=A*x1+B*U;
```

Table 2 : MATLAB Calling Program

```
%calling program that evaluates the function
from t=0 to t=3.0 save as
%example 1a.m
t0=0;
tf=15;
tinterval=0.02;
x0=[0 0];
tspan=t0:tinterval:tf;
[T,x]= ode23('example1',tspan,x0);
% we now generate the first graph
figure(1)
plot(T,x(:,1),'k')
grid on
xlabel('Time[s]')
ylabel('Displacement,Velocity')
hold on
plot(T,x(:,2),'ok')
legend('Displacement','Velocity')
figure(2)
plot(x(:,1),x(:,2),'k')
grid on
xlabel('Displacement')
ylabel('Velocity')
title('Graph of Velocity against Displacement')
```

b) Tutorial 2- Transients in R-L-C Circuit

MATLAB was applied to a series R-L-C circuit in Figure 2 in which both the charge Q and the current are initially zero and contains the elements R=8Ω, L=4H, C=0.25F. If a constant voltage E=1.5V is suddenly switched into the circuit current and charge against time at t=0(0.01)10. A MATLAB program to perform this was developed and also shown in Table 3 and Table 4.

Table 3 : MATLAB Function Program

```
%function file that defines equations ( 5)
and (6)
%save as exaple2.m
function dx = example2(t,x);
dx = zeros(2,1);
dx(1) = x(2);
dx(2) = 0.375-x(1)-2*x(2);
dx = [dx(1);dx(2)];
```

Table 4 : MATLAB Calling Program

```
%calling program that evaluates the functions to
save as 2a.m
t0 = 0;
tf = 10;
tinterval = 0.01;
tspan=t0:0.01:tf;
x0 = [0 0];
[t,x] = ode45('example2',tspan,x0);
% we now plot the graphs
Q = x(:,1); % charge
I = x(:,2); % current
figure (1)
plot (t,Q,'k')
grid on
xlabel('Time[s]')
ylabel ('Charge[c]')
figure (2)
plot(t,I,'k')
grid on
xlabel('Time[s]')
ylabel('Current[A]')
```

V. Simulated Results and Discussions

The system output for spring-mass system and electrical transients are shown in figures 1, 2, 3 and 4 respectively.

Figure 1 shows velocity-displacement graph for the spring-mass system. It is seen that the mass is displaced from zero metre till it attains its full velocity at 2s. The spring-mass system finally decelerates to zero at 4s. Furthermore, in figure 2 the velocity changes as well as displacement after one second and two seconds respectively followed by a deceleration and a struggle for stability due to external or built-in influences until stability is maintained after seven seconds. Considering figure 3, it is seen that the circuit charge rises steadily from zero second and remains constant after six seconds. Likewise current rises steadily from zero second to one second after which there is a sharp fall due to transients and remains constant after eight seconds.

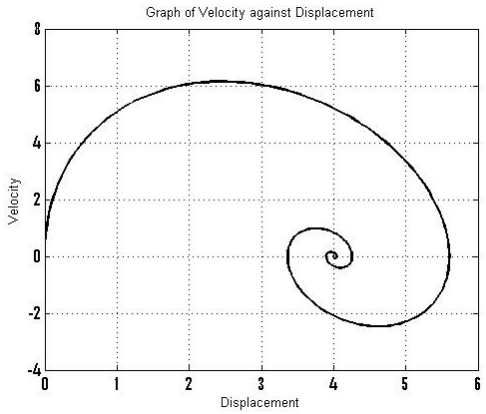

Figure 1 : System Response for Spring-Mass System

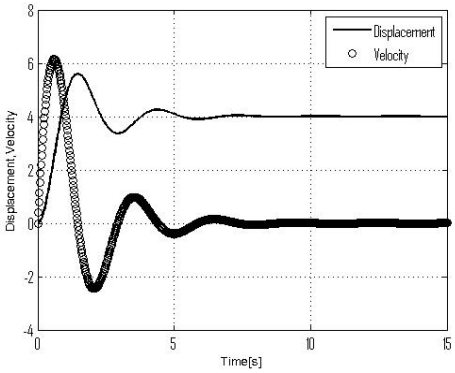

Figure 2 : System Response for Spring-Mass System

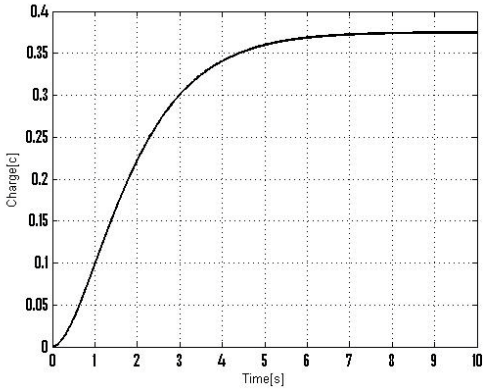

Figure 3 : System Response for Electrical Transients

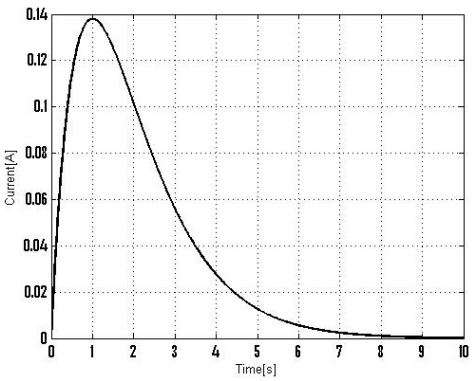

Figure 4 : System Response for Electrical Transients

VI. Conclusion and Recommendations

The potentials of MATLAB in teaching and research have been explored and certified very efficient in solving wide range of engineering and science problems. It has been shown that the use of MATLAB software package in mechanical systems and electrical transients could make their analysis less tedious, more accurate and more speedily.

Therefore, in order to encourage the use of this all-important software by students and staff in Nigerian higher institutions, the following recommendations are considered inevitable:

1. MATLAB should be introduced in the nation's engineering faculties and made compulsory for all engineering students.
2. Postgraduate engineering students should be made to carry out one or two projects on MATLAB before embarking on their final thesis.
3. MATLAB groups among students should be encouraged in all the nation's universities. These groups should be involved in discussions about problems encountered and successes made while solving a particular problem.
4. Engineering faculties should encourage their teaching staff to attend workshops/seminars on the recent versions of MATLAB.
5. Calculations and analysis done using MATLAB should be well documented for future references.
6. Inter-university and inter-departmental competitions among students on MATLAB and its programming application should be encouraged to stimulate interest in the use of the software.
7. MATLAB just like any other engineering software, is very expensive for a department to purchase it, therefore Deans of Faculties should be made to bear the financial burden-especially in securing the necessary software toolboxes.
8. COREN and NSE can ensure that recommendation number one is achieved through appropriate legislation.

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Nonlinear Estimation of External Power System Dynamic Equivalent Parameters

By R. Gueddouche & M. Boudour
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Abstract - Based on the concept of the external power system dynamic equivalent for the study system, this paper proposes a novel evolutionary method for the identification of the equivalent's parameters, comparing the answers of the complete network and its equivalent following the small disturbances which emerged in the study system. The proposed method is demonstrated and compared with the original system using the 10 machines 39 buses New England test system. The comparison shows that the proposed approach can preserve all dynamic properties of the original network.

Keywords : *Dynamic equivalents, Dynamic modeling, Genetic algorithm, Nonlinear identification, Multi-machine system, Parameter identification, Power system, Structure preservation.*

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Nonlinear Estimation of External Power System Dynamic Equivalent Parameters

R. Gueddouche [α] & M. Boudour [σ]

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Index Terms : Dynamic equivalents, Dynamic modeling, Genetic algorithm, Nonlinear identification, Multi-machine system, Parameter identification, Power system, Structure preservation.

I. Introduction

Electric power systems have long been perceived and exploited like national entities or regional areas. The interconnections between such zones being mainly used with the aim of help in case of failure in a nearby zone. In the new context of the electricity sector, this situation has changed since the interconnections are increasingly used in order to maximize the exchange of electricity through power exchanges recently introduced. This leads the transmission system operators (TSOs) to operate their systems increasingly close to their limits. In an individual way, each TSO is obliged to re-examine its way of doing the usual studies on its own network. In particular, a more refined modeling of the influence of neighboring systems on its own should be considered. Moreover, the process of extension of the synchronous area which continues today, led to a significant increase in the size of dynamical systems to study. Besides the difficulty posed by the size, new structural phenomena occur from this extension as the electromechanical oscillations of low frequency observed between generators remote network.

Many dynamic equivalence techniques have been developed over the years [1]-[9]. More research focused on coherency equivalents and modal equivalents nowadays, however, they need detailed data of the external system which may be difficult to get in the power market environment. Some estimation methods are based on available information from the boundaries nodes and do not require any knowledge detail of the external network. The classical estimation methods are mainly based on the linearization of the system around an operating point with theoretical constraints validity [10] - [12]. Consequently, they are limited by their validity in nonlinear practical applications, offline and online applications. This paper proposes a new evolutionary approach for estimating parameters to determine a dynamic equivalent model of an external power system from synchronized measurements of disturbance occurred in internal system, which obtained by PMUs (Phasor Measurement Units). This approach was applied to 10 machines 39 buses New England test system [13]. Comparing the properties of the equivalent system with ones of the original system, the result shows that the reduced system can represent dynamic behaviors of the original system well, for any kind of disturbance.

II. Dynamic Equivalents

The equivalent is represented by a model with unknown parameters. In operation, the power system is often perturbed by small random disturbances. The estimation of unknown parameters of the equivalent model is operated by comparing the measurements obtained from the real network, and the same measurements made on the equivalent network by minimizing some objective function.

a) Dynamic equivalent model

The basic requirement of the dynamic equivalents is that the response of the equivalent system can fit the original system dynamically and approximately when faults happen in the internal system. In our equivalent system, equivalent generator represents dynamic effect of the external system on the internal system located at the boundary bus (Fig.1). When there are multiple boundary buses connecting the external system with the internal system, multiple generators are adopted to represent dynamic influence of the external system on the internal system, with an equivalent generator located at each boundary bus [14]. Parameters to be estimated are: X_d,X_q,X'_d,H,D,T'_{do}, voltage regulator gain K_a and its time constant T_a.

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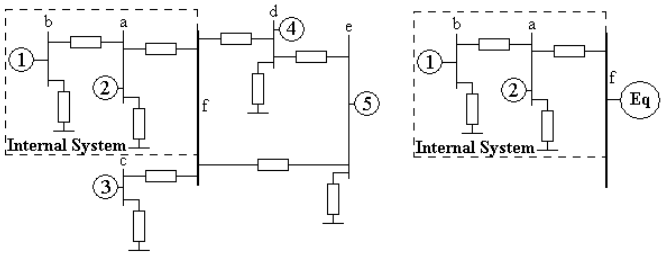

Fig. 1.a : Original System *Fig. 1.b :* Equivalent System

The equivalent generator model can be expressed by the following equations:

$$\dot{\omega} = \frac{1}{2H}(T_m - E'_q I_q + (X_q - X'_d) I_d I_q - D(\Delta\omega - 1)) \quad (1)$$

$$\dot{\delta} = \omega_0(\Delta\omega - 1) \quad (2)$$

$$\dot{E}'_q = \frac{1}{T'_{d0}}(E_{fd} - (X_d - X'_d) I_d - E'_q) \quad (3)$$

$$\dot{E}_{fd} = \frac{1}{T_a}(K_a(V_{ref} - V_t + V_s) - E_{fd}) \quad (4)$$

b) Parameter identification of equivalent model

The parameters identification for nonlinear systems includes deterministic and evolutionary methods. Evolutionary methods offer greater ease of adjustment problems and other advantages over deterministic methods because they:

- Require only the calculation of the objective function, without this last being forced to be continuous or differentiable.
- Easily adaptable to multi-objective problems optimization, and complex systems with very important unknown number of parameter.
- Have great theoretical probability to find the global optimum.
- Offer great simplicity of implementation.

An evolutionary approach based on genetic algorithms is presented in this document, to identify the dynamic equivalent model parameters, by minimizing the range of speed variation, electrical power variation and terminal voltage variation produced in all generators of the internal system between the original and the equivalent system.

i. *Error function*

The original system equations are generally written:

$$\Delta\dot{x} = A\Delta x + B\Delta u$$
$$\Delta y = C\Delta x \quad (5)$$

Where:

A= State matrix ($4m \times 4m$).

B = Control matrix ($4m \times 2m$).

C = Output matrix ($2m \times 4m$).

$$\Delta x = [\Delta\omega_1 \dots \Delta\omega_m \ \Delta\delta_1 \dots \Delta\delta_m \ \Delta E'_{q1} \dots \Delta E'_{qm} \ \Delta E_{fd1} \dots \Delta E_{fdm}]^T$$

$$\Delta u = [\Delta T_{m1} \dots \Delta T_{mm} \ \Delta U_{s1} \dots \Delta U_{sm}]^T$$

$$\Delta y = [\Delta\omega_1 \dots \Delta\omega_m \ \Delta Pe_1 \dots \Delta Pe_m \ \Delta V_{t1} \dots \Delta V_{tm}]^T$$

with :

- $\Delta\delta$ Absolute angle rotor variation (rad. elec/sec).
- $\Delta\omega$ Angular velocity rotor variation (*pu*).
- $\Delta E'q$ Internal voltage variation (*pu*).
- ΔEfd Internal excitation voltage variation (*pu*).
- ΔTm Mechanical torque variation (*pu*).
- ΔUs Order excitation systems variation (*pu*).
- ΔPe Active power variation (*pu*).
- ΔVt Change in terminal voltage generators (*pu*).

The equations describing the dynamic equivalent system are expressed similar to those of the original system (5), but with a simplified structure and less parameters.

$$\Delta\tilde{\dot{x}}(\alpha) = \tilde{A}(\alpha)\Delta\tilde{x}(\alpha) + B\Delta u$$
$$\Delta\tilde{y}(\alpha) = \tilde{C}(\alpha)\Delta\tilde{x}(\alpha) \quad (6)$$

$\tilde{A}(\alpha), \tilde{C}(\alpha), \Delta\tilde{x}(\alpha) et\ \Delta\tilde{y}(\alpha)$, are all functions of α, the equivalent system parameter vector to be identified. Therefore, an error function may be defined by:

$$e(\alpha) = \Delta y - \Delta\tilde{y}(\alpha) \quad (7)$$

Where Δy represents the responses of the original system, which are directly measureable.

And $\Delta\tilde{y}(\alpha)$, must be calculated by simulating the equivalent system with the same disturbance.

ii. *Objective function*

The idea is to minimize the error function (7) between the measure and the model output for all machines belonging to the internal network. The mathematical model of the optimization problem is a multi-objective function and can be formulated as follows:

$$\begin{cases} [min] \ e(\alpha) = [e_1(\alpha), e_2(\alpha), \dots, e_{3(m-nex)}(\alpha)] \\ \alpha > 0 \end{cases} \quad (8)$$

Where:

$$e_i(\alpha) = \sum_{t=to}^{t_{fin}} (|\Delta y_i(t) - \Delta\tilde{y}_i(\alpha, t)|) \ ; \ i = 1,2, \dots, 3(m - nex)$$

By weighting the measurements by a weighting factor λi, our objective function becomes:

$$\begin{cases} [min] \ e(\alpha) = \sum_{i=1}^{3(m-nex)} \left[\lambda_i \sum_{t=to}^{t_{fin}} (|\Delta y_i(t) - \Delta\tilde{y}_i(\alpha, t)|)\right] \\ \alpha > 0 \end{cases} \quad (9)$$

Where:

$$\alpha = [X_d, X_q, X'_d, H, D, T'_{do}, K_a, T_a]$$

$$\Delta y = \left[\Delta\omega_1 \dots \Delta\omega_{m-nex} \;\; \Delta Pe_1 \dots \Delta Pe_{m-nex} \;\; \Delta V_{t1} \dots \Delta V_{t(m-nex)}\right]^T$$

$$\Delta \tilde{y} = \left[\Delta\tilde{\omega}_1 \dots \Delta\tilde{\omega}_{m-nex} \;\; \Delta\widetilde{Pe}_1 \dots \Delta\widetilde{Pe}_{m-nex} \;\; \Delta\tilde{V}_{t1} \dots \Delta\tilde{V}_{t(m-nex)}\right]^T$$

m = number of machines belonging to the complete system.

$m-nex$= number of machines belonging to the study system (internal system).

iii. *Encoding and initial population*

The encoding of individuals is an important parameter in population research methods. These are represented as a strings (chromosomes) containing characters or genes of a predetermined alphabet. There are different ways to code a solution. In our study, the individual is represented by eight parts of chromosome corresponding to the eight parameters to be estimated, each gene (parameter) is represented by its physical value, which means that, the real coding is adopted (fig.2).

The GAs requires an initial population to start search process. Applied methods generate randomly a set of solutions belonging to the following area:

$$\alpha_{min} \leq \alpha \leq \alpha_{max} \qquad (10)$$

Where:

$$\alpha_{min}{}^T = \begin{bmatrix} \frac{\sum_{i=1}^{m-nex} X_{di}}{2(m-nex)} \\ \frac{\sum_{i=1}^{m-nex} X_{qi}}{2(m-nex)} \\ \frac{\sum_{i=1}^{m-nex} X'_{di}}{2(m-nex)} \\ \frac{\sum_{i=1}^{m-nex} H_i}{2(m-nex)} \\ \frac{\sum_{i=1}^{m-nex} D_i}{2(m-nex)} \\ \frac{\sum_{i=1}^{m-nex} T'_{doi}}{2(m-nex)} \\ \frac{\sum_{i=1}^{m-nex} K_{ai}}{2(m-nex)} \\ \frac{\sum_{i=1}^{m-nex} T_{ai}}{2(m-nex)} \end{bmatrix} \quad ; \quad \alpha_{max}{}^T = \begin{bmatrix} \frac{2\sum_{i=1}^{m-nex} X_{di}}{(m-nex)} \\ \frac{2\sum_{i=1}^{m-nex} X_{qi}}{(m-nex)} \\ \frac{2\sum_{i=1}^{m-nex} X'_{di}}{(m-nex)} \\ \frac{2\sum_{i=1}^{m-nex} H_i}{(m-nex)} \\ \frac{2\sum_{i=1}^{m-nex} D_i}{(m-nex)} \\ \frac{2\sum_{i=1}^{m-nex} T'_{doi}}{(m-nex)} \\ \frac{2\sum_{i=1}^{m-nex} K_{ai}}{(m-nex)} \\ \frac{2\sum_{i=1}^{m-nex} T_{ai}}{(m-nex)} \end{bmatrix}$$

The individuals' number in the initial population is chosen such that:

$$N_{ind} > N_{mes} * (m - nex) \qquad (11)$$

Where:

N_{mes} = Number of measures nature considered (ω,Pe,Vt)=3.

m= Total number of machines belonging to the complete network.

nex= Number of machines belonging to the external system.

A representation of *Nind* individuals (solutions) in an initial population is shown in fig.2.

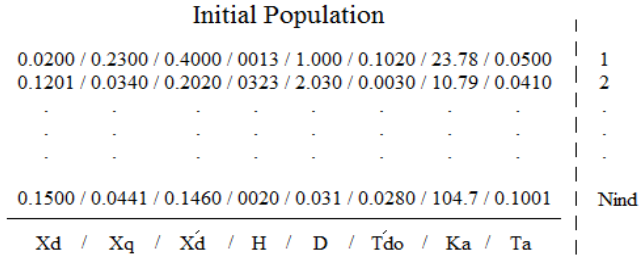

Fig. 2 : Organization and coding of individuals in initial population.

iv. *Evaluation mechanism*

With a fitness function or adaptive function the evaluation is done in a closed interval $[t_o, tf_{in}]$ using each time a new dynamic simulation of the equivalent system for each population individuals.

$$f_i(\alpha) = \lambda_i \sum_{t=to}^{t_{fin}} (|\Delta y_i(t) - \Delta\tilde{y}_i(\alpha, t)|) \qquad (12)$$

Where:

$$\lambda_i = \frac{1}{\sum_{t=to}^{t_{fin}} (|\Delta y_i(t)|)} \quad ; \quad i = 1,2, \dots, N_{mes} * (m - nex)$$

v. *Evolution mechanism*

a. Parents selection

Among initial population individuals, we choose:

- A number of individual « $Nmes* m-nex$ »;

To form a group of (*Local parents*), in which each parent *"i"* satisfied the fitness function minimum:

$$parent_i = \min_{j=1..N_{ind}} [f_i(Ind_j)] \qquad (13)$$

Where:

$$i = 1,2, \dots, N_{mes} * (m - nex)$$

– A number of individual « $Nmes$ » ;

To form a group of (***Global parents***), in which each parent *"k"* satisfied the fitness function minimum:

$$parent_k = \min_{j=1..N_{ind}} \left(\sum_{i=1}^{N_{mes}*(m-nex)} f_i(Ind_j)\right) \qquad (14)$$

Where: $k = 1,2, \dots, N_{mes}$

The local parents group includes the favorable solutions for each type of measure that corresponds to each machine belonging to the internal system. However the global parents group includes the favorable solutions for each type of measure that corresponds to all the machines belonging to the internal system. The population called, *"Parents population"* is made up of the two groups (*Global parents & Local parents*).

b. Multi-parent recombination

Recombination is used mainly in evolutionary strategies. Contrary to k points crossover operators, which exchange information between two parents, the recombination creates the descendants, by weighting many parents components'. We define three weighting operators:

$$Op_1(chr) = \frac{Pr_1(chr)+Pr_2(chr)}{2}$$
$$Op_2(chr) = max\big(Pr_1(chr), Pr_2(chr)\big) + \frac{|Pr_1(chr)-Pr_2(chr)|}{2}$$
$$Op_3(chr) = min\big(Pr_1(chr), Pr_2(chr)\big) - \frac{|Pr_1(chr)-Pr_2(chr)|}{2}$$

Where:

chr : Integer belonging to [1,8], which represents crossed chromosome order.

Pr_1,Pr_2 : Two individuals of local parents group.

We generate $Nind$ individuals for construct the new population (generation) from the two groups' "***local parents***" and "***global parents***", with the following steps:

1. We reproduce the same individuals in the global parents group for construct, N_{ind} individuals of the new population (Fig. 3).

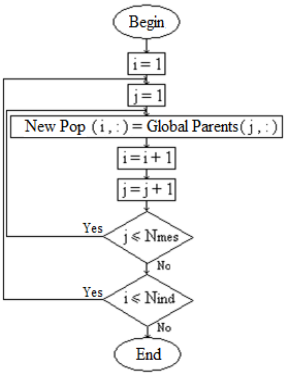

Fig. 3 : New population from the group Global Parents

2. For each individual "/ " belonging to the new population:

- A random integer number of weighted point "k" is generated between 1 and $8*T_{div}$.
- In each weightings j=1,2…,k :
  - we choose a random pair of individuals from the local parents group.
  - a crossed chromosome is chosen randomly « chr ».
  -a random real number, “h”, is generated between 0 and 1, to select the weighting operator (Fig. 4).

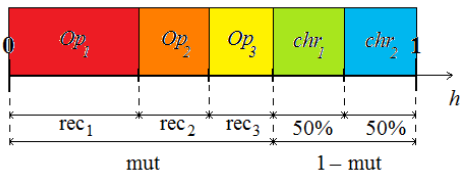

Fig. 4 : Recombination operator distribution's

- the value obtained by the weighting operator is assigned to the individual's chromosome "i(chr)" of the new population, if this value satisfies the constraint:

$$\alpha > 0 \qquad (15)$$

- we move to the next individual "i +1" when the number of weighting point "k" of the individual "i" is complete.

3. Accordance with the procedure for selection of parents, the best individuals evaluated by the fitness function (12) between *parents population* and this *new population*, construct the *new parents population* and clear the *old parents population* for the next generation *(elitist strategy).*

III. Algorithm

The complete algorithm of the proposed method is given below:

Step1 : Introduction of static and dynamic data of the complete system.
Step2 : Power flow calculation, linearization, disturbance choice and network dynamic simulation.
Step3 : Border node choice and equivalent system linear model construction from results of the power flow.
Step4 : Generating the initial population according to the procedure specified in subsection *(III.B.3)*.
Step5 : Run equivalent system dynamic simulation and evaluate all individuals by fitness function (12).
Step6 : Construct the population of parents following the procedure described in paragraph *(III.B.5.a)*, with equations (13,14).
Step7 : While the number of generation has not reached the maximum number N_{gen}:
Step7.1 : Generate the new population using described procedure in paragraph (III.B.5.b).
Step7.2 : Run equivalent system dynamic simulation and evaluate all individuals by fitness function (12).
Step7.3 : Select the new individuals in parents population following described procedure in paragraph (III.B.5.b.3).
Step8 : End while.
Step9 : Select best individuals in parents population with the objective function (9), and display the results.

Table.I, represents the most significant parameters that characterize this algorithm.

Table I : Control Parameters

Control parameters	Definition
N_{ind}	Number of individual in a population
N_{gen}	Maximum number of generation
T_{div}	Weighting rate
rec_1, rec_2, rec_3	Recombination rate
Op_1, Op_2, Op_3	Recombination operator

IV. Application

To validate the proposed approach, developed algorithm was used to build the dynamic equivalent of transmission network IEEE New-England 39 bus [13]. It represents a simplified New England transmission network (northeastern United States) that is part of real U.S. network. This network consists of 10 generators (PGtotal= 6.19 GW, QGtotal= 1.28 GVAr) and 39 bus with 19 load bus. The original system structure is as Fig.5.

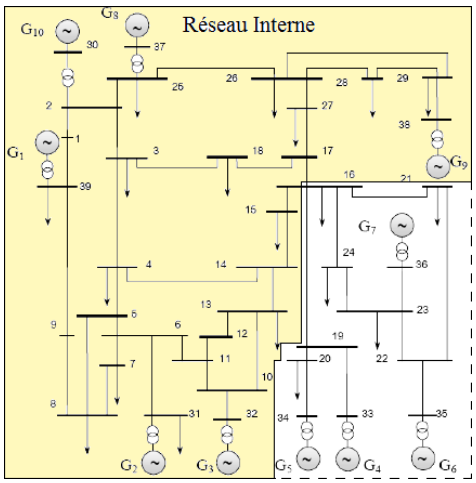

Fig.5 : Original system IEEE-39 bus

In Fig. 5, the shaded part is the internal system and the rest is the external system to be reduced. There are a boundary bus 16 and two tie lines 16-15 and 16-17 between the internal and the external systems. Fig. 6 is the sketch of the equivalent system.

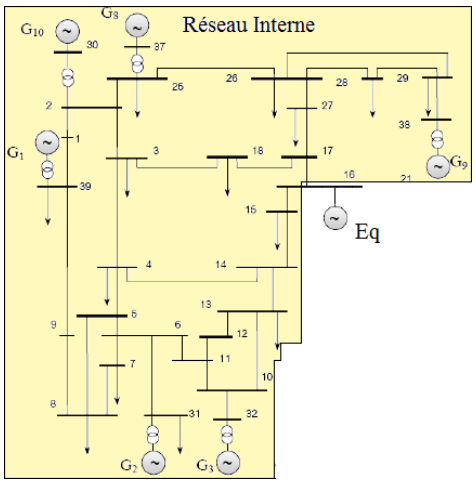

Fig. 6 : Equivalents system

a) Simulation

The network linear model is used by the algorithm for solutions evaluation in estimation procedure. The proposed algorithm programming and dynamic linear model simulation was implemented in Matlab.V7 environment. The algorithm control parameters are summarized in Table II. These parameters were obtained after several tests with an appropriate adjustment.

Table II : Control Parameter Values

Control parameters	Values
N_{ind}	80
N_{gen}	60
$T_{div}(\%)$	100
rec_1, rec_2, rec_3	0.5 , 0.25 , 0.25

To allow a better parameters estimation, different disturbances were applied in different parts of the internal system. Each proposed disturbance has a period of 10s. An event is generated each time to the first second of the simulation. The algorithm verifies the equivalents behavior in period of 10s, by comparing its response with the response of the original system. If the equivalent response exceeds some level relatively to the original systems response in a new disturbance, the equivalent generator parameters are recalculated and updated. Each solution obtained by applying the previous disturbances must be part of the initial population of the next estimation procedure. The estimated parameters of the equivalent generator are presented in Table III.

b) Validation

A small perturbation represented by disconnecting the line 3-18 is applied to bus18 of the equivalent system and the original system respectively at time, t=2s and lasted for about 12 cycles. Time domain dynamic simulations were performed both on the two systems.

Table III : Equivalent Generator Parameters

	Parameter							
Dist.	X_d	X_q	X'_d	H	D	T'_{do}	K_a	T_a
3	0.4718	0.0438	0.0603	135.09	$2.5 \cdot 10^{-5}$	7.8986	155.08	0.0685

Dynamic responses are shown in fig. 7 to fig. 9. The boundary node voltage is shown by fig. 7, The angle of the machine n°10 is shown in fig. 8 and angular velocity of the machine n°8 in fig. 9.

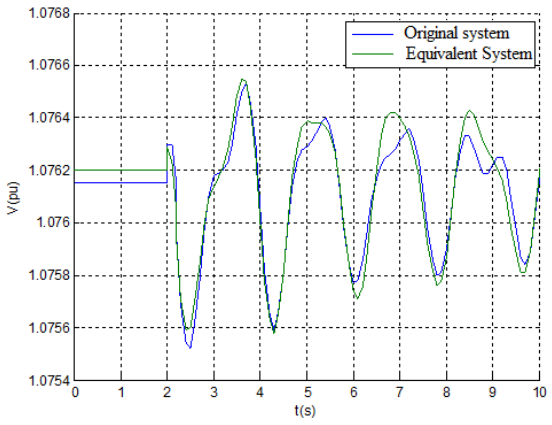

Fig. 7 : Voltage variation at bus 16

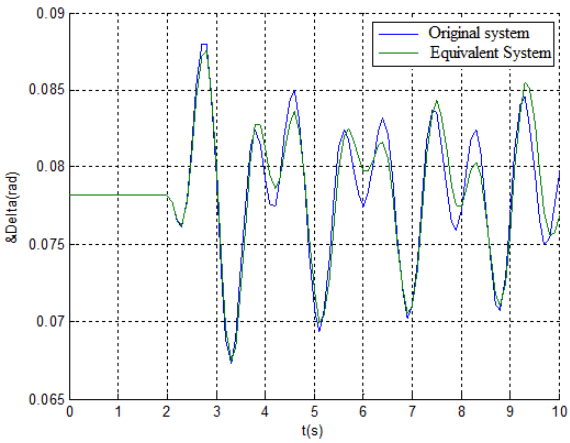

Fig. 8 : Angle of the machine 10

In order to verify the performance of the proposed dynamic equivalent approach in the case of the large disturbances, three-phase fault was applied to bus 30 of the equivalent system and the original system respectively at time t=2s, and the fault lasted for about 3 cycles. Time domain dynamic simulations were carried out on the original system and the equivalent system, and dynamic responses are shown in fig. 10 and fig. 11. The angle of the machine n°10 is shown in fig. 10 and angular velocity of the machine n°8 in fig. 11.

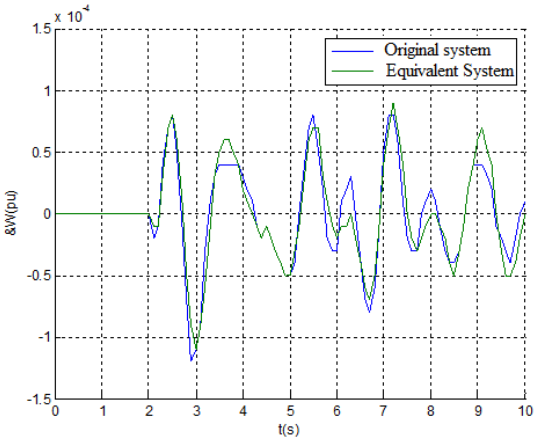

Fig. 9 : Angular velocity rotor variation of machine 8

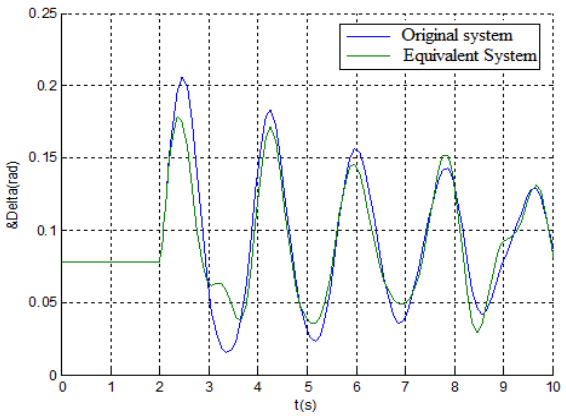

Fig. 10 : Angle of the machine 10

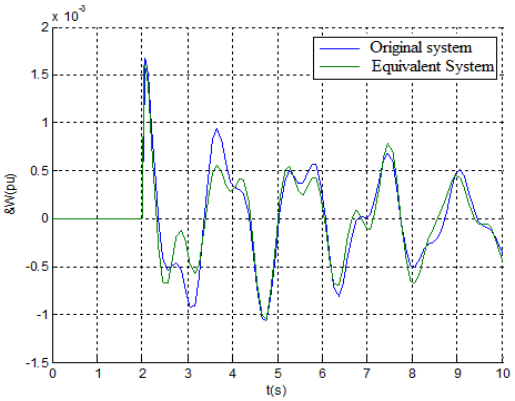

Fig. 11 : Angular velocity rotor variation of machine 8

The simulation results of equivalent system with estimated parameters are encouraging and show the effectiveness of the developed algorithm and the ability of the estimated equivalent to reproduce the influence of the external system on internal system for small and severe disturbances.

V. Conclusion

In this study, we proposed a nonlinear estimation method for parameters, based on an evolutionary algorithm. In order to obtain the external system dynamic equivalent, several dynamic simulation disturbances were applied to increase the accuracy of the model estimated by the developed algorithm. The proposed approach does not require data of external system. This approach requires only configuration information, settings and operating status of the internal system. Dynamic simulation was performed on both the original system and the equivalent system under different operating conditions, and the results show that the obtained equivalent system can represent the main dynamic characteristics of the original system well. Thus, the approach proposed is proved to be feasible and has potential for tackling the complex practical application in power system.

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A Qualitative Approach to Design Multi Channel UART Using FPGA and FIFO Technologies

By C.K.Hemantha Lakshmi, C.K.Hemantha Rama & C.K.Mahesh Babu

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Abstract - To meet modern complex control systems communication demands, my paper presents a multi channel UART controller based on FIFO (first in first out) and FPGA (field programmable gate array).The paper presents design method of asynchronous FIFO and structure of controller.This controller is designed with FIFO circuit block and UART (universal asynchronous teceiver transmitter) circuit block with in FPGA to implement communication in modern complex control systems quickly and effectively. This controller can be used to implement communication when master equipment and slaver equipment are set at different baud rate. It can also be used to reduce synchronization error between sub systems in asystem with several sub systems. The controller is reconfigurable and scalable. The whole scenario is simulated using VHDL coding.

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Strictly as per the compliance and regulations of:

A Qualitative Approach to Design Multi Channel UART Using FPGA and FIFO Technologies

C.K.Hemantha Lakshmi [α], C.K.Hemantha Rama [σ] & C.K.Mahesh Babu [ρ]

Abstract - To meet modern complex control systems communication demands, my paper presents a multi channel UART controller based on FIFO (first in first out) and FPGA (field programmable gate array).The paper presents design method of asynchronous FIFO and structure of controller.This controller is designed with FIFO circuit block and UART (universal asynchronous teceiver transmitter) circuit block with in FPGA to implement communication in modern complex control systems quickly and effectively. This controller can be used to implement communication when master equipment and slaver equipment are set at different baud rate. It can also be used to reduce synchronization error between sub systems in asystem with several sub systems. The controller is reconfigurable and scalable. The whole scenario is simulated using VHDL coding.

I. Introduction

Today, owing to availability of state-of–the–art microcontrollers and digital signal processors(DSPs), complex control algorithms can be easily implemented to attain the desired system performance [3].But in actual control systems it is difficult to attain the expected result for various factors affect the control systems such as control algorithms itself, capability of implement equipment and states of control circumstance. Except those factors, communication parameters of control systems including baud rate, BER (bit error rate) and synchronization between sub systems also engender great effect .In order to improve precision of control system and make good use of modern control algorithms ,we should pay much more attention on communication in control systems[1].

In several control systems, UART a kind of serial communication circuit used widely. A universal asynchronous receive transmit is an integrated circuit which plays most important role in serial communication. It handles the conversion between serial and parallel data. Serial communication reduces the distortion of a signal therefore makes data transfer between two systems separated in great distance possible[2].

In some complex systems, communications between the master controller and slaver controllers are implemented by serial or parallel port. Parallel communication needs a lot of multi-bit address bus and data bus and it is only convenient for short distance transmission. Serial communication is another way of communication used extensively because of its simple structure and long transmission distance .But sometimes a common serial port could not meet requirements of complex systems with different baud rates equipments even some special baud rate equipments. It is impossible to implement this multi baud rate communication system without a special baud rate converter[3].

a) Proposed system is

- RTL design and verification of RS 232.
- Interfacing digital clock manager.

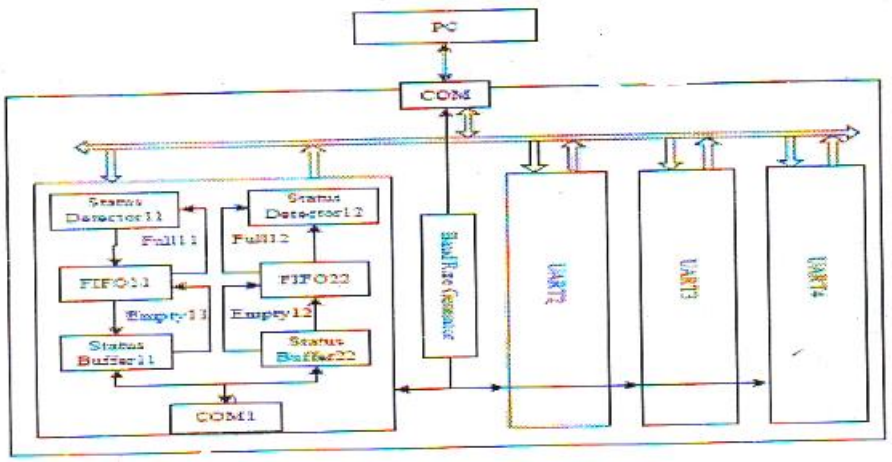

Figure 1 : Multi Channel UART

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II. Design Implementation

a) Designing of Asynchronous FIFOs

An asynchronous FIFO refers to a FIFO design where data values are written to a FIFO buffer from one clock domain and data the data value are read from the same FIFO buffer from another clock domain, where the two clock domains are asynchronous to each other. FIFOs are always used for data cache, storing differences of frequency or phase of asynchronous signals. Asynchronous FIFOs are often used to quickly and safely pass data from one clock domain to another asynchronous clock domain. In asynchronous clock circuit, periods and phases of each clock domain are completely independent so the probability of data loss is always not zero.

b) Structure of Asynchronous FIFO

A FIFO consists of a RAM array block status block writer pointer (WR_ptr) and a read pointer (RD_ptr) and its structure is shown below figure

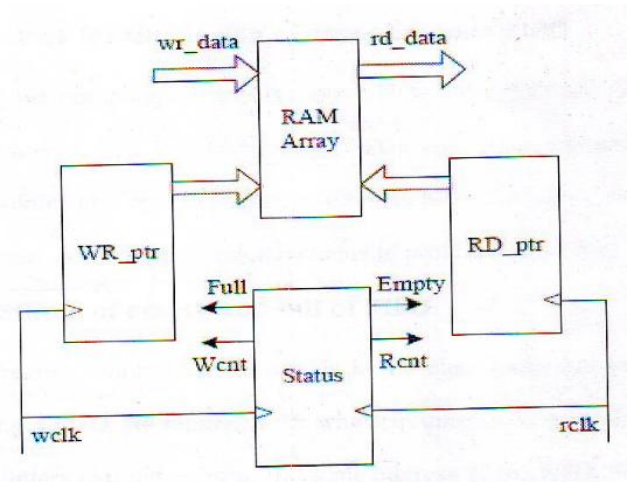

Figure 2 : Asynchronous FIFO

A RAM array with separate read and write ports is used to store data .The writer pointer points to the location that will be written next, and read pointer points to the location that will be read currently. A write operation increments the writer pointer and read operation increments the read pointer. On reset, both pointers are rest to zero, the FIFO is empty. The write pointer happens to be the next FIFO location to be written and read pointer is pointing to invalid data. The responsibility of status block is to generate the EMPTY and FULL signals to the FIFO [4]. If the FULL signal is active then the FIFO cannot accommodate more data and if the EMPTY is active then the FIFO cannot provide more data to read out. When writing data into the FIFO „wclk"will be used as the clock domain and when reading data out of the FIFO „rclk" will be used as the clock domain. These both clock domains are asynchronous.

c) Factors for the design of Asynchronous FIFO

In the designing of asynchronous FIFOs, two important factors are considered. One is how to judge FIFOs status according to the writer pointer and read pointer. The other is how to design circuit to synchronize asynchronous clock domains to avoid metastability.

d) Status of empty and full of FIFO

Creating empty and full signals is the most important part of designing a FIFO. No matter under what circumstance, the read and write pointers cannot point to the same address of the FIFO. So the empty and full signals play very important roles within FIFO that they block access to further read or write respectively. Generally, in an ordinary FIFO, when the read pointer equals the write pointer the FIFO is empty. But in a circular FIFO it is either empty or fll when both of the pointers are equal. Because the FULL and EMPTY signals can not only be decided by the pointers value but also influenced by the operation that caused the pointers to become equal. If a reset or read makes the pointers equal to each other, the FIFO is really empty. If a write makes the pointers equal, the FIFO is full.

One design technique used to distinguish between FULL and EMPTY is to add an extra bit to each pointer. When the write pointer increments past the final FIFO address, the write pointer will increment the unused MSB while setting the rest of the bits back to zero as shown In below figure(the FIFO has wrapped and toggled the pointer MSB).The same is done with the read pointer. If the MSBs of the two pointers are different, it means that the write pointer has wrapped one more time that the read pointer. If the MSBs of the two pointers are the same, it means that both pointers have wrapped the same number of times.

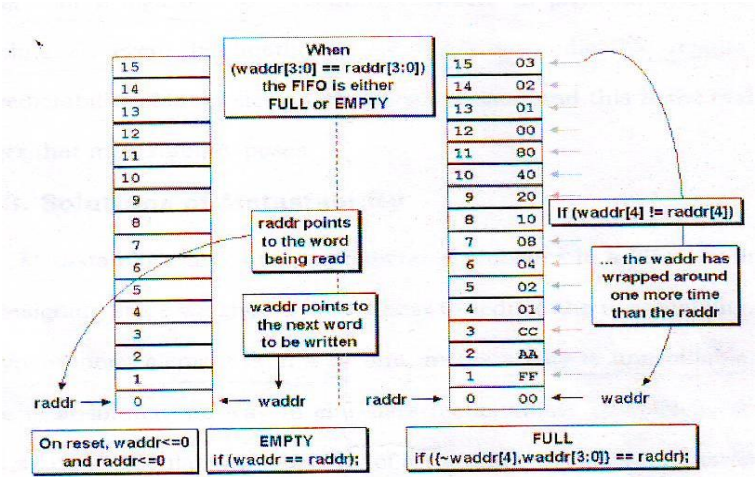

Figure 3 : FIFO organization

Using n-bit pointers where (n-1) is the number of address bits required to access the entire FIFO memory buffer. As shown in above figure the FIFO is empty when both pointers, including the MSBs are equal. And the FIFO is full when both pointers. Except the MSBs are equal. The FIFO design described here uses n-bit pointers for a FIFO with 2(n-1) write-able locations to hep handle FULL and EMPTY conditions.

e) UART circuit block and structure

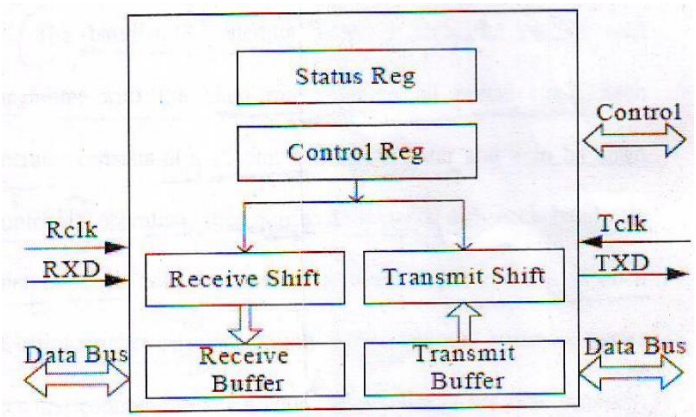

Figure 4 : UART Block diagram

f) Software structure

We can use software codes in VHDL to design FPGAs hardware structure, it is easy to create and adjust to satisfy requirements of applications. There are one UART used to communicate with PC or other main MCU and there are also four other UARTs used to communication with sub MCUs [5]. Each channel has two FIFOs one for receiving data and the other for transmitting data. Each FIFO"s depth is 64 bytes. The software flow chart is shown in figure 6.

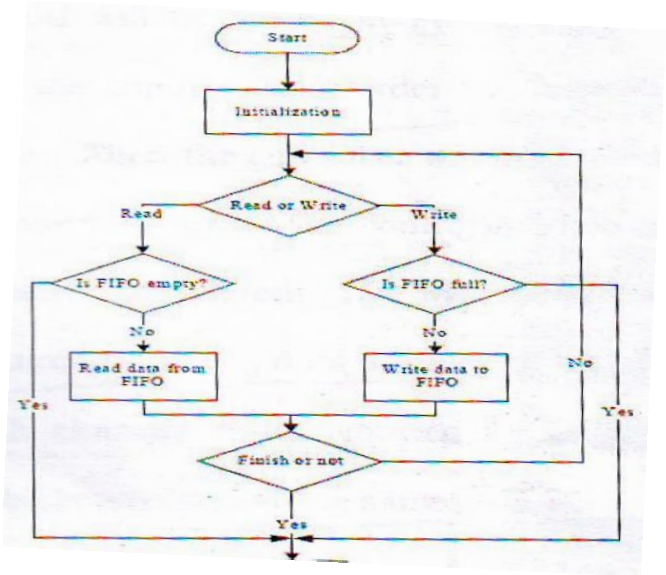

Figure 5 : Proposed method Flow Chart

As shown in figure ,when FIFO is full we cannot write any more byte into the FIFO.At this time, the status detector will set CS high to indicate that the FIFO is full and when FIFO is full you cannot write any more byte into the FIFO. At this time, the status detector will set CS high to indicate that the FIFO is full and stop writing to the FIFO. When FIFO is empty we cannot read from it any more. Then the status detector will set empty high to indicate the status of FIFO and stop reading from it [6][7].

When FIFO is not full or empty it will be written or read data according to the control order. After finishing all write or read operation it will stop until next access is coming.

III. Simulation Results

a) Simulation And Verification

To verify design of the controller a test bench is written to make verification in modelsim .Data received from the PC or other main MCU will be stored in FIFO"s within FPGA till the controller will set a kind of baud rate according to commands desired. The controller is receiving data and store the data received to different FIFO waiting for read. When sub-controllers are required to receive data at different baud rates, the controller can set each channel at its required baud rate to transmit data. The controller sends data at the same time but at different baud rate.

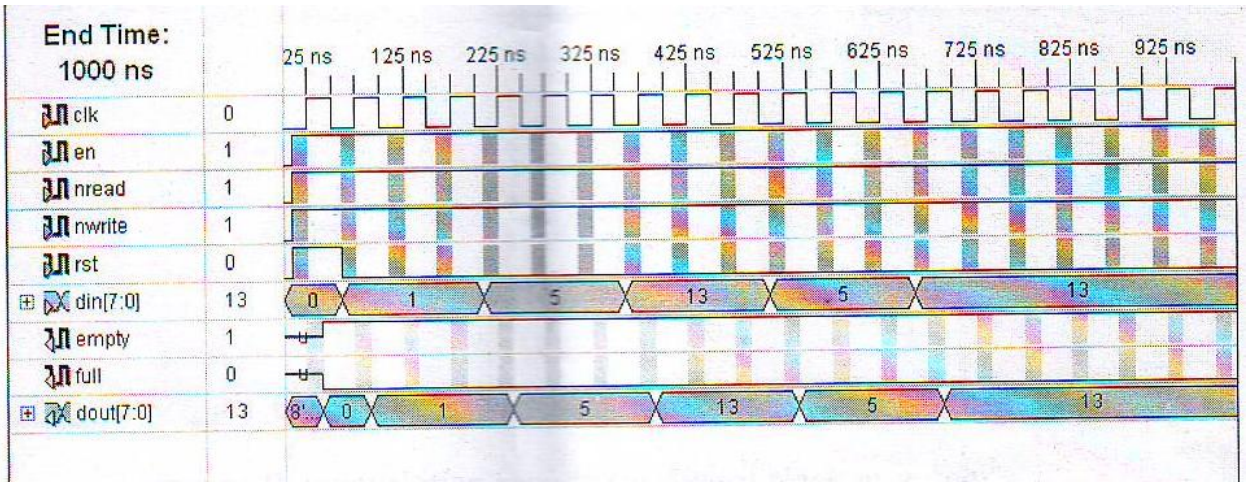

Figure 6 : Simulation results for single FIFO

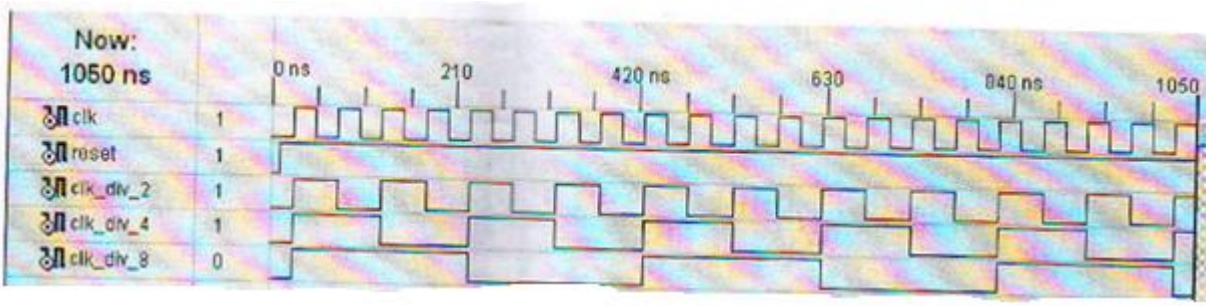

Figure 7 : Simulation results for digital clock manager

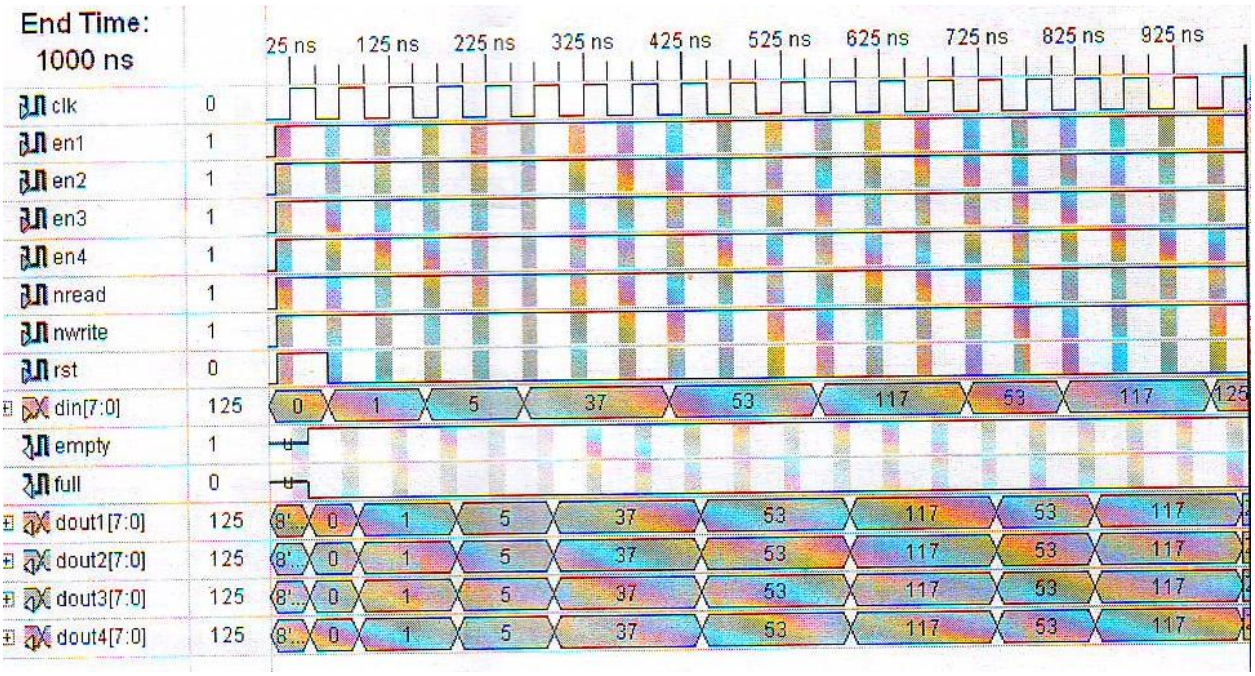

Figure 8 : Simulation results for same baud rates

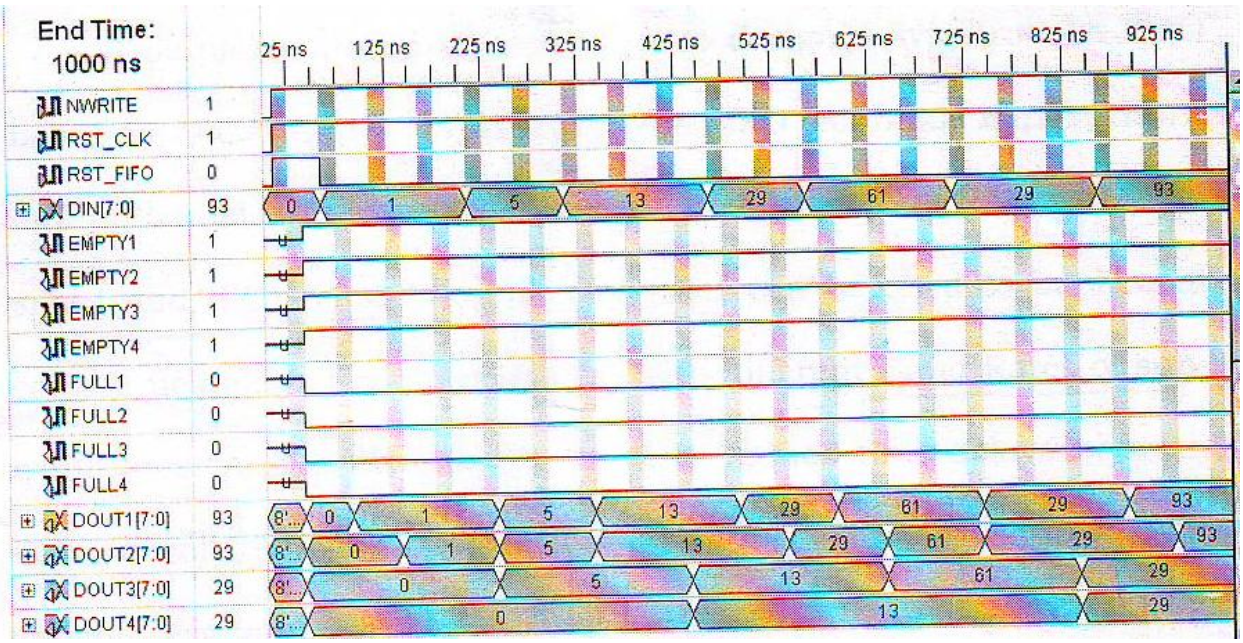

Figure 9 : Simulation results for different baud rates

IV. Conclusion

This paper introduces a method to design a method to design a asynchronous FIFO based on FPGA. And using asynchronous FIFO technique implements a multi channel UART controller within FPGA based on SRAM wit high speed and reliability .The controller can be used to implement communications in complex system with different baud rates of sub controllers. And it also can be used to reduce time delays between sub controllers of a complex control system to improve the synchronization of each sub controller. The controller is reconfigurable, so the controller"s fault is that it would be influenced by the radiation from surroundings and by short time pulses easily.

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Design and Implementation of General Purpose Remote Terminal Unit (R.T.U)

By Eng. Wael E. Matti & Dr. Jabir S. Aziz

Abstract - This paper introduce the design and development of multifunctional sensor nodes, the design based on microcontroller which represent the heart of any low cost R.T.U. A small size R.T.U can be used as a server provides the required data in the remote area. The proposed R.T.U is of low cost, low power, easy to implement and efficient to be used in different applications.

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Design and Implementation of General Purpose Remote Terminal Unit (R.T.U)

Eng. Wael E. Matti [α] & Dr.Jabir S. Aziz [σ]

Abstract - This paper introduce the design and development of multifunctional sensor nodes, the design based on microcontroller which represent the heart of any low cost R.T.U. A small size R.T.U can be used as a server provides the required data in the remote area. The proposed R.T.U is of low cost, low power, easy to implement and efficient to be used in different applications.

I. Introduction

Telemetry is the science of gathering information at some remote location and transmitting the data to a convenient location to be examined and recorded, when telemetry is used both to monitor and control, the term supervisory control and data acquisition (SCADA) is often used to describe the system.[1]

Telemetry system consists of three parts, which are: central unit, RTU and communication media.[2]

A remote terminal unit (R.T.U) is a microprocessor-controlled electronic device that interfaces objects in the physical world to a central unit or SCADA by transmitting the required data to the system and sometimes by using messages from the central unit to control connected objects.[2]

The remote terminal unit consists mainly from three major parts (sensors, microprocessor or controller, Communications parts), Each R.T.U composed from the sensors that provide the required data for a certain application, the microcontroller which is the most important part of the R.T.U that collect the data from the sensors, process it and give it to the communication part for delivering it to the central unit.[2]

Microcontrollers are devices also known as computer in a chip, the design in cooperates all of the features found in a microprocessor (CPU, ALU,PC,SP and all registers) it has also other added features need it to be a complete computer : Rom, RAM, serial and parallel I/O, counters and a clock circuit. The prime use of the microcontroller is to control the operation of the R.T.U using a fixed program which is stored in ROM.[3]

The microcontroller is an embedded system which is used by individuals, who are, in the main, unaware that the system is a computer–based. The microcontroller is not flexible, it does not have an operating system; it's programmed to perform the required task.[4]

The microcontroller inside the R.T.U itself can not send data over any transmition media unless it is interfaced with parts or IC's capable of doing that [1].

To make the proposed R.T.U send data over computer networks, the controller inside the R.T.U need to have a TCP/IP protocol in the code memory making it an Ethernet node, well the controller also needs special parts that allow us to reach this media.[5]

Ethernet is the technology for LANs, Standardized in IEEE 802.3. In the OSI reference system, Ethernet is at the Data Link layer. used to connect computers in home and offices. It is also possible to interconnect networks by router and Gateways end with WANs.[6]

TCP/IP is a suite of protocols used in the internet to allow communication between computers, it is a layered protocol based on the open system interconnection OSI model, The term TCP/IP refers to communications that use TCP and IP protocols.[5]

II. Hardware Design of the Proposed System

a) *The Hardware Design of the R.T.U.*

The propose hardware design of the R.T.U is shown in figure (1)

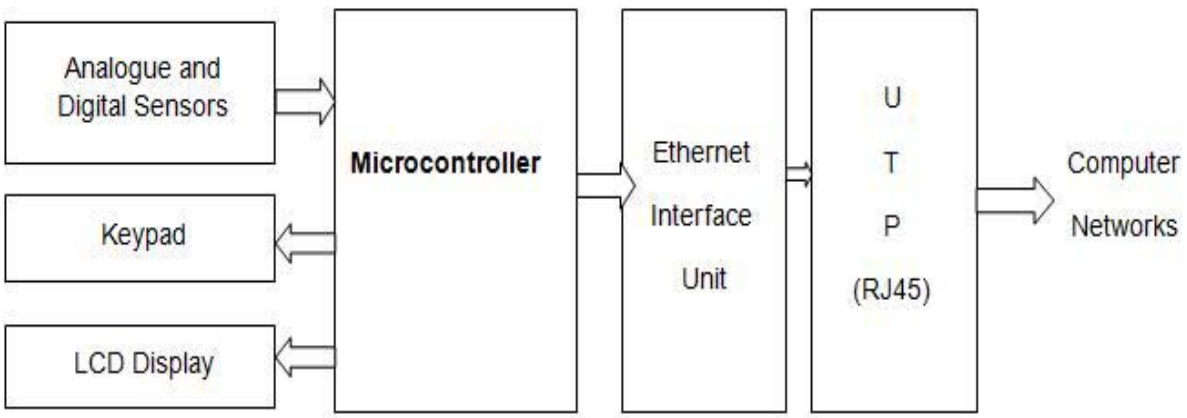


Figure 1 : The block diagram of the proposed R.T.U

The proposed R.T.U was implemented by using the following electronic components

- PIC16F887 Microcontroller.
- LM35 and DS18s20 as a temperature sensors.
- ENC28J60 as the Ethernet controller.
- Keypad and LCD

The PIC16F887 microcontroller has an 35-I/O pins, 14-I/O pin can be programmed to be either analogue or digital inputs, the other I/O pins can interface digital inputs. [7]

The first step of implementing the proposed design of Ethernet system is to interface the microcontroller (PIC16F887) with sensors, accessory part and the Ethernet controller 28J60. These interfaces include the hardware connections and programs reside in the mind of the microcontroller, the details can be summarized by the following sections

i. *data collection part*

The data collection section is performed by interface the PIC16F887 with sensors. The sensors identify which data is to be collected such as temperature, pressure, humidity, force and etc. LM35 and DS18s20 were selected as examples of analogue and digital sensors respectively.

The LM35DZ is an analogue sensor that is used for reading temperature range from -55 ^{o} to + 150 ^{o}. The PIC16F887 microcontroller has a built in Analogue-to-digital (ADC), so that the sensor's analogue signal can be connected directly to the analog input of the microcontroller.

DS18S20 is an example of digital sensors that read temperature provides 9-bit centigrade temperature measurement range from -55^{o} to +125^{o}.

In the implemented R.T.U two LM35 and two DS18S20 were connected to the PIC 16F887.

ii. *Accessory Part*

Adding a keypad and LCD display to the proposed R.T.U give to it aesthetic, not only this, in some applications the user want to interact with the R.T.U such as give it a new IP address or see some results, in the designed and implemented Ethernet R.T.U keypad and LCD display were added for security assigning a password to R.T.U.

iii. *Ethernet module part*

The PIC16F887 microcontroller can be connected to the computer network media via an Ethernet controller unit.

Microchip ENC28J60 is a stand- alone Ethernet controller with SPI (Serial peripheral interface). The ENC 28J60 meets all of the IEEE 802.3 specification, support one 10BASE-T port full duplex mode. ENC28j60 was used in the implementation of the proposed R.T.U.

b) The Hardware Design of the Central Unit

The main function of the central unit is to receive, process, store and display the data received from the R.T.U.

The implemented hardware consists of PC with NIC (network interface card) and IP address 192.168.1.67.

III. The Software Design

a) The Software Design of R.T.U.

The general flow chart of the implemented program is shown in figure (2), complex functions were given in subroutines. These routines easily give a good understanding of the main program. This program was implemented to reside in the ROM of the PIC16F887 which perform the operation of data collection from sensors and transmitting these data to the central unit via the communication media.

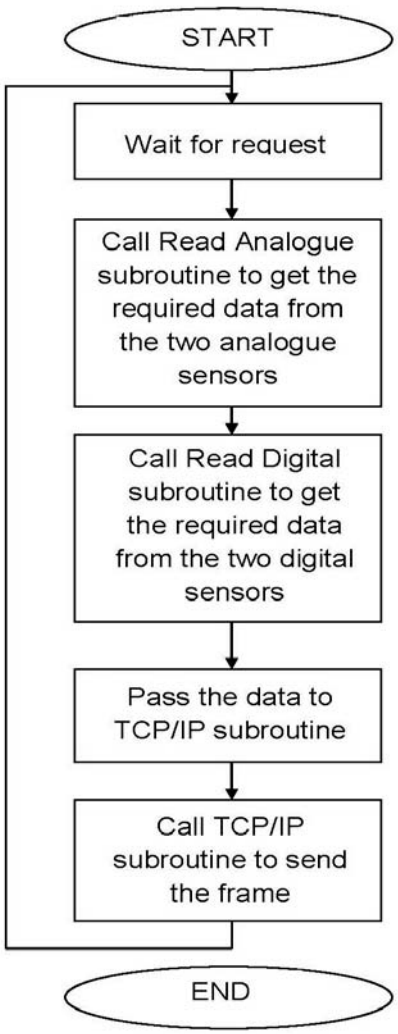


Figure 2 : The implemented program in the mind of R.T.U

There is no end stage in this flow chart because the R.T.U will always waiting for any request from the central unit.

With interfacing (hardware and software) with Ethernet controller the PIC now has NIC (network

interface card), the Ethernet system was become a R.T.U which is capable of sending the collected data.

The designed and implemented Ethernet R.T.U has the following features:-

a. Port Address 80:- the port address operates in transport layer guaranty the delivery of the data to the collect application in the PC. Port 80 is a HTTP (hypertext transfer protocol) function as a request-respond protocol in the client server model.

b. IP Address 192.168.1.60:- the IP address operate in the network layer guaranty the delivery of the packet to the correct device in the wide area network, each device on the computer network must have a unique IP address.

c. MAC Address 00.14.A5.67.19.3F h: - the MAC address operates in data link layer guaranty delivery of the frame to the correct device in local area network. Each device in the LAN has a unique MAC address.

d. The Speed of R.T.U:- is 10Mbs which is a good data transfer rate, this good data rate allow the R.T.U to transfer images and videos.

b) Software Design of Central Unit

The software was designed and implemented in visual basic program as shown in figure (3).

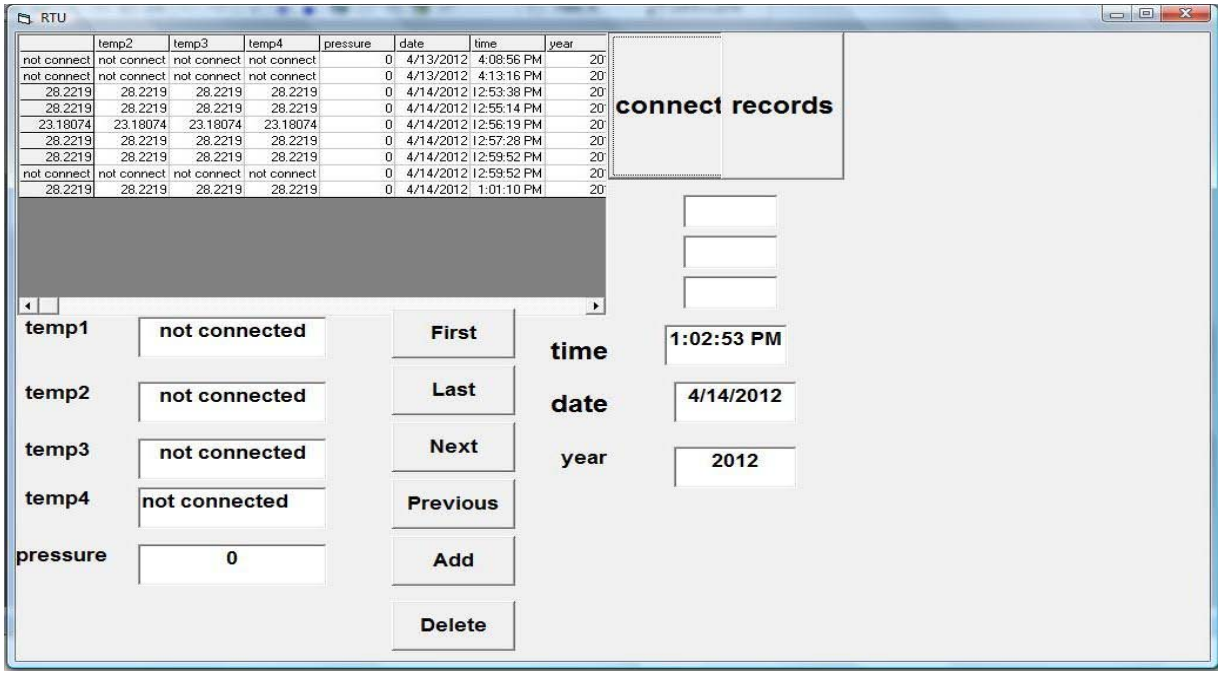


Figure 3 : The designed and implemented central unit program

Programming in visual basic is a combination of visually arranging components or controls on a form and writing additional lines of code for the functionality. The Winsock control can be used for TCP communications, properly must be set for TCP protocol, the IP address and port number of the target device are stored in the' Remote Host' and 'Remote Port' properties, these properties can be set either on design time or run time.

The flow chart of the implemented central unit program is shown in figure (4).

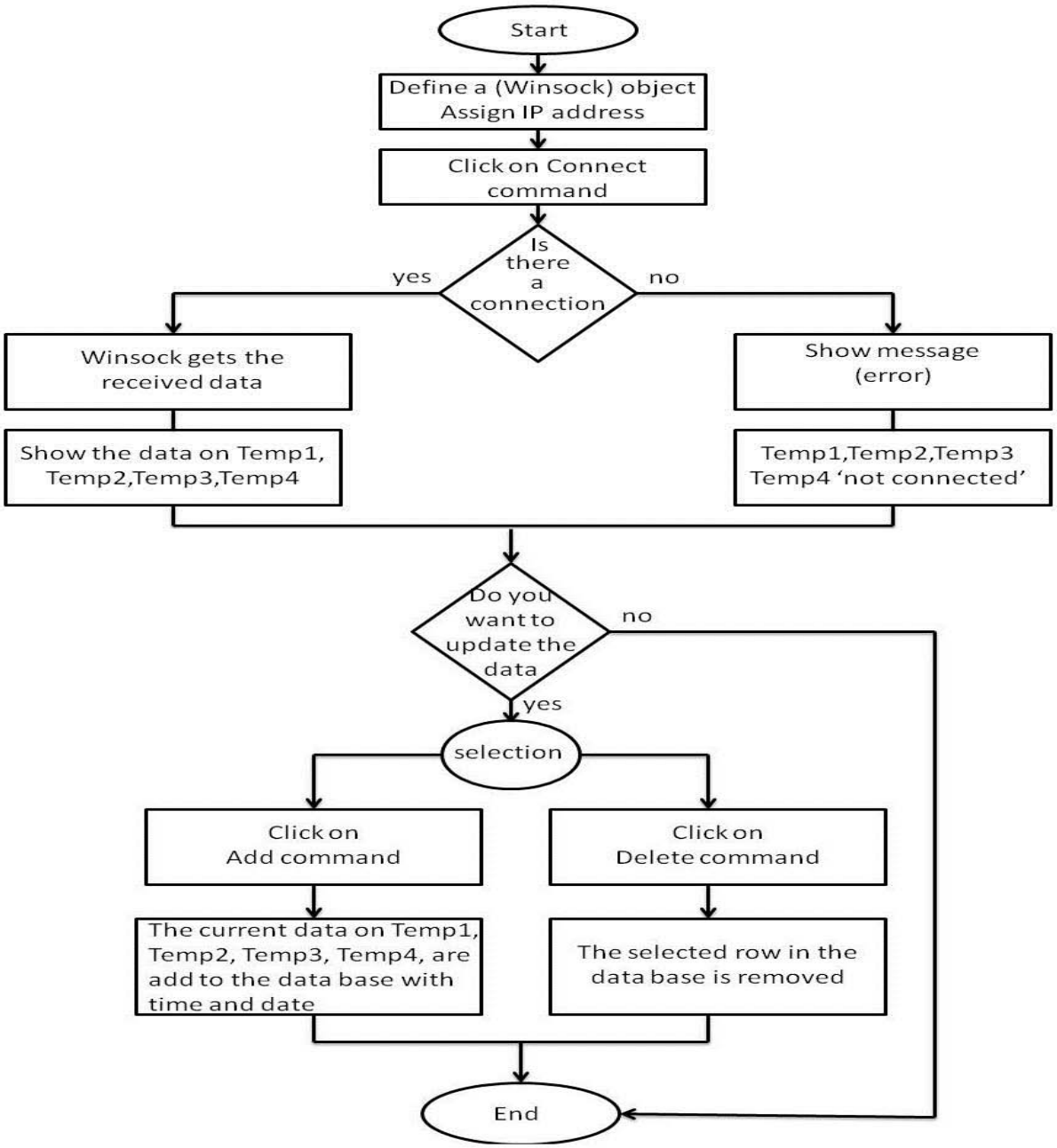


Figure 4 : Flow chart of the central unit program

IV. Result and Discussion

The Ethernet R.T.U was designed and implemented successfully as shown in figure (5). The technical specifications for the R.T.U are:

- Supplied voltage: - 5volt.
- Operating frequency: - 5Mhz.
- Output current: - 100mA.
- Bit rate: - 10Mbs.
- Number of input: - 2 analogue signal, 2 digital signal.

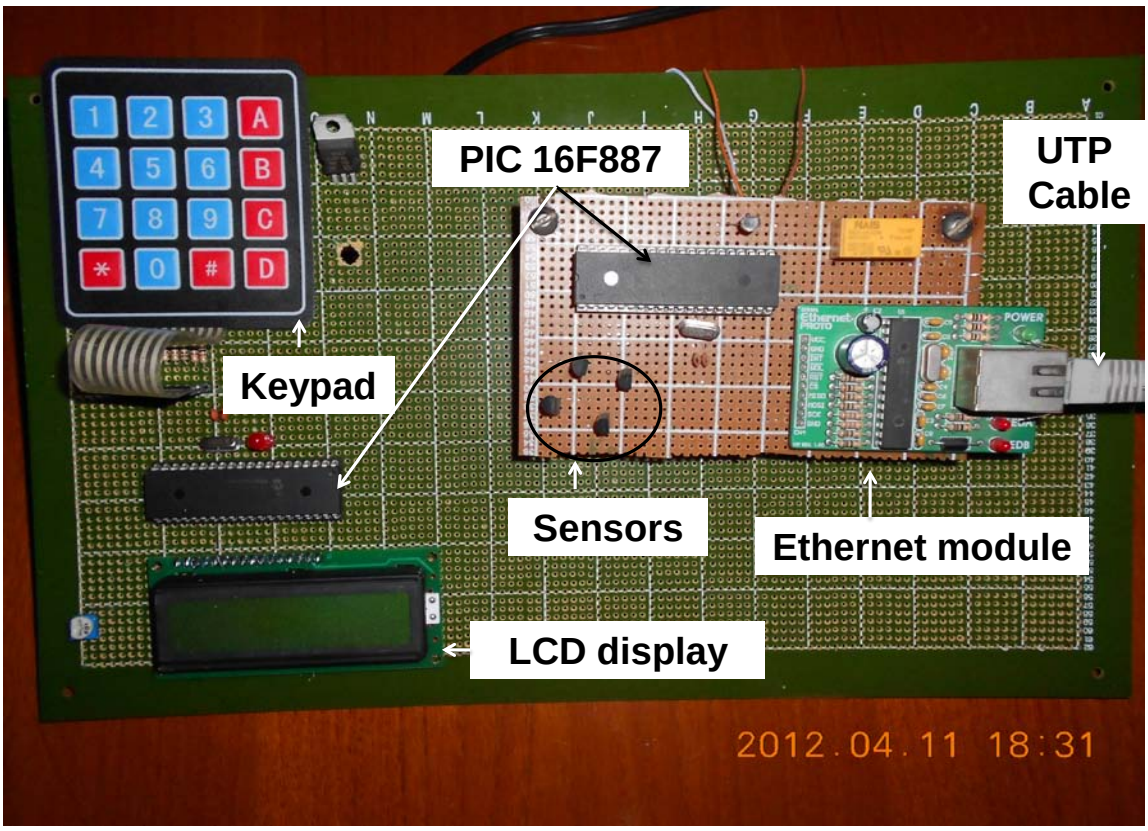


Figure 5 : The implemented Ethernet R.T.U

Figure (6) shows a connection between R.T.U and central unit over a WAN . A router was added to allow access to WAN and internet networks.

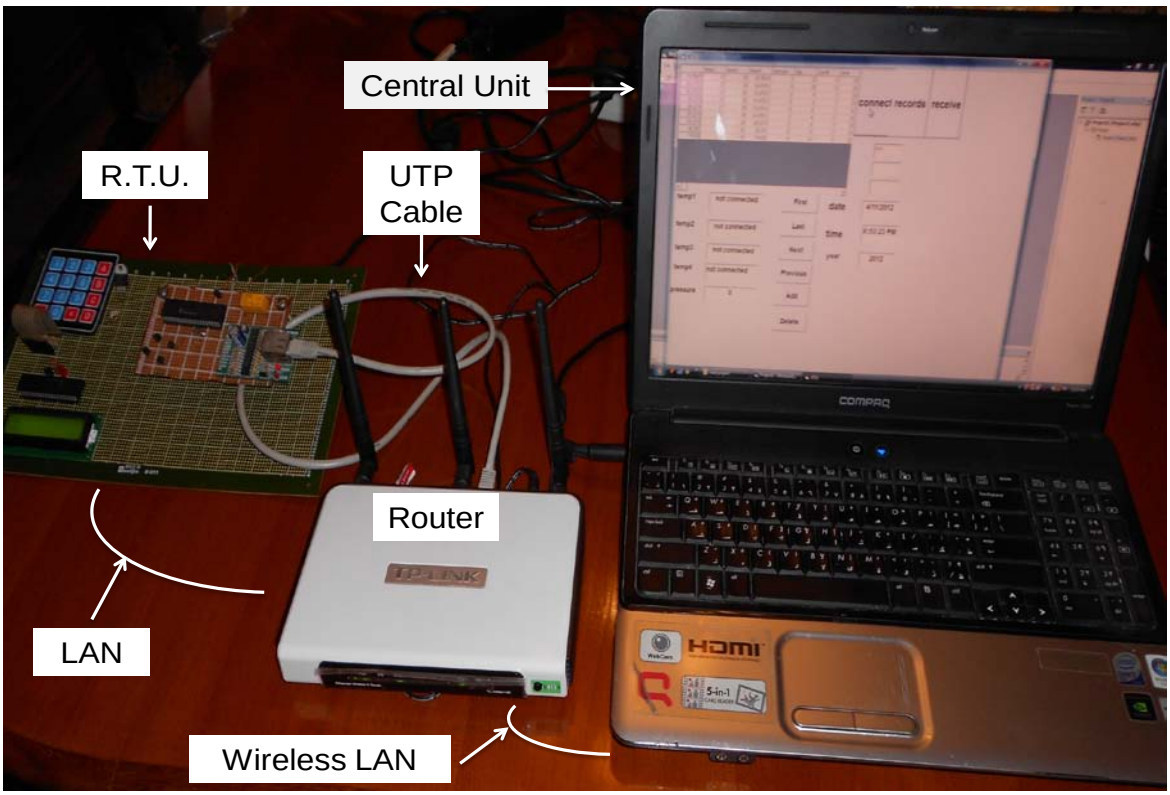


Figure 6 : The implemented telemetry system over WAN

When the R.T.U is switched ON the LCD display shows a "Enter the password "message. The password should be entered by the user correctly. Then LCD shows a "OK" message and activate the other part of the R.T.U.

When the implemented R.T.U is connected to central unit, clicking on the connect command field will start a connection and request the implemented R.T.U to send its data to central unit, the R.T.U collects the data from the sensors process it and send it to central unit.

In the central unit the data has been received from R.T.U is displayed in Temp 1, Temp 2, Temp 3 and Temp 4 fields as shown in figure (7).

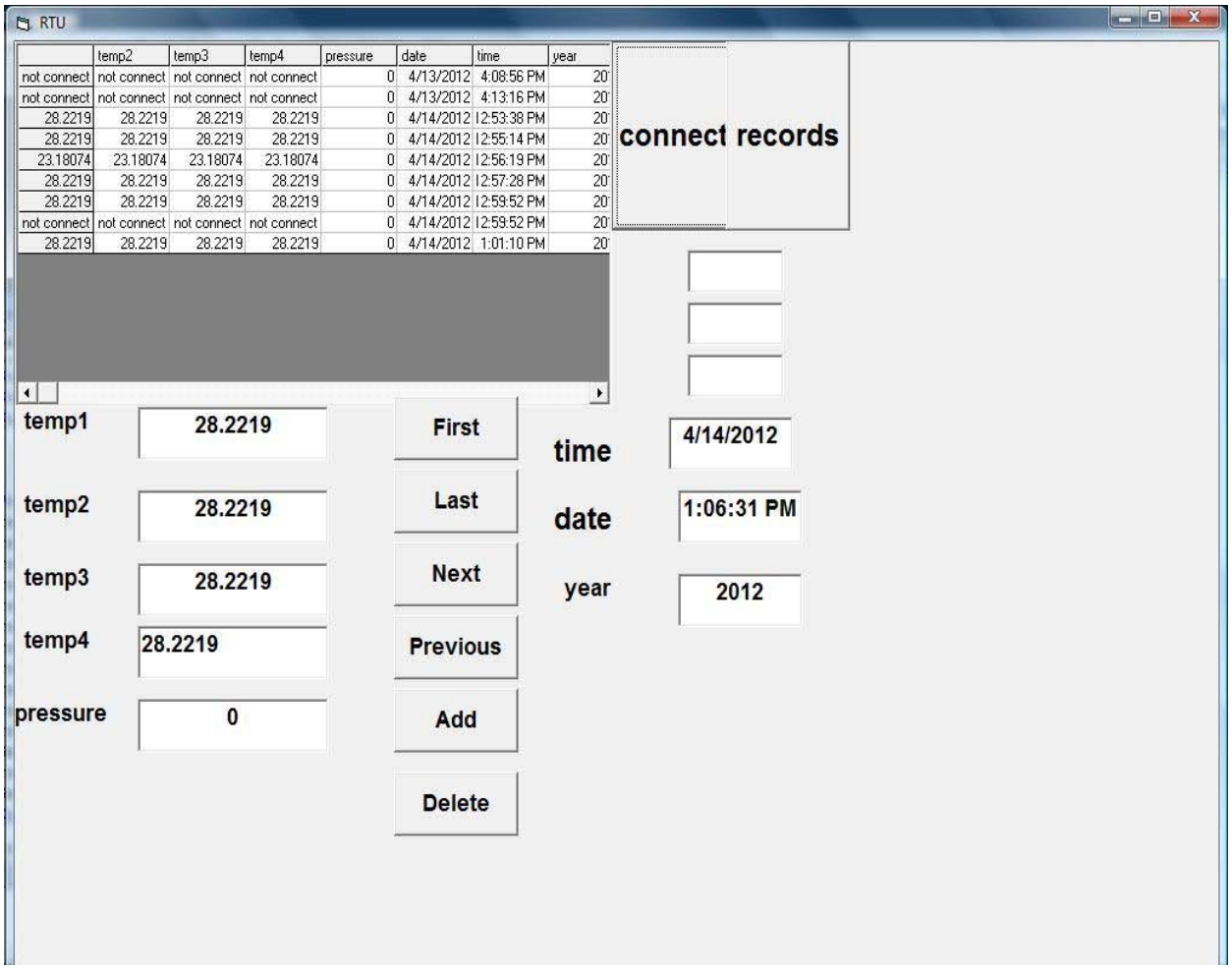
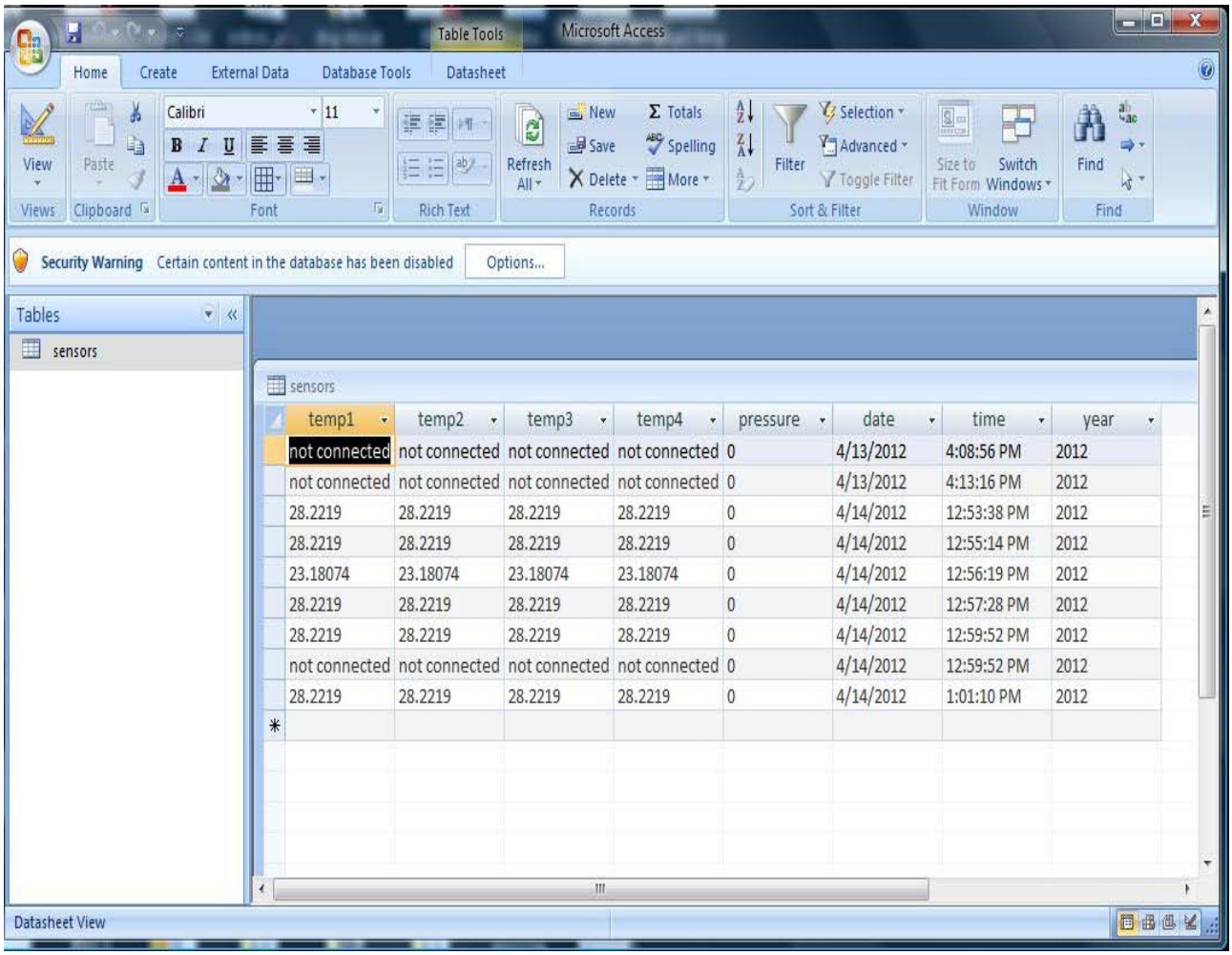


Figure 7 : The central unit program shows the data received

A data base and access files were constructed which modify and update by the implemented central unit program, the access sheet is shown in figure (8).

The data base and the access sheet store the received data at the exact time and date on which the data was collected.

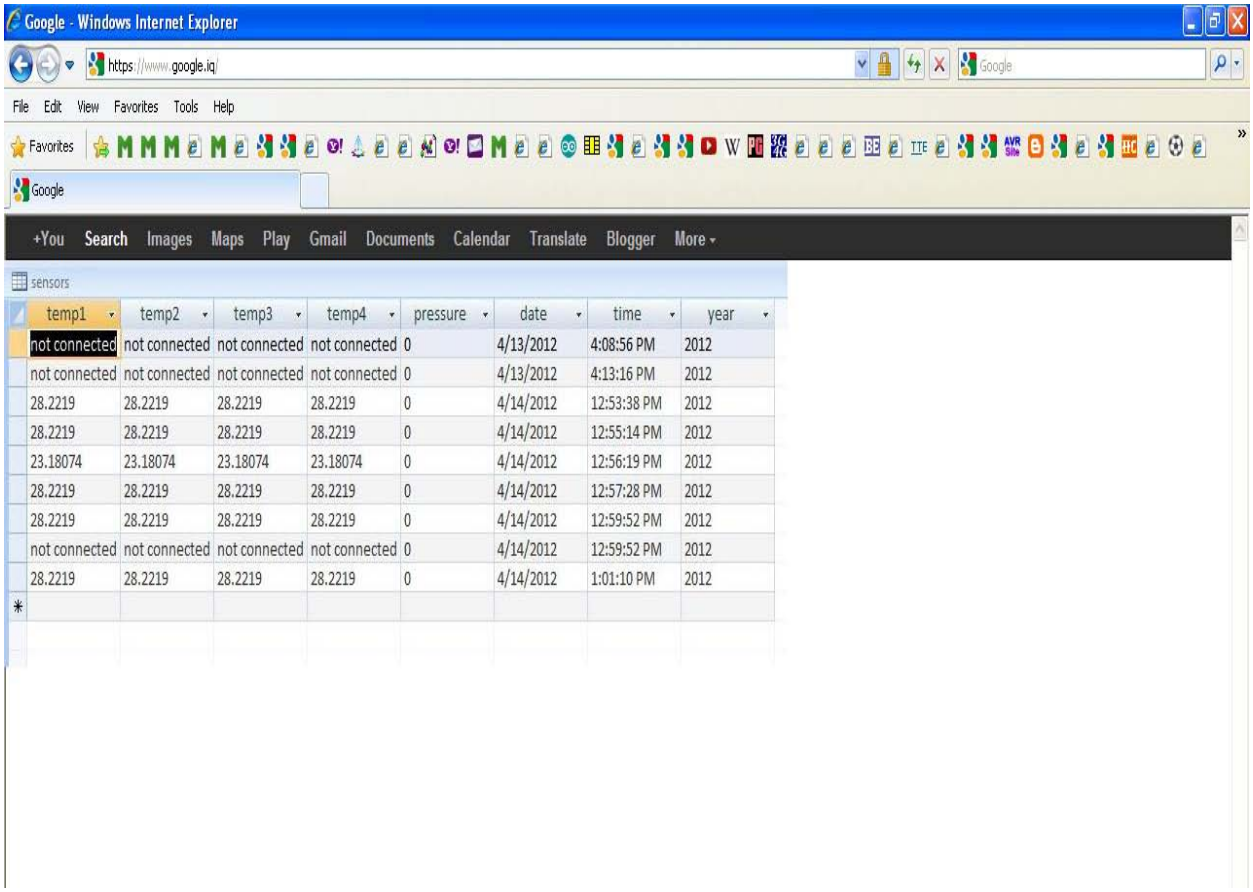
The benefit of having a data base is to provide reliable persistent storage and the ease of extract data to obtain reports.



temp1	temp2	temp3	temp4	pressure	date	time	year
not connected	not connected	not connected	not connected	0	4/13/2012	4:08:56 PM	2012
not connected	not connected	not connected	not connected	0	4/13/2012	4:13:16 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	12:53:38 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	12:55:14 PM	2012
23.18074	23.18074	23.18074	23.18074	0	4/14/2012	12:56:19 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	12:57:28 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	12:59:52 PM	2012
not connected	not connected	not connected	not connected	0	4/14/2012	12:59:52 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	1:01:10 PM	2012

Figure 8 : Constructed access files

A web page was constructed in the central unit to show the received data in the internet pages as shown in figure (9).



temp1	temp2	temp3	temp4	pressure	date	time	year
not connected	not connected	not connected	not connected	0	4/13/2012	4:08:56 PM	2012
not connected	not connected	not connected	not connected	0	4/13/2012	4:13:16 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	12:53:38 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	12:55:14 PM	2012
23.18074	23.18074	23.18074	23.18074	0	4/14/2012	12:56:19 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	12:57:28 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	12:59:52 PM	2012
not connected	not connected	not connected	not connected	0	4/14/2012	12:59:52 PM	2012
28.2219	28.2219	28.2219	28.2219	0	4/14/2012	1:01:10 PM	2012

Figure 9 : The constructed web page

V. Conclusions

In this paper a telemetry system was designed and implemented. The remote terminal unit which was designed and implemented has the following features:

- Low cost and small size RTU unit.
- PIC16F887 microcontroller gives the proposed system the ability to be used in different applications.
- The use of Ethernet facilitates the communication mechanism allowing the proposed system to run over any computer network infrastructure.
- The designed software in the central unit allow data to be stored in a database which provide reliable persistent storage. This allow The ease of extract data and obtain reports and the ease of data management to some level of quality.
- The use of Internet Browser allows the data to be shared in many locations that have access to the designed web page.
- The use of TCP ensured the delivery of packets on the contrary of the use of UDP which is unreliable.

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New Techniques for Hardware Implementations of SHA

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Abstract - Secure Hash Algorithms are one of the forms of cryptographic algorithms. SHA hash functions are widely used security constructs. However, they are software implementations of SHA. This paper proposes techniques for hardware implementation of SHA. In order to provide security and improve performance, these methods are used in hardware reutilization and operation rescheduling. The purpose of implementing SHA at hardware level is to improve throughput. The empirical results revealed that the throughput is increased by 29 to 59% in case of SHA-1 implementation. The throughput is further increased up to 100% when SHA-2 is implemented and used. Thus it is evident that hardwahre implementation of SHA has more speed when compared with software implementations of SHA.

Index Terms : *Secure Hash Algorithm (SHA), cryptography, hash functions, hardware implementation, FPGA, software implementation.*

GJRE-F Classification : *FOR Code: 100504,E.2*

Strictly as per the compliance and regulations of:

New Techniques for Hardware Implementations of SHA

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Abstract - Secure Hash Algorithms are one of the forms of cryptographic algorithms. SHA hash functions are widely used security constructs. However, they are software implementations of SHA. This paper proposes techniques for hardware implementation of SHA. In order to provide security and improve performance, these methods are used in hardware reutilization and operation rescheduling. The purpose of implementing SHA at hardware level is to improve throughput. The empirical results revealed that the throughput is increased by 29 to 59% in case of SHA-1 implementation. The throughput is further increased up to 100% when SHA-2 is implemented and used. Thus it is evident that hardwahre implementation of SHA has more speed when compared with software implementations of SHA.

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I. Introduction

Cryptography is the branch of computer science that deals with security. It supports operations such as encryption and decryption. The cryptography is implemented in the form of hash functions, symmetric key algorithms, and public key algorithms. The symmetric and public key algorithms are used for encryption and decryption while hash functions are one way functions as they don't allow the retrieval of processed data. As MD5 and SHA are the two mostly used algorithms in the industry, this paper focuses on secure hash algorithms. MD5 can avoid collision attacks [1] with computational feasibility while SHA -1 attacks also computationally expensive [2]. As SHA-1 is not fully secure, the SHA -2 was introduced [3]. At hardware level in order to improve the performance, GPPs (General Purpose Processors) are used. SHA improvement has been done [10], [11]. This paper introduces the implementation of SHA algorithm at hardware level using techniques described here. They are pipeline techniques [5], [18]; embedded memories used to store constant values [8]; improved addition and balanced delays [4], [12]; unrolling techniques [5], [9], [10], [12]; balanced carry save address and parallel counters [4], [5], [7].

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This paper proposes two architectures that can be used with hardware. This is meant for achieving high throughput. The results of implementation of SHA-1and SHA-2 algorithms at hardware level provide more speed when compared with software implementations.

II. Hash Functions

Since from its inception in 1993, the hash algorithms are improved further to have SHA, SHA-1 and SHA-2. The original SHA was revised in 1995 [15] and named as SHA-1 while SHA-2 WAS INTRODUCED IN 2001 which makes use of DM thus making it more robust to security attacks. SHA functions are available with 128, 256 and 512 bits. From the given input message SHA-1 can produce 160 bit message digest as output. Final DM of 256 bits is the output of SHA 256. The computation of SHA 512 is identical to that of SHA 256. The difference is in the size of operands that means it uses 64 bits instead of 32 bits. Moreover the DM of this algorithm has 512 bits the logical function used are also different [15]. Fig. 1 and Fig. 2 show the round calculations of SHA-1 and SHA-2. SHA-1 needs 80 rounds while SHA 256 uses 64 rounds.

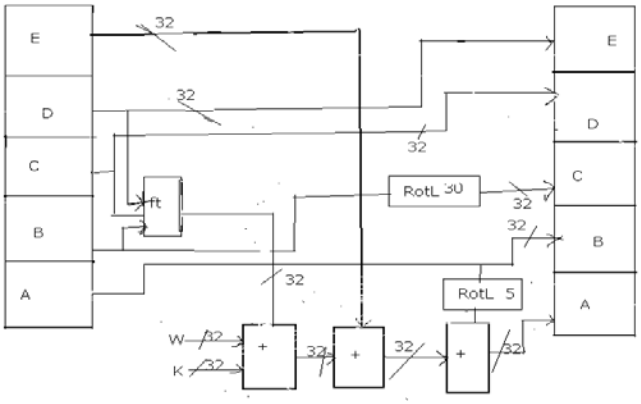

Fig. 1 : Shows round calculation of SHA-1

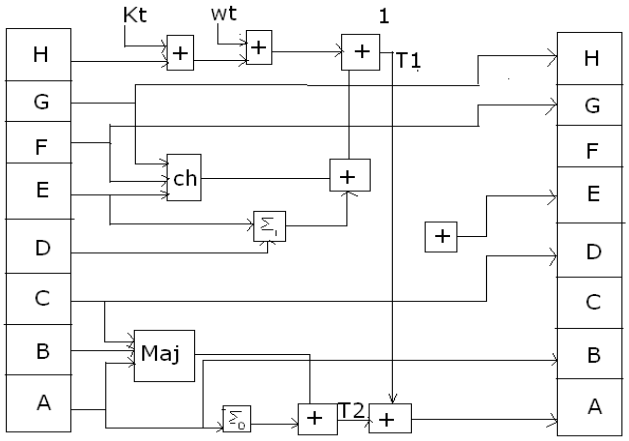

Fig. 2 : Shows round calculation of SHA-2

a) Design for SHA 1.

Each round of SHA-1 requires value from previous round. As rounds are data dependent, it is essential that rounds are carried out sequentially. By unrolling each round computations [10] attempts to speed it up. Another approach increases throughput as it makes use of pipelined structure [11]. As described in [13], high throughput is achieved in SHA-1. Operations rescheduling with respect to this paper has operations rescheduling, hash value initialization, and improved Hash Value Function. The whole computation of SHA-1 is in the A as the rest do not need any computation. The required values are provided by previous round values of various A to D. By adding zero to initialization vector, the internal hash value of first data block can be initialized. Later on this value is loaded into internal registers through multiplexer. In this case instead of the value to the register, it is set to zero as described in [6]. Improving hash value addition is done after all the rounds have been computed for a given data block. Here the internal variables are to be added to the current DM and it needs four additional adders. Finally SHA-1 data block expansion is described here. 512 bits of each data block is expanded in hardware for efficiency reasons as described in [1]. It can be implemented using XOR operations and also registers. Final output is original data for first 16 rounds and computed values for the rest of rounds.

b) Design for SHA 2.

As done in SHA-1, the functional rescheduling can also be applied to SHA-2 as well. However, its computational complexity of it is more. In each round values are calculated as and when required. As described in [19], the part that has to be computed is identified. With respect to operational rescheduling values for B, C, D, F, G and H are obtained directly. However, A and E values can't be computed until they are computed in the previous round. With respect to hash value addition and initialization, similar to SHA-1, the internal variables of SHA-2 also have to be added to the DM. It needs eight adders. For each SHA 256 and SHA 512 of 32 bits and 64 bits respectively an adder is required. The empirical results reveal that DM addition with a shift is more efficient. With respect to SHA-2 data block expansion done by data block expansion unit, it is similar to SHA128 in terms of computations. The XOR operation is replaced by arithmetic addition.

III. Implementation

The SHA designs described above has been implemented as processor cores on a Xilinx VIRTEX II Pro FPGA. The FPGA embedded RAMs (BRAMs) are used in order to implement ROM used to store SHA256 and SHA512. Register – based structures can also be used alternatively. One is based on circular fashion in which memory blocks addressed while the other one is based on FIFOs (First – inputs –first – outputs).

IV. Performance Analysis and Related Work

The resulting cores have been implemented in different Xilinx devices in order to compare the architectural gains of the proposed SHA structures. SHA -1 core, SHA 256 core and SHA 512 core performance comparisons are provided in tables I, II and III respectively.

Design	Lien[11]	Lien[11]	Our-Exp.	CAST[20]	Helion[21]	Our-Cst.	Our+IV
Device	Virtex-E	Virtex-E	Virtex-E	XCV2P2-7	XCV2P-7	XCV2P30-7	XCV2P30-7
Expansion	no	no	no	yes	yes	yes	yes
IV	Cst.	Cst.	Cst.	Cst.	Cst.	Cst.	yes
Slices	484	1484	388	568	564	533	565
Freq.(MHz)	103	73	135	127	194	230	227
TrPut.(Mbps)	659	1160	840	802	1211	1435	1420
TP/Slice	1.4	0.8	2.2	1.4	2.1	2.7	2.5

Table 1 : Shows SHA-1 Core performance comparisons

Architecture	Sklav[22]	Our	McEv.[13]	Our	Helion[23]	Our
Device	XCV	XCV	XC2V	XC2V	XC2PV-7	XC2PV-7
IV	Cst	Yes	Cst	Yes	Cst	Yes
Slice	1060	764	1373	797	815	755
BRAMS	>=1	1	>=1	1	1	1
Freq.	83	82	133	150	126	174
Cycles	n.a.	65	68	65	n.a.	65
Throughput	326	646	1009	1184	977	1370
TP/Slice	0.31	0.84	0.74	1.49	1.2	1.83

Table 2 : Shows SHA256 Core performance comparisons

Architecture	Sklav[22]	Lien[11]	Lien[11]	Our	McEv.[13]	Our	Our
Device	XCV	XCV	XCV	XCV	XC2V	XC2V	XC2VP
Expension	Yes	no	no	Yes	Yes	Yes	yes
IV	Cst	Cst	Cst	Yes	Cst	Yes	Yes
Slice	2237	2384	3521	1680	2726	1666	1667
BRAMS	n.a.	n.a.	n.a.	2	>=1	1	1
Freq.	75	56	67	70	109	121	141
Cycles	n.a.	n.a.	n.a.	81	84	81	81
Throughput	480	717	929	889	1329	1534	1780
TP/Slice	0.21	0.3	0.26	0.53	0.49	0.92	1.01

Table 3 : Shows SHA512 Core performance comparisons

V. Integration with Processor

SHA algorithms that have been implemented are integrated with a processor known as MOLEN polymorphic processor and its operation [14], [16] is based on the coprocessor architectureal paradigm which allows SHA cores to be embedded in a reconfigurable coprocessor with the GPP. This implementation is similar to the one given in [17]. When compared with software implementations, it is capable of achieving throughputs such as 5 Mbit/s and 4 Mbit/s for SHA 256 and SHA 128 respectively and overall speed is increased by 150 times.

VI. Conclusion

We have implemented SHA-1 and SHA-2 algorithms at hardware level. This achieves the reutilization and rescheduling of hardware in terms of area and speed. Critical path can be reduced with the help of operation rescheduling. It leads to the very good usage of pipeline structure. The SHA-2 which makes use of DM causes the reduction of reconfigurable resources. This also hides the extra clock cycle delay. The results of implementation reveals that the hard ware implementation of the hash algorithms are many times better than the software implementations of the same.

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Power Profiling and Analysis of MI-Benchmarks Using Xscale Power Simulator (XEEMU)

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Abstract - It is often required to compute the power consumed by an application to avoid later surprises of low battery life, or high temperature a device reaches while running the application; potentially damaging the device. There are three ways to find power consumed by a system for executing a particular application. 1) Run application on a reference board and measure the power dissipated. 2) Simulate the power consumed by the target system by running standard applications on it, but simulations can be time consuming. 3) Use heuristic formulas based on pre-analyzed simulation data. In this paper we come with some empirical formulas to calculate the power of a particular application, So that we do not need to run extensive simulations.

Keywords : *VLSI, Xscale, XEEMU.*

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Nishant Kumar [α] & Rahul Johari [σ]

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Keywords : *VLSI, Xscale, XEEMU.*

I. Introduction

Power consumed by a particular application running on a device defines:

1) Battery life of the device
2) Maximum temperature device can reach while running the application

Power dissipated in embedded systems can be reduced with multiple hardware optimization techniques, such as transistor resizing, low-voltage design techniques and frequency control methods. There is a considerable amount of work done in hardware power optimization; however these techniques are only applied in early design steps such as VLSI design and synthesis. Embedded software transformations are another way to reduce power consumption, since software is responsible for driving the circuits and components of the system. In terms of software optimization techniques, power dissipation can be reduced with compiler, instruction-level, and source code-level optimization methods. Most of the work done to reduce power consumption has been oriented to compiler optimization where several techniques have been created and incorporated into compilers. Source code and instruction-level optimizations are an alternative in low power consumption analysis. Although instruction-level optimizations give excellent results with respect to low power consumption, source code optimizations have advantages in terms of portability, readability, and maintenance. Some studies done in embedded software optimization have shown that source code optimization techniques tend to diminish power consumption.

II. Instruction Level Power Analysis

The increasing popularity of power constrained mobile computers and embedded computing applications drives the need for analyzing and optimizing power in all components of a system. Software constitutes a major component of systems where power is a constraint. In light of this, there is a clear need for considering the power consumption in systems from the point of view of software. Software impacts the system power consumption at various levels of the design. However, in order to systematically analyze and quantify this impact, it is important to start at the most fundamental level – the instruction level. Just as logic gates are the fundamental units of computation in digital hardware circuits, instructions can be thought of as the fundamental unit of software. Accurate modelling and analysis at this level is the essential capability needed to quantify the power costs of higher abstractions of software. Traditional power analysis tools are not suited for power analysis of software. Accurate tools exist only for the lower most levels of the design, but they can be slow and cumbersome to use, and often these cannot even be applied, since the lower level information is not available to the software or embedded system designer. These problems can be overcome if the current being drawn by the CPU during the execution of a program is physically measured. An instruction level power analysis technique based on this idea has recently been developed. This technique helps in formulating instruction level power models that provide the fundamental information needed to evaluate the power cost of entire programs.

The average power, ***P,*** consumed by a microprocessor while running a program is given by:

$$P = I \times VCC, \quad (1)$$

Where, ***I*** is the average current and *Vcc* is the supply voltage.

The energy, E, consumed by a program is further given by:

$$E = P \times N \times r, \quad (2)$$

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Where, N is the number of clock cycles taken by the program and T is the clock period.

Thus, the ability to measure the current drawn by the CPU during the execution of the program is essential for measuring its power/energy cost.

A simple and practical technique has been developed to measure this current. The power supply connections to the CPU are isolated from the rest of the system. The program under consideration is put in an infinite loop and executed on the CPU. The current waveform will now be periodic and an average value can be visually obtained from a standard off the shelf digital ammeter. [3]

III. MI-Benchmarks

A benchmark is a program used as reference to make comparisons about the performance of a system. Benchmarks represent real applications which are run on computing systems. Although the concept of benchmarking is widely used in the area of computing systems performance, it can also be used when measuring other metrics such as power consumption. A benchmark has three important features:

1. Benchmark programs are easy to use.
2. Small size.
3. May run on different platforms.

These benchmarks were divided in six groups that represent embedded systems market:

- Automotive
- Consumers
- Office
- Networking
- Security
- Telecommunications [5]

IV. Selected Benchmarks

For the purposes of this work, a subgroup of the benchmarks explained before was chosen. The benchmarks used in this study are shown in table

Table 1 : Selected from Mi-Benchmarks for the study of Power Consumption

BENCHMARK	GROUP
Jpegtran	Consumer
Basicmath1	Automotive
Basicmath3	Automotive
Basicmath4	Automotive
QSORT	Automotive
String search	office
Susan	Automotive

V. Simulation Tool Used

We have used XEEMU (Xscale power simulator) to find the power consumed by a software program. XEEMU is a fast, cycle-accurate simulator for the XScale architecture. In contrast to many other existing power simulators, which simulate power and performance of theoretical microprocessor architectures, XEEMU aims at the most accurate modelling of the XScale architecture possible, trading off flexibility for much more reliable results. XEEMU proves to be more accurate than the other power simulators in terms of runtime and energy estimation, due to its improved pipeline and power model and the cycle accurate simulation of the SDRAM subsystem. It offers a high flexibility through freely and independently configurable frequencies for the core clock and the memory. [6]

VI. Methodology

Let the total energy consumed by a program is E, energy consumed by a particular type of instruction is I_j, and N_j is the number of times the instruction consuming I_j energy is executed in the program. We can write following formula:

$$\sum I_j * N_j = E \qquad (3)$$

To solve the problem, we will use:

1) A power simulator, to find the total energy consumed (E) by a software program
2) An instruction trace generator to find
   a. Types of instructions executed (to derive the correct range of j)
   b. Total number of times, a particular type of instruction is executed (N_j)

We will run power simulator and instruction trace generator on standard programs to come up multiple equations; we can decide to run 6 programs to generate 6 equations in 1 variable). We will then solve the available equations and find power consumed by each instruction (I_j). Once we know the power consumed by instruction, I_j, we need not run time consuming simulation to find E. Instead, we can compute the approximate Energy consumed from the instruction trace. We took 6 Mi-benchmark programs and calculated the power of each.

VII. Analysis

In this analysis, we assume that all instructions consume equal amount of energy to execute. Since, we have 6 MI-Benchmarks; we have 6 equations in 1 variable.

Table 2 : Number of Instructions

Program	Number of instructions
Jpegtran	6129891
Basicmath1	515034
Basicmath3	327723
Basicmath4	29329196
QSORT	10878448
String search	11564494

Table 3 : Energy of programs from Simulator

Program	Energy
Jpegtran	0.0083
Basicmath1	0.0005
Basicmath3	0.0004
Basicmath4	0.0288
QSORT	0.0134
String search	0.0129

Table 4 : Test programs Data

Programs	Instructions	Energy
Susan	32308776	0.0340
Matrix add	10172676	0.0104
Matrix multiplication	12138715	0.0127

VIII. Experimental Results

We used GNU Octave to solve Over-determined case of Equations to get the following results.

ALL_INSTRS = [6129891; 515034; 327723; 29329196; 10878448; 11564494];

SIMULATED_ENERGY = [0.0083; 0.0005 ; 0.0004; 0.0288; 0.0134 ; 0.0129];

Energy_per_inst = ALL_INSTRS\SIMULATED_ENERGY = 1.0354e-009

test_program_total_instr1 =32308776;

SIMULATED_ENERGY1 = 0.0340;

empirical_energy1 = Energy_per_inst*test_program_total_instr1= 0.0335

test_program_total_instr2=10172676

SIMULATED_ENERGY2 =0.0104

empirical_energy2 = Energy_per_inst*test_program_total_instr2=0.010532

test_program_total_instr3=12138715

SIMULATED_ENERGY3= 0.0127

empirical_energy3 = Energy_per_inst*test_program_total_instr3=0.012568

IX. Error Calculation

%Error=[(Theoretical Value-Experimental Value)/Theoretical Value] * 100

1) **E1** = [(0.0340-0.0335)/ 0.0340] x 100

   E1= 1.4705

2) **E2** = [(0.0104-0.010532)/ 0.010532] x 100

   E2=-0.0132

3) **E3** = [(0.0127-0.012568)/ 0.0127] x 100

   E3 = 1.0393

X. Future Work

We will perform different analysis by dividing the instructions into multiple categories:

1) Memory instructions.
2) Non memory instructions.
3) ALU instructions.
4) Branch instructions.
5) Register Transfer instructions.

Now we will calculate the energy consumed by each type of instruction. We have multiple equations in 2,3,4,5 variables. By solving them we get the energy consumed by one instruction of each type. By this information we can calculate the energy of a particular program only by the knowledge of number of instructions executed of each type.

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A Cyclic Prefix OFDM System with BPSK Modulation

By Er. V ipin Mittal & Prof. S.R. Mittal
Indus Institute of Engineering and Technology

Abstract - Orthogonal Frequency Division Multiplexing (OFDM) is a promising technique for high data rate wireless communications because it can combat inter-symbol interference caused by the dispersive fading of wireless channels. A FDM channel is like water flow out of a faucet, in contrast the OFDM signal is like a shower. In a faucet all water comes in one big stream and cannot be subdivided. OFDM shower is made up of a lot of little streams. The demand for high speed mobile wireless communications is rapidly growing. OFDM technology promises to be a key technique for achieving the high data rate capacity and spectral efficiency requirements for wireless communications of the near future which was a source of motivation for this project. Here in this paper, we simulate a cyclic prefix OFDM system with Binary Phase Shift Keying Modulation on each subcarrier. CP-OFDM system includes a repetition code and interleaving across subcarriers as well as a Rayleigh fading channel model with exponentially decaying power profile.

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A Cyclic Prefix OFDM System with BPSK Modulation

Er. Vipin Mittal [α] & Prof. S.R. Mittal [σ]

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The demand for high speed mobile wireless communications is rapidly growing. OFDM technology promises to be a key technique for achieving the high data rate capacity and spectral efficiency requirements for wireless communications of the near future which was a source of motivation for this project. Here in this paper, we simulate a cyclic prefix OFDM system with Binary Phase Shift Keying Modulation on each subcarrier. CP-OFDM system includes a repetition code and interleaving across subcarriers as well as a Rayleigh fading channel model with exponentially decaying power profile.

I. Introduction

High speed communications over broadband wireless channels has emerged as a key feature of future communications systems due in part to the explosive interest in information technology applications, including wireless networks, mobile computing, high speed mobile internet, and video transmission over wireless channels. The demand for higher information capacity in these and other similar applications has motivated the use of broadband wireless channels in order to provide wider bandwidth and higher data rates.

OFDM is a widely recognized modulation technique for high data rate communications over wireless links. Because of its capability to capture multipath energy and eliminate inter-symbol interference, OFDM has been chosen as the transmission method for several standards, including the IEEE 802.11a wireless local area network (WLAN) standard in the 5-GHz band, the IEEE 802.11g WLAN standard in the 2.4-GHz band. Also, the OFDM-based physical layer is being considered by several standardization groups, such as the IEEE 802.15.3 wireless personal area network (WPAN) and the IEEE 802.20 mobile broad-band wireless access (MBWA) groups. The heightened interest in OFDM has resulted in tremendous research activities in this field to make the real systems more reliable and less costly in practice.

OFDM has been practically implemented in the United Kingdom in the form of digital Video broadcasting- Terrestrial (DVB-T) for quiet sometime now and it has been found useful there. In addition to that earlier this year this technology has given birth to a new concept known as "telemedicine" where doctor and patient can be in different parts of the globe but the patient can still consult the doctor. There can be nothing more to humanity! This is made possible by the high speed data transfer offered by this technique. We feel OFDM is a potential candidate for the physical layer of 4G mobile communication.

II. Niceties

a) Channel Modeling

In order to evaluate the effectiveness of a given channel coding and processing technique before actual implementation, some model of the channel must be developed that adequately describes the environment. Such analysis reduces the cost of developing a complex system by reducing the amount of hardware that has to be developed for evaluation of performance. By examining the details of how a signal is propagated from a transmitter to a receiver, we can effectively generate a better hardware of transmitter and receiver as physical processes can be judged which modify the transmitted signal.

It is usually described by three components: An input alphabet, an output alphabet and a transition probability 'p' (i,o).

b) Multipath Fading

Modern During propagation, radio signals weaken with distance. This is due to the wave front of the radio signal expanding and thus reducing in power density. In free space, the propagating wave expands as a sphere and thus the power density reduces in proportion to the surface area of this sphere. If the signal is transmitted using a directional antenna, the signal still expands as a sphere, except that the energy density is concentrated to one or more areas (see Figure). If we transmitted the same energy from an omnidirectional as a direction antenna, the integrated energy over the surface area of the RF sphere, the energy would be the same. The figure shows an expanding RF pulse, if we were to imagine a sinusoidal

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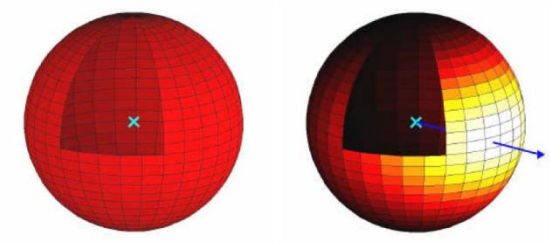
transmission (single frequency) it would be continuous stream of expanding spheres, with the power of these following a sinusoid waveform.

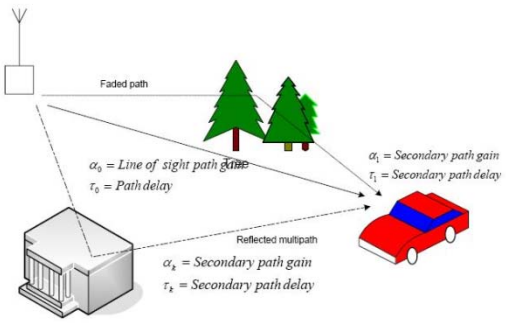


(a) (b)

c) Multipath Fading

Mathematically, Fading is modeled as a time-varying random change in amplitude and phase of transmitted signal. It is the distortion that a signal experiences.

If the path from the transmitter to receiver either has reflections or obstructions, we get fading effects. In this case, signal reaches the receiver from many different routes, each a copy of original. Each of these rays, called multipath signals/waves, has a slightly different delay and slightly different gain. This results in either constructive or destructive interference, amplifying or attenuating the signal power at receiver. Strong destructive interference is frequently referred to as a deep fade and thus SNR drops significantly.



$$h_c(t) = \sum_{k=0}^{K-1} \alpha_k \delta(t - \tau_k)$$

α_k = Compl ex p ath gain

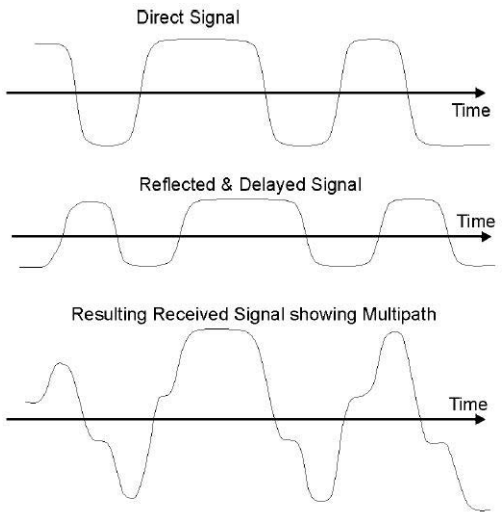
τ_0 = Normalized path delay relative to LOS

$\Delta_k = \tau_k - \tau_0$ difference in path time

d) Delay Spread

Delay spread is a measure of the spread in the time over which the multipath signals arrive. It is a measure of the time dispersion of a channel, and is very important in determining how fast the symbol rate can be in digital communications. A symbol is a period over which one or more groups of bits of information are sent. For a single carrier transmission, using Binary Phase Shift Keying (BPSK) as the modulation scheme, each symbol carries one bit of information. The symbol corresponds to the period required to send the phase information as 0° or 180°, which corresponds to the digital information of zero or one respectively. The faster the phase is varied the faster the symbol rate and the higher the data rate and bandwidth. For OFDM transmission, each symbol corresponds to a parallel transmission of many low bandwidth carriers. The symbol time in this case corresponds to the period over which the amplitude and phase of the data carriers is remained fixed corresponding to one data vector. Delay spread results in time blurring, where energy from previous data symbols becomes mixed in with current symbols. This causes interference, known as Inter-Symbol Interference (ISI), because previous symbols are uncorrelated, effectively adding noise to the signal. Single carrier transmissions are particularly prone to problems caused by delay spread as it normally sets the upper limit on symbol rate. This is because the bit error rate (BER) increases as the delay spread time becomes a significant fraction of the symbol time. Simple modulation schemes such as BPSK can tolerate a delay spread of approximately 10 - 20% of the symbol period; anymore and the BER is too high.

However, higher modulation schemes such as 16-QAM, 256-QAM, etc, which have a higher spectral efficiency, are much more sensitive to ISI and thus the delay spread must be less than several percent of the symbol period.



e) Equalization

One method to overcome the limitations of delay spread for single carrier transmission is to use equalization. The aim of equalization is to find an inverse filter that compensates for the ISI so that all the multipath signals become shifted and aligned in time, rather than being spread out. For example, the GSM phone system, which uses 270 k symbols/s (3.7 ms symbol period), can tolerate a delay spread of up to 15 ms. This is a delay spread of over four symbol periods. The problem with equalization is that it becomes increasing difficult, as the ISI is spread over more symbols. Errors in equalization, particularly for delay spreads over more than one symbol, make it difficult to use higher modulation schemes in multipath

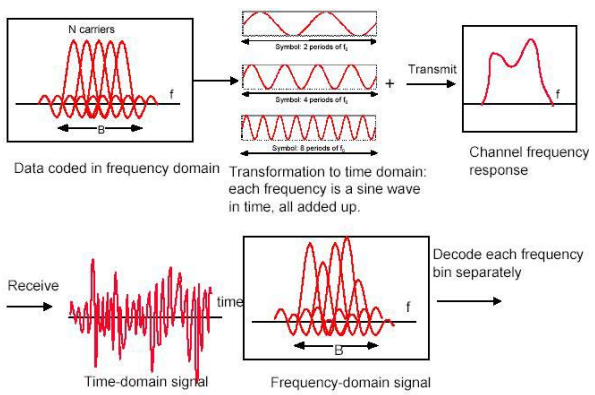
environments. OFDM systems work by resolving the frequency domain so that the width of the subcarriers is much narrower than frequency selective fading of the radio channel. This makes the frequency response over the bandwidth of each subcarrier effectively flat. Only simple equalization is required for each subcarrier for data transmission as the flat fading on each subcarrier only results in an amplitude scaling and a phase rotation. For coherent transmissions, equalization is implemented by transmitting reference pilot symbols or tones, which are set to an amplitude and phase known by both the transmitter and receiver. The channel response is then estimated by dividing the received subcarrier IQ vector of the pilot symbol or tone by the known transmitted vector. This measured channel response is then used to equalize the transmitted data. No equalization is needed for transmissions using differential phase modulation. With this method, the amplitude of the subcarrier is not used for carrying information and so its value is not important. With differential phase modulation the data is transferred as a phase difference between successive symbols. This compensates for any phase offset caused by the propagation channel.

f) Principle of OFDM System

OFDM is a parallel transmission scheme, where a high-rate serial data stream is split up into a set of low rate substreams, each of which is modulated on a separate SC (FDM). Thereby, the bandwidth of the SCs becomes small compared with the coherence bandwidth of the channel; that is, the individual SCs experience flat fading, which allows for simple equalization.

This implies that the symbol period of the substreams is made long compared to the delay spread of the time-dispersive radio channel. By selecting a special set of (orthogonal) carrier frequencies, high spectral efficiency is obtained because the spectra of the SCs overlap, while mutual influence among the SCs can be avoided.

The derivation of the system model shows that by introducing a cyclic prefix, the orthogonality can be maintained over a dispersive channel.



g) Orthogonality

Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier transmission technique, which divides the available spectrum into many carriers, each one being modulated by a low rate data stream. In Communications, multiple-access schemes are orthogonal when an ideal receiver can completely reject arbitrarily strong unwanted signals using different basis functions than the desired signal. One such scheme is TDMA, where the orthogonal basis functions are non-overlapping rectangular pulses ("time slots"). Another scheme is orthogonal frequency-division multiplexing (OFDM), which refers to the use, by a single transmitter, of a set of frequency multiplexed signals with the exact minimum frequency spacing needed to make them orthogonal so that they do not interfere with each other. Well known examples include a and g versions of 802.11 Wi-Fi; Wimax; ITU-T G.hn, DVB-T, the terrestrial digital TV broadcast system used in most of the world outside North America; and DMT, the standard form of ADSL.

One major limitation faced by OFDM is its high sensitivity to phase noise introduced by local oscillators. Phase noise is the phase difference between the phase of the carrier signal and the phase of the local oscillator. The distortion caused by this phase noise is characterized by a CPE term and an ICI term. CPE term represents the common rotation of all constellation points in the complex plane, while the ICI term behaves like AWGN.

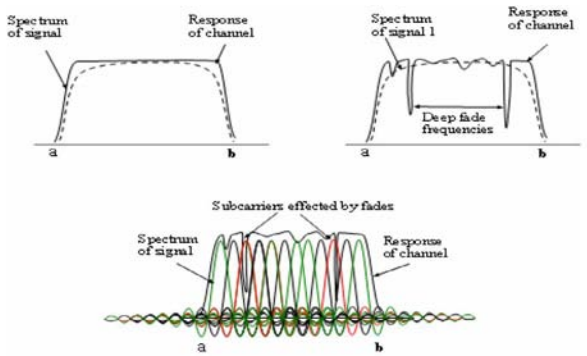


Figure (a) Signal & Channel Frequency Response are well matched (b) Data lost due to Fading (c) With OFDM, only a small subset of data is lost due to fading due to a number of sub-carriers.

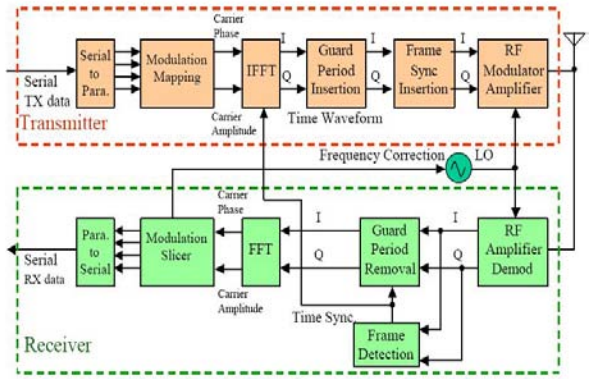
h) Pilot Symbols

A Pilot is a signal, usually a single frequency, transmitted over a communication channel for supervisory or control or reference purposes. A pilot tone of 19 KHz indicates that there is information at 19*2=38KHz. The receiver doubles the frequency of the pilot tone and uses it as a phase reference to demodulate information. Normally a guard band of ±4KHz is used to protect the pilot tone from interference. Pilots are used in OFDM for frame

detection, carrier frequency offset estimation, and channel estimation.

i) OFDM Generation & Reception

OFDM signals are typically generated digitally due to the difficulty in creating large banks of phase lock oscillators and receivers in the analog domain. Figure below shows the block diagram of a typical OFDM transceiver. The transmitter section converts digital data to be transmitted, into a mapping of subcarrier amplitude and phase. It then transforms this spectral representation of the data into the time domain using an Inverse Discrete Fourier Transform (IDFT). The Inverse Fast Fourier Transform (IFFT) performs the same operations as an IDFT, except that it is much more computationally efficiency, and so is used in all practical systems. In order to transmit the OFDM signal the calculated time domain signal is then mixed up to the required frequency. The receiver performs the reverse operation of the transmitter, mixing the RF signal to base band for processing, then using a Fast Fourier Transform (FFT) to analyze the signal in the frequency domain. The amplitude and phase of the subcarriers is then picked out and converted back to digital data. The IFFT and the FFT are complementary function and the most appropriate term depends on whether the signal is being received or generated. In cases where the signal is independent of this distinction then the term FFT and IFFT is used interchangeably.



j) Interleaving

Let's understand this concept with the help of an example. Suppose there are four families (each having four members) going on a holiday in there four cars. In each of the cars there is exactly one family. Now if unfortunately a car meets with an accident then one whole family will be finished. But suppose if they were to be seated differently i.e. if each car had exactly one member of each family and then the accident were to happen then no single family would be finished. The loss would be equal for all the families. This is certainly better. Same is with our data. If we send our data this way then we can eliminate some noise effect like burst noise effect.

k) Cyclic Prefix

In an OFDM, the cyclic prefix is a repeat of the end of the symbol at the beginning. The purpose is to allow multipath to settle before the main data arrives at receiver. The receiver is normally arranged to decode the signal after it has settled because this is when the frequencies become orthogonal to each other. The length of cyclic prefix is equal to guard interval.

III. System Overview

Wireless multi-carrier transmission system is based on Orthogonal Frequency-Division Multiplexing (OFDM) including a simple channel coding scheme for error correction and interleaving across subcarriers for increased frequency diversity.

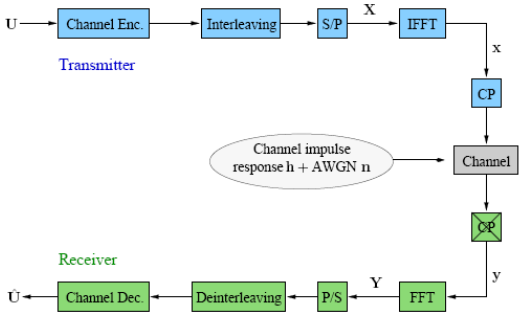
a) Some Assumptions

- Usage of Cyclic Prefix
- Impulse response of the channel shorter than cyclic prefix.
- Slow fading effects so that the channel is time invariant over the symbol interval.
- Rectangular windowing of the transmitted pulses.
- Perfect Synchronization of transmitter and receiver.
- Additive, White, Gaussian Noise channel.
- Data Rate of OFDM signal: 1Mbps/carrier
- Guard Length: 16
- Guard Type: Cyclic Extension

b) Values of Constants

N_{real}	10,000 OFDM symbols
N_c	128 subcarriers
N_{ch}	10 channel coefficients
C_{att}	2 for channel profile

The basic communication model used in this research paper is as shown in the figure:



IV. Findings

We obtained the following graphical results:

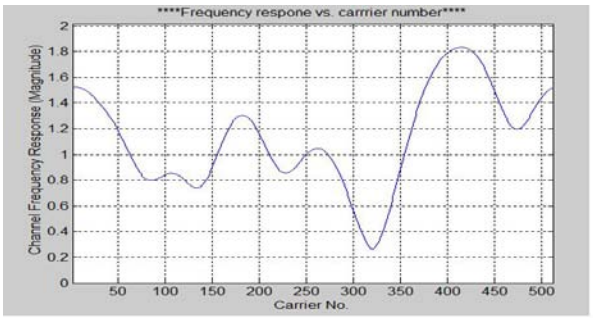


Figure a : Frequency Response at code rate, R=1(without interleaving)

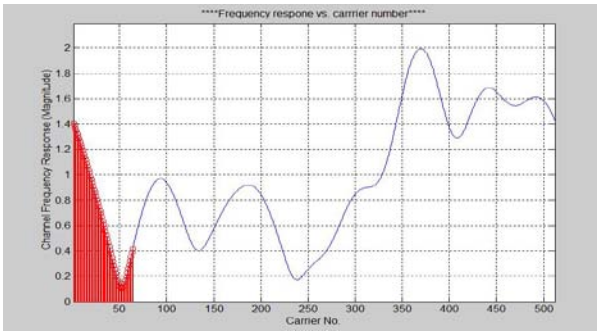


Figure b : Frequency Response at code rate, R=1/64 (without interleaving)

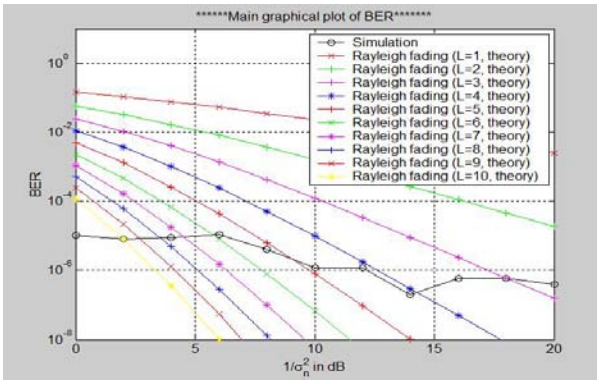


Figure c : Analytical BER Performance (without interleaving)

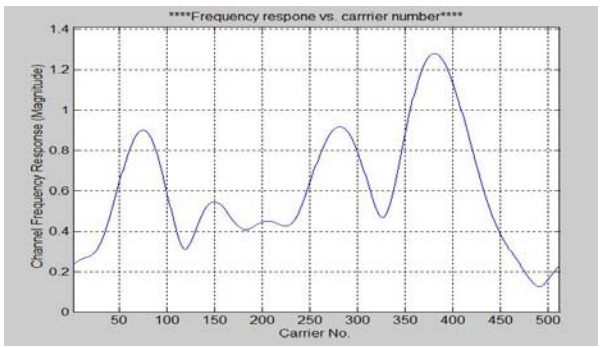


Figure d : Frequency Response at code rate, R=1(with interleaving)

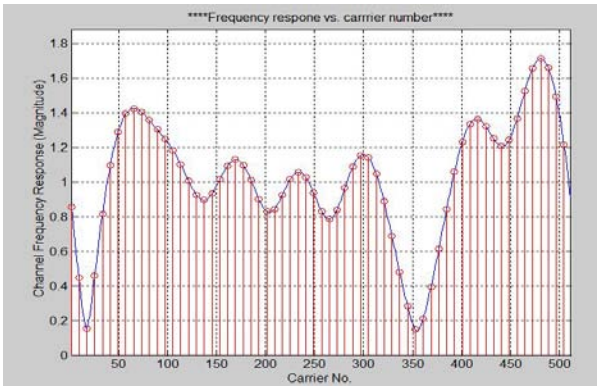


Figure e : Frequency Response at code rate, R=1/64(with interleaving)

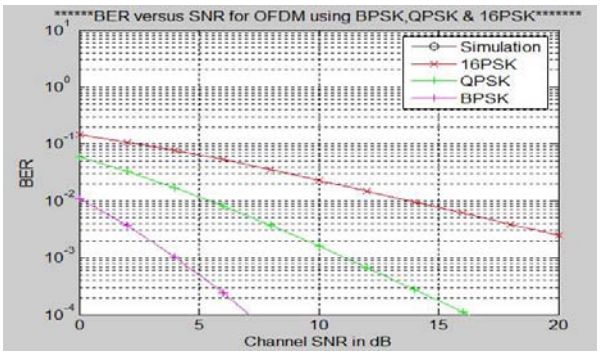


Figure f : BER vs. SNR for OFDM using BPSK, QPSK & 16PSK

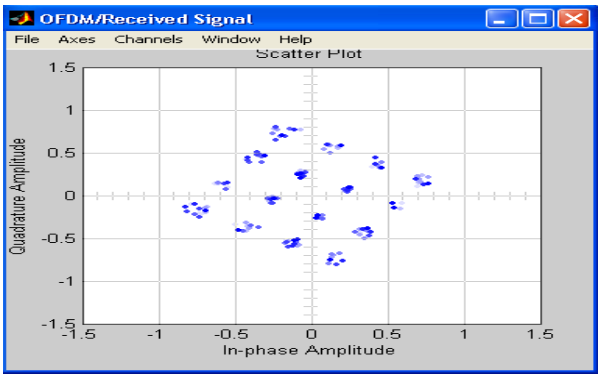


Figure g : Received OFDM Signals

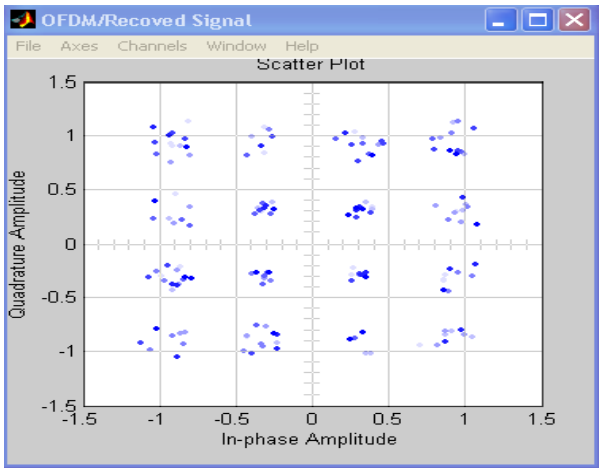


Figure h : Recovered OFDM Signals

V. Conclusion

The results show that using QPSK the transmission can tolerate a SNR of >10-12 dB. The bit error rate BER gets rapidly worse as the SNR drops below 6 dB. However, using BPSK allows the BER to be improved in a noisy channel, at the expense of transmission data capacity. Using BPSK the OFDM transmission can tolerate a SNR of >6-8 dB. In a low noise link, using 16PSK can increase the capacity. If the SNR is >25 dB 16PSK can be used, doubling the data capacity compared with QPSK.

The simulations shown above calculated the signal to noise ratio based on the power of the time domain signal waveform and the power of the time domain noise waveform, with no consideration of the signal bandwidth. At the receiver the signal is filtered by the FFT stage, thus making the receiver only see noise within the signal bandwidth. The simulations were performed using 800 carriers and generated using a 2048-point IFFT. The nyquist bandwidth is half the transmission sample rate as the signal is real (i.e. no imaginary components) and so the nyquist bandwidth corresponds to 1024 carriers. The signal bandwidth is thus 800/1024 = 0.781 or 78.1% of the nyquist bandwidth. Since the receiver was only seeing 78.1% of the total noise the error rate is lower than it should be. The correct SNR values can be found by adding 1.07 dB (10log10(0.781)) to the scale in Figure (f).

Also we noted down that to achieve the same BER performance, SNR must be higher. SNR performance loss reduces almost proportionally with number of pilot tones, thus the loss when using 4 pilot tones is 4 times lower (in db).

Table I : SNR Required and Bit Rate for a Selection of Coding & Modulation Schemes

Subcarrier Modulation	Code Rate	SNR for BER=2*10^{-4}	Bit Rate(Mbps) at Guard period duration, 1/4	Bit Rate(Mbps) at Guard period duration, 1/32
BPSK	½	5.4	4.98	6.03
QPSK	½	16.3	8.71	10.56
16PSK	½	22.8	17.42	12.06

Table II : B: BPSK Modulation, Q: QPSK Modulation, P: 16PSK Modulation

Number of pilot symbols	BER 1×10^{-2}			BER 1×10^{-3}			BER 1×10^{-4}			BER 1×10^{-5}		
B	*Q*	*P*	*B*	*Q*	*P*	*B*	*Q*	*P*	*B*	*Q*	*P*	*B*	*Q*	*P*
1	1	1	1.55	2.5	2.7	1.2	2.4	2.9	1.0	2.4	3.0	0.8	2.35	3.2
2	2	2	0.6	1.3	1.5	0.35	1.3	1.6	0.2	1.2	1.7	0.15	1.2	1.7
3	3	3	0.3	0.85	1.0	0.2	0.8	1.1	0.15	0.8	1.1	0.12	0.7	1.1
4	4	4	0.2	0.65	0.8	0.15	0.6	0.8	0.1	0.6	0.8	0.10	0.45	0.8

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Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
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References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

INDEX