Online ISSN: 2249-4596
Print ISSN: 0975-5861

Global Journal

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Electrical and Electronics Engineering

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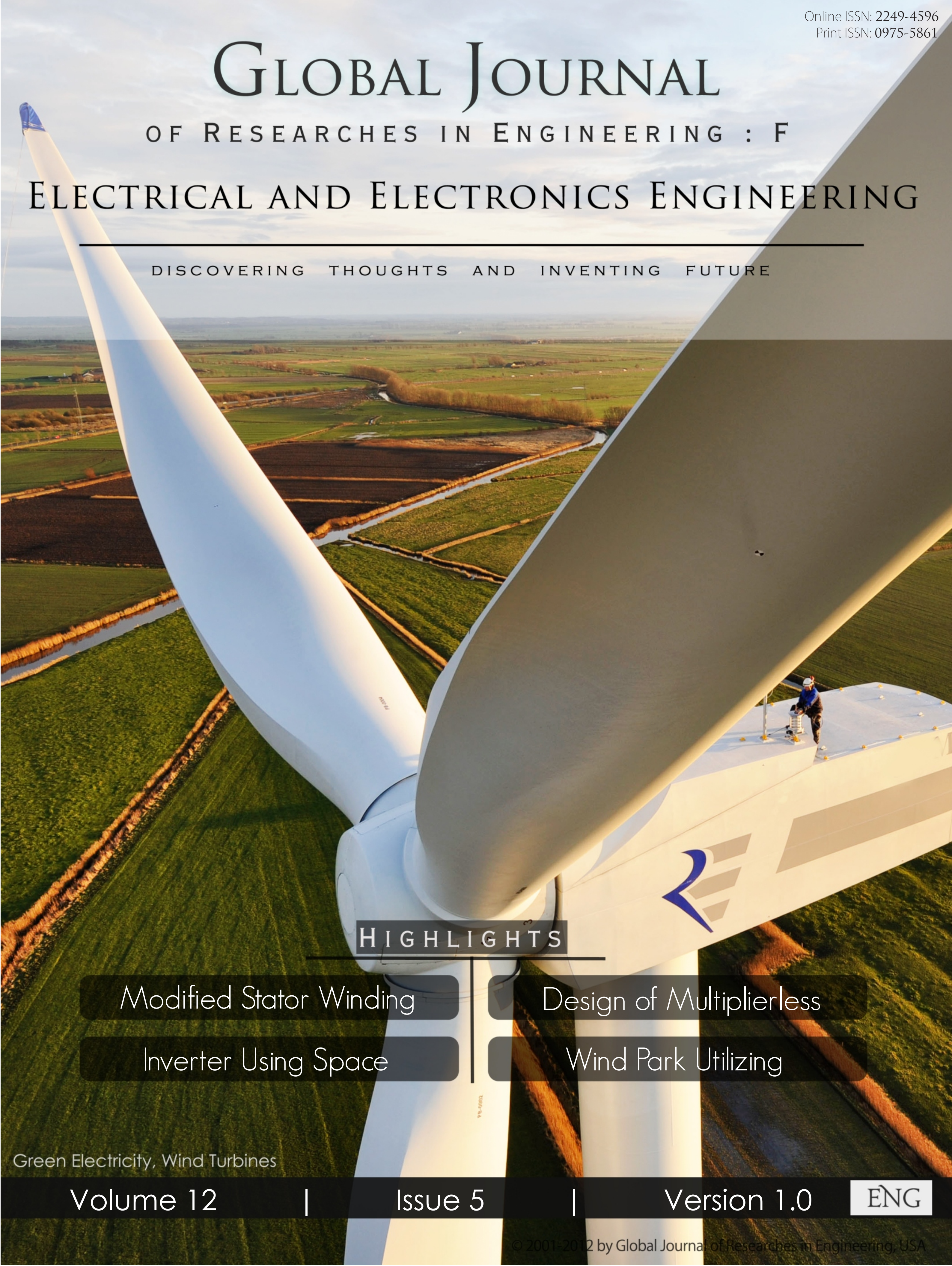

Highlights

Modified Stator Winding

Design of Multiplierless

Inverter Using Space

Wind Park Utilizing

Green Electricity, Wind Turbines

Volume 12 | Issue 5 | Version 1.0

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Global Journal of Researches in Engineering: F
Electrical and Electronics Engineering

Global Journal of Researches in Engineering: F
Electrical and Electronics Engineering
Volume 12 Issue 5 (Ver. 1.0)

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Contents of the Volume

Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 5 Version 1.0 April 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Performance of Three Phase Induction Motor Using Modified Stator Winding

By C. Saravanan, A. Mohamed Azarudeen & S. Selvakumar
Tagore Engineering College/ Anna University

Abstract - Induction machine is an important class of electrical machines which finds wide applications as a motor in industryand in its single phase form in several domestic applications. More than 85% of industrial motors in use today are in factinduction motors. The minimization of electrical energy consumption through better motor design becomes a major concern. This paper proposes a novel technique to improve the performance of induction motor. By using a modified stator winding arrangement the efficiency has been improved by 7% and tested in laboratory. Experimental results and simulations have been presented to validate the results.

Keywords : Induction motor, Squirrel cage and Mathematical modeling.

GJRE- F Classification : FOR Code: 0906

PERFORMANCE OF THREE PHASE INDUCTION MOTORUSING MODIFIED STATOR WINDING

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Performance of Three Phase Induction Motor Using Modified Stator Winding

C. Saravanan [α], A. Mohamed Azarudeen [σ] & S. Selvakumar [ρ]

Abstract - Induction machine is an important class of electrical machines which finds wide applications as a motor in industry and in its single phase form in several domestic applications. More than 85% of industrial motors in use today are in fact induction motors. The minimization of electrical energy consumption through better motor design becomes a major concern. This paper proposes a novel technique to improve the performance of induction motor. By using a modified stator winding arrangement the efficiency has been improved by 7% and tested in laboratory. Experimental results and simulations have been presented to validate the results.

Keywords : Induction motor, Squirrel cage and Mathematical modeling.

I. Introduction

Induction motor drives with cage-type machines have been the work-horses in the industry for variable-speed applications in a wide power range that covers fractional horse-power to megawatts. These applications include pumps and fans, paper and textile mills, subway and locomotive propulsions, electric and hybrid vehicles, machine tools and robotics, home appliances, heat pumps and air-conditioners, rolling mills, wind generation systems, etc. In addition to the process control, the energy saving aspect of variable-frequency drives is getting a lot of applications nowadays.

During the last few years, the significance of the squirrel cage induction motors in speed and position controlled drives have grown drastically. In recent years due to the advances in the development of high speed computers and power electronics technology with associated high speed microcontrollers, AC drive systems have been a viable alternative to DC machines for variable speed applications. This increased interest in induction motors is because of its merits over the other types of industrial motors [1].

These merits include: lightness, simplicity, ruggedness less initial cost, high torque-inertia ratio, capability of much higher speed, ease of maintenance etc. Moreover the most important feature which makes the induction motor most viable alternative to DC drive system is its cost per KVA which is approximately one fifth of that of DC motor and its suitability in hostile environment. Thus in the present situation induction motor consumes large amount of electric power and an increase in the efficiency of the motor will reduce the consumption of the electric power which in turn further reduces its cost [2].

The major losses in the induction motor are in the stator windings in terms of stator copper loss. This paper proposes a novel method of reducing the stator copper loss by using modified stator winding arrangement.

The design of motor is done by increasing the active material part in the motor. Using active material effectively will increase the efficiency of the motor to a considerable extent. The proposed motor is modeled and simulated with the help of SIMULINK model. [3]

Alternating current supplied to the primary winding from an electric power system includes an opposing current in the secondary winding, when the latter is short circuited or closed through external impedance. Relative motion between the primary and secondary structure is produced by electromagnetic forces corresponding to the power transferred across the air gap by induction.

The essential feature which distinguishes the induction machine from other type of electric motors is that the secondary currents are created solely by induction, as in a transformer instead of being supplied by a DC exciter. The equivalent circuit of the induction motor is very similar to that of a transformer. The rotor currents are at a slip frequency and it is incorporated into the circuit in a simple way [4].

II. Efficiency Improvement

The efficiency of the motor is increased by using multi-strand with multi turn coils in the stator winding. Two conductors separated from each other by a pole pitch form one turn. Multi strand with multi-turn coils will increase the area of the conductors in a slot. This increases the active material present in the stator winding resulting in increase of efficiency. The reduction in the stator resistance is explained by the following equations:

The resistance of stator winding with single strand with multi turn coil, $\mathbf{R=\varrho l/A}$

Where, R= Resistance of the stator winding and

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ϱ=Resistivity of the winding

l=Length of the winding

Stator copper loss = $I^2R = I^2 \varrho l/A$

Resistance of the winding with multi strand with multi-turn coil with X number of strand per turn.

$$R=\varrho l/XA$$

Stator copper loss = $I^2R = I^2\varrho l/XA$, where X=1, 2, 3 ...N

Therefore, with increase in number of strands in a turn, the area of the coil increases, hence stator resistance decreases to a considerable extent. (The inductance value is same as the existing motor)

III. Measurement of Motor Parameters

a) Stator Resistance

The stator resistance per phase is measured using a suitable meter. The resistance values in the order of few ohms and the resistance values are crucial to determine the winding data. Hence the resistance should be measured with high accuracy.

b) No Load Test

The stator of the induction motor is energized by applying rated voltage at rated frequency. The corresponding input power per phase and line current is measured accurately under no-load conditions.

c) Locked Rotor Test

The rotor of the induction motor is locked to keep it at standstill and a low voltage is applied to circulate rated stator currents. Input power per phase is measured along with the input voltage and the stator current. The slip is unity for the locked rotor condition and hence the circuit resembles that of a secondary-shorted transformer.

d) Efficiency of Induction Motor

In an induction motor the total losses consist of copper losses, core losses and friction and windage losses are occurred. There are copper losses and core losses in the stator, and copper losses and friction losses in the rotor. Actually there is some core losses in the rotor. Under operating conditions, however, the rotor frequency is so low that it may logically be assumed that all core losses occur in the stator only. The efficiency of induction motor is determined by loading the motor and measuring the input and output directly.

$$\eta = \text{Poutput/Pinput}$$

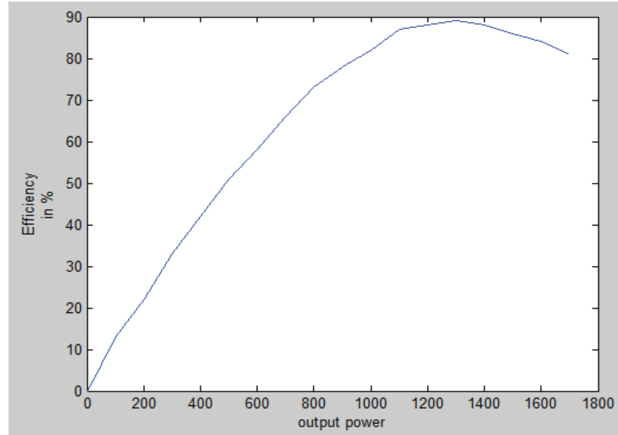

Fig.1 : Efficiency characteristics of induction motor

e) Power Factor of Induction Motor

When the winding is changed from single strand with multi turn coil into multi strands multi-turn coil the power factor increases from 0.8 to 0.85.

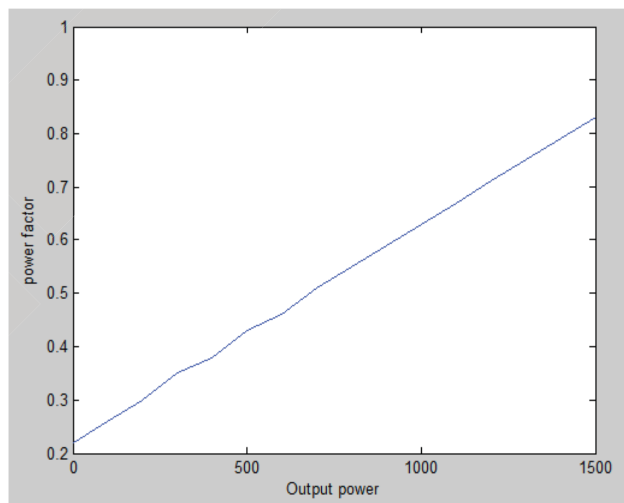

Fig.2 : Power factor of induction motor

IV. Computation of Steady State Performance of Induction Motor

The slip is chosen in place of rotor speed as it is non dimensional and so it is applicable to any motor frequency. Near the synchronous speed, at low slips, the torque is linear and is proportional to slip beyond the maximum torque the torque is approximately inversely proportional to slip.

V. Dynamic Simulation of Three Phase Induction Motor

Torque and speed characteristics are obtained from this model.

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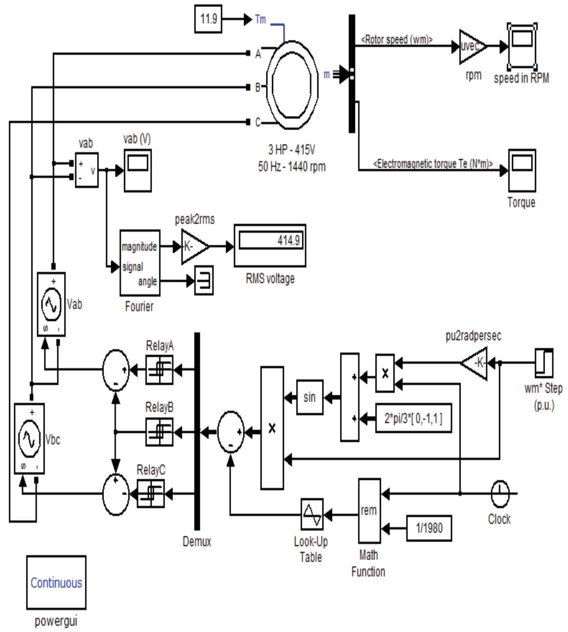

Fig.3 : The SIMULINK block diagram of three phase induction motor

Table.1 : Block parameters of induction motor

Quantity	Input values
No of phases	3
Number of poles	4
Frequency	50Hz
Line voltage	410v
Stator resistance	1.9Ω
Mutual inductance	0.26674H

A three phase motor rated 3hp, 410V, 1440 rpm is fed by a sinusoidal PWM inverter. The base frequency of the sinusoidal reference wave is 50Hz. The PWM inverter is built entirely with standard SIMULINK blocks. Its output goes through controlled voltage source blocks before being applied to the asynchronous machine block's stator windings. The machine's rotor is short circuited. Its stator leakage inductance is set to twice its actual value to simulate the effect of a smoothing reactor placed between the inverter and the machine. The load torque applied to the machine's shaft is kept constant. The motor is started from standstill. The speed set point is set to 1.0pu, or 1440 rpm. This speed is reached after 0.8s.

The noise introduced by the PWM inverter is also observed in the electromagnetic torque waveform. However, the motor's inertia prevents this noise from appearing in the motor's speed waveform.

a) Rotor speed of an induction motor

Figure 4 & 5 shows the rotor speed curve of winding with the single strand with multi turn coil and multi strand with multi turn coil of the induction motor respectively. The rotor speed is gradually increased to the rated speed.

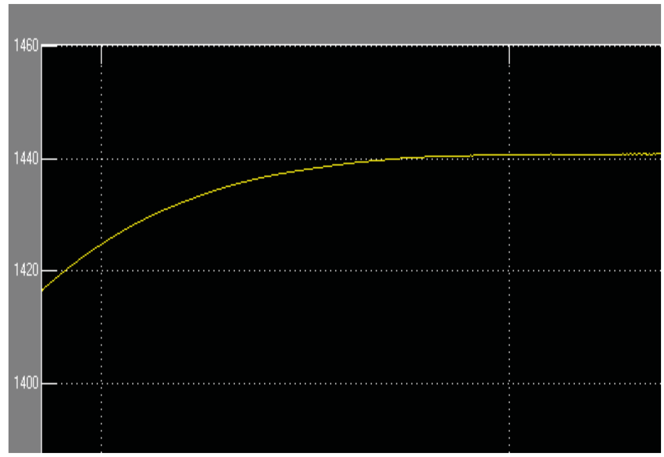

Fig.4 : Rotor speed of existing induction motor

Above Figure shows the motor with single strand with multi turn coil attain a steady state speed of 1440 rpm.

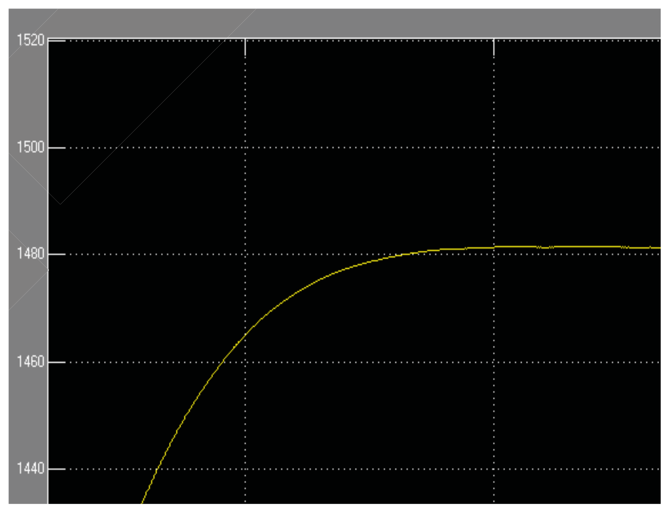

Fig.5 : Rotor speed of new induction motor.

Above Figure shows the motor with multi strand with multi turn coil attain a steady state speed of 1480 rpm.

b) Time Response of Electromagnetic Torque in Three Phase Induction Motor

In Fig.6. the time response of electromagnetic torque of three-phase induction motor is expressed. The electromagnetic torque of three-phase induction motor is firstly variable in 0 to 0.4 second. The rated torque is reached at 0.8 seconds.

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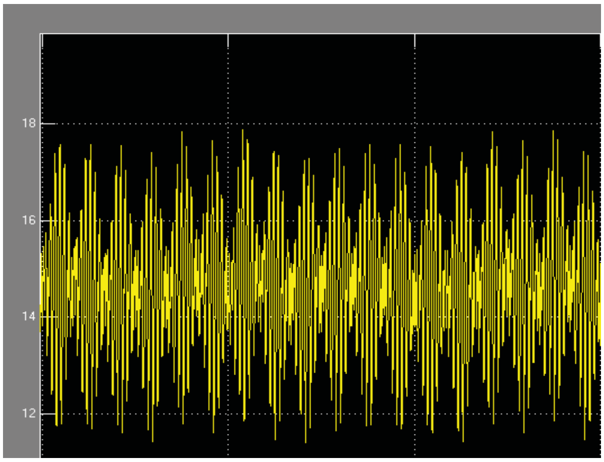

Fig.6 : Time response of electromagnetic torque of existing induction motor

Above Figure shows the torque of the motor with single strand with multi turn coil.

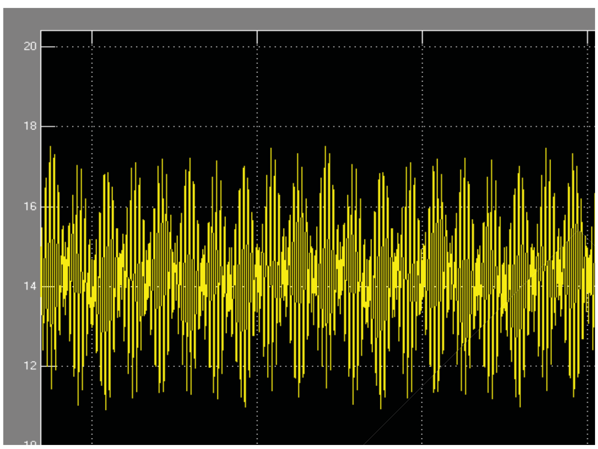

Fig.7 : Time response of electromagnetic torque of new induction motor.

Above Figure shows the torque of the motor with multi strand with multi turn coil.

Table 2 : Comparision of Single –Turn and Multi-Turn Motor

Parameters	Existing motor	Motor with modified stator winding.
Voltage	410v	410v
Frequency	50Hz	50Hz
Efficiency	80.7%	87.8%
Stator copper loss	240w	83w
Rotor copper loss	120w	107w
Fixed loss	167w	167w
Power factor	0.79	0.85

Table 2 shows the comparison of efficiency and losses for the existing motor and new motor. The efficiency is increased in the new motor.

Fig.8 : Existing induction motor

Above Figure shows the winding of the motor with single strand with multi turn coil.

Fig.9 : New induction motor

Above Figure shows the winding of the motor with multi strand with multi turn coil.

VI. Conclusion

A novel method to increase the efficiency of three phase squirrel cage induction motor is new. The dynamic simulation of the motor is performed by its mathematical modeling. The stator copper loss is minimized by using modified stator winding arrangement. The hardware is proposed after doing the above modifications and thus the efficiency of the motor is increased, the motor is also modeled and simulated with the help of the MATLAB SIMULINK model.

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Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 5 Version 1.0 April 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Security Issues in Wireless Broadband Networks

By Dr. Gurjeet Singh & Dr. Jatinder Singh
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Abstract - In this paper, we would be discussing about major issues pertaining to security feature in broadband technology. To know different securities aspect which may hinder advancement of broadband technology. In this research paper taking up Wimax broadband technology working concepts and it's different security features, which needs to be taken up at a clear scale.

Keywords : Security, Broadband Networks.

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Dr. Gurjeet Singh [α] & Dr. Jatinder Singh [σ]

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Keywords : Security, Broadband Networks.

I. Introduction

Broadband in the general term also referred as high-speed network connections. Broadband describes a medium that can carry signals from multiple independent network carriers on a single coaxial or fiber optic cable .While the benefits are compelling, there are still a number of challenges with moving to broadband Internet. Spotty geographic coverage and installation challenges are a significant impediment. As cable and DSL providers accelerate their deployment plans, this situation is improving, but there are still significant challenges. Network security is another very significant issue, and one that is becoming increasingly visible as hacker attacks on home PCs [1]

There are so many profits when we adapt a broadband network, this broadband network can spread through different geographic but installation is the major problem. Internet connections via cable modem and Digital Subscriber Line (DSL) are frequently known as broadband Internet connections. Cable and DSL providers speed up their operations plan and the conditions are improving, but network security is the major concern.

Security problems are increasing rapidly as hacker attacks on home PCs and major company websites such as government organizations. One of the most compelling uses of broadband connections is to allow enterprises to Connect branch offices and telecommuters into the corporate network with high-speed remote access. [2]

To come across the suggested subsequent security solutions:

1. **Firewall:** To access control policy connecting two networks firewall implemented. Firewalls might be dependent on the software like checkpoint, CA or hardware appliance similar to Net Screen, watch guard and Nokia etc. Personal firewalls solutions still give the impression of being for Home users resembling Network ICE etc.
2. **Anti-Virus:** Anti-Virus looks for patterns in the files or memory of your computer to specify possible occurrence of a recognized virus.
3. **Encryption:** To think about encrypting traffic at your PC communications are mostly responsive. The beginning of denial of service attacks from these computers VPN, SSL provide secure for e-commerce transactions the Firewall with VPN protection secures sensitive data to the remote site and prevent both U-turn attacks and products similar to Net Screen PGP and Cisco etc. The type of tracking appears the danger of cookies. [4]
4. Modem Security: In some cases modem configuration & authentication information would be stored on modem, in others, stored on your computer.
5. Shared Cable Modem Connection: Cable networks are shared among numerous subscribers in a given neighborhood. As a result, neighbors could monitor your transmission by using sniffer. Please ensure service provider upgraded networks and equipments to DOCSIS (Data over Cable Service Interface Specification).
6. **Content Inspection:** Since interactive technologies like Java, JavaScript, ActiveX are a big part of broadband content sites & emails, as well as potentially an emerging vehicle for hack attacks. It is recommended that disable mobile codes such as Java, JavaScript & ActiveX. Disable scripting features in e-mail programs. You may want to explore active content security products such as Trend Micro, CA, and Finjan etc.
7. **System Security:** It is recommended that you log off & power down your PC when you are not using your connection.

Commonly, security issues at home and small office installations involve are:

1. The Internet to your computer approaching in the form of Unauthorized Internet traffic.
2. AKA software home work to Unauthorized Information departing out from your Hard Drive to someone else web Server.
3. Sudden outflow in the firewall left disable, computer left in DMZ etc.

Suddenly home work Unauthorized Information departing out is mainly a function of spyware and programs. The sum of home work programs that are rising through the day. [5]

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To use Cable/DSL the most common solution is to share Broadband Internet connection. The Internet desires identify to which computer it belongs to utilize a small number of computers to share one Internet connection from the information that comes. The major function of Cable/DSL Router is to Route the Internet signal to the request computer. This function is called Network Address Translation (NAT). [6]

In this paper we would talk about subject concerning security mechanism can be worked out. In this study, we would decrease the converse various techniques pertaining to security tools and techniques.

II. Introduction to Wimax Technology

Worldwide Interoperability for Microwave Access (WiMax) is an emerging fixed broadband wireless technology that will deliver last mile broadband connectivity in a larger geographic area than Wi-Fi. It is expected to provide coverage anywhere from one to six miles wide. Such WiMax coverage range is expected to provide fixed and nomadic wireless broadband connectivity without necessarily having a line-of-site (LOS) with a base station. WiMax will also enable greater mobility, higher speed data applications, range and throughput than its counterpart, Wi-Fi.

WiMax uses the IEEE 802.16 standards specifications (802.16d and g). The IEEE 802.16d specification is primarily tailored to wireless wide area networks (WWANs). The recently approved IEEE 802.16e specification, the mobile version of WiMax, on the other hand is primarily used for mobile wireless metropolitan networks (WMANs). These two specifications render WiMax architecturally ideal for the last mile, the backhaul, Internet Service Providers, cellular base stations that bypass PSTN's, hotspots, and enterprise networks.

Abilities such as a high bandwidth frequencies between 2 GHz and 11GHz, makes WiMax ideal for data transport. WiMax has a total range of up to 30 miles. This ability is enhanced by WiMax's cell radius of 4-6 miles. More so, WiMax has the ability to support various data transmitting rates of up to 75Mbps. WiMax is gaining tremendous popularity each day. In the recent 3GSM Congress, dozens in the field touted WiMax, the way forward. In fact, on August 8, 2006 Sprint, the number three ranked mobile operator in the US announced that it has selected WiMax technology for its 4G initiatives.

There are several advantages that can be derived from the deployment of WiMax. Firstly, it supports higher throughput rates, higher data speed rates, and wider operating range. These make the technology very useful for deployment in bad terrain areas or in environments with limited wired infrastructure. Moreover, WiMax supports and interfaces easily to other wired and wireless technologies such as Ethernet, ATM, VLANs, and Wi-Fi. Furthermore, WiMax provides network connectivity that explores multipath signals without the stringent requirement of a direct line of sight. Finally, WiMax provides a better Quality of Service (QoS) by taking advantage of smart antenna technology that utilizes the spectrum more efficiently.

The main drawback to the deployment of WiMax is proprietary equipment. WiMax equipment must be able to utilize power efficiently in order to deliver optimum functionality. For WiMax, the output power usage is based on a ranging process that determines the correct timing offset and power settings. Therefore, the transmissions for each subscriber station are supposed to be such that they arrive at the base station at the proper time and at the same power level. When WiMax is deployed outdoors, in non-line of sight environments it may encounter delay, which can cause potential intersymbol interference. Though the use of scalable orthogonal frequency division multiplexing (SOFDM) is meant to try and alleviate this problem, OFDM usage has the problem of generating phase noise, which Broadband introduces two new security challenges:

a. Increased vulnerability to hacker attacks
b. Establishing secure connections to other networks across a public IP network.

III. Research Methodology

As our research is mainly concentrating on security issues and different work mechanism of security tools and techniques through which, we can overcome those. This section discusses the security mechanisms included in IEEE 802.16-2004, IEEE 802.16e-2005, IEEE 802.16-2009, and IEEE 802.16j-200912 to illustrate their functions and provide a foundation for the security recommendations in Section 5. The IEEE 802.16 standards specify two basic security services:

- Authentication
- Confidentiality

Authentication involves the process of verifying the identity claimed by a WiMAX device. IEEE 802.16e-2005 and IEEE 802.16-2009 share the same authentication and confidentiality mechanisms. They both support user authentication in addition to device authentication. Confidentiality involves preventing the disclosure of information by ensuring that only authorized devices can view the contents of WiMAX data messages. The IEEE 802.16 standards do not provide any capability to encrypt management messages.

The IEEE 802.16 standards do not address other security services such as availability and confidentiality protection for management messages; if such services are needed, they must be provided through additional means. Also, IEEE 802.16 security protects communications over the WMAN link between an SS/MS and a BS, but not communications on the wired operator network behind the BS. End-to-end

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security is not possible without applying additional security controls not specified by the IEEE standards.

The latest development in wireless metropolitan area networks is IEEE 802.16, also known as WiMAX (Worldwide Interoperability for Microwave Access) [IEEE04] [IEEE06] [Hos06]. This new standard brings us higher range and speeds compared to 802.11 (WLAN, wireless local area network). The standard is still evolving these days and many problems are not solved yet. One major issue of WiMAX is security. Several scientific papers call this is a big problem. For example [YZZ+05] tells us: "But the security problems in its original protocol may be becoming the most serious obstacle in its marketable producing process." [LL06] states: "As the mobile services supported in the standard, new security problems may be coming and becoming a serious obstacle to develop the WMAN (Wireless Metropolitan Access Network)."The latest standard for WiMAX, IEEE 802.16e [IEEE06], already offers significant security improvements over 802.16-2004 [IEEE04]. It uses better encryption methods and has a more secure key management protocol. Also a new authentication method based on EAP (extensible authentication protocol) [DCA06] [Man03] was added. But still a lot of security issues remain to be solved. Security, and especially authentication and authorization, is crucial to every wireless technology, because without good security the technology is not usable at all. Several researchers have published solutions on the security issues of WiMAX, but are these solutions satisfactory? In this research we will answer that question with a focus on the authentication and authorization part for 802.16e. This paper gives a state of the art on security solutions for WiMAX and it provides a comparison of hese solutions based on certain criteria.

Research questions

The main research question for this paper is:

1. Are the proposed security solutions concerning authentication and authorization for WiMAX satisfactory based on certain criteria?
2. What are the main authentication and authorization aspects in WiMAX?
3. What are the main security issues associated with authentication and authorization for WiMAX?
4. What are the proposed solutions in literature for these security issues?
5. What criteria can be used to analyze those solutions?
6. Which security solutions satisfy the criteria?

IV. Authentication and Authorization

In this paper we will first explain the basic security aspects of WiMAX considering authentication and authorization. Authentication addresses establishing the genuine identity of the device or user wishing to join a wireless network. Authorization addresses determining whether the authenticated user or device is permitted to join the network, see [DCA06]. When a subscriber station (SS) wants to connect to a WiMAX base station (BS), see [Aiko06], at first a connection is established between them. The next step is the authentication of the SS so it can enter the network. SS sends a so-called X.509 certificate [Hou02] to BS to identify itself. The certificate is like a signature for the SS. It contains data like a serial number, the certificates issuer, the public key of the sender, its MAC address etcetera.

After the authentication message SS sends an authorization message to BS. This message contains SSs supported authentication and data encryption algorithms. If BS determines that SS is authorized it sends a message back containing an authentication key (AK), a 4-bit sequence number and a lifetime for it containing the number of seconds before it expires [Aik06]. MS refers here to a mobile subscriber station (SS). When all these steps have been done successfully, the SS has entered the network of BS and it can communicate with all the entities in its network. Authentication and authorization [LL06] the communication between SS and BS is protected by the so-called security associations (SAs). These SAs perform encryption on the data between SS and BS using a 'traffic encryption key' (TEK). Different types of encryption are supported. [Aik06].

V. Security Issues and Solutions

a) DOS (Denial of Service)/ Reply attack

Denial of Service (DoS) is one of the major issues of all types of wireless networks especially broadband wireless networks. When authorized users are not provided a requested service within a defined maximum waiting time, it means that a DoS violation has occurred. It is the most harmful and dangerous attack which can be launched on any layer of broadband Wireless Network. DoS attacks target availability by preventing communication between network devices or by preventing a single device from sending or receiving traffic, where availability ensures that authorized users can access the data, services and network resources from anywhere anytime.

Physical Layer Vulnerabilities WMN and IEEE 802.11 uses 2.4 GHz frequency band while IEEE 802.16 uses 10-66 GHz and 2-11 GHz bands at physical layers. DoS attack can be launched against physical layer by using radio jamming device or a source of strong noise to interfere the physical channels and may compromise the service availability. However this kind of attack is not common as it need specialized hardware equipment to be launched, furthermore jamming attacks can be detected using radio analyzers. It can create great problems during exchange of sensitive information or during warfare. For jamming attack in

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- IEEE 802.11, the attacker needs to be close to the target AP
- IEEE 802.16, the attacker needs to be close to the Base Station (BS)
- WMN, the attacker can launch the attack from anywhere. Due to the vast coverage area and dense deployment of wireless mesh routers in WMN, it is more vulnerable to physical layer DoS attacks.

Currently, IEEE 802.11 uses Direct Sequence Spread Spectrum (DSSS) and Frequency Hopping Spread Spectrum (FHSS), IEEE 802.16 is using Orthogonal Frequency Division Multiple Access (OFDM) and Scalable OFDM access (SOFDMA), while WMN uses OFDM and Ultra wide band (UWB) mechanisms for radio transmission. None of the mechanism is capable enough to handle the jamming attack on these broadband wireless networks.

b) Distributed Flooding DoS

A distributed flooding DoS attack is a huge challenge for all the wireless broadband networks, as this attack can bring down an entire network or consume the network bandwidth to a great extent. This kind of attack is launched by first compromising large number of innocent nodes in the wireless network termed as Zombies, which are programmed by highly skilled programmer. These zombies send data to selected attack targets such that the aggregate traffic congests the network. In most of the cases, the DDoS is impossible to prevent and it has the ability to flood and overflow the network. In IEEE 802.11 the target of distributed flooding would be Access Point (AP), in WMN the target is wireless mesh router while in IEEE 802.16 it is base station.

c) Rogue and selfish backbone devices

The attacker can seriously disrupt the broadband wireless networks by compromising the core network devices. In WMN and IEEE 802.11, a selfish mesh router or selfish AP can degrade the network performance either causing congestion or unavailability. IEEE 802.16, a rogue BS is an attacker station which is used to confuse the mobile stations of the network; as such kind of BS seems and acts like a legitimate BS. Mesh routers or APs are compromised by the attackers using sniffers. A sniffer is an application which is used for passive traffic analysis attack to analyze the network traffic. In IEEE 802.16, the BS is compromised by reprogramming a device with the hardware address of another legitimate device with hardware address can be detected by intercepting the management messages of IEEE 802.1 using sniffers. The same mechanism can be applied on mesh routers and APs to compromise using hardware address of another network device.

Authorization flooding on backbone devices WMN and IEEE 802.11 nodes use Probe request frames to discover a wireless network, if a wireless network exist then the AP respond with Probe response frame. The clients select that AP which provides the strongest signal to it. Here the attacker can spoof a flood of probe request frames presenting a lot of nodes searching for wireless network, can seriously overload the AP or wireless mesh router. If the load exceeds the threshold value will cause the AP or wireless mesh router to stop responding and may create service unavailability. In IEEE 802.16 the client stations use certificate to authenticate and register with the BS. The client station can send a bulk of registration requests to the BS may result in DoS.

d) Node deprivation attack

In node deprivation attack, the attackers target a single node and isolate it from taking part in the normal network operations. In WMN and IEEE 802.11, the nodes first authenticate itself with the mesh router or AP, and needs to de-authenticate it if the node has no more desire to use the network resources. The attacker can spoof the de-authentication message on behalf of the target node so that to stop it from using the network resources. The same vulnerability exist in IEEE 802.16, where the adversary eavesdrop the authentication message exchange between the node and the BS, and then replays this message many times to BS, creating DoS for the target node.

VI. Results of Dos Attacks and Possible Countermeasures

The results of different DoS attacks on broadband wireless networks vary with the nature and type of DoS attack.

- DoS attack is of low intensity, if launched against a single node either to exhaust its battery or to isolate it from the network Soperations.
- DoS attack is of high intensity if it is launched to make services unavailable for a target area in wireless broadband networks. Selfish mesh router attack in WMN and rogue BS attack is used for this purpose.
- Dos attack will be of highest intensity if it is launched to cripple down the entire broadband wireless network by distributive flooding.

Distributed flooding is normally used for this purpose to exhaust the bandwidth of the network or to overflow the resources of the gateways. DoS in any form against any network is regarded as a severe attack. Some possible countermeasure needs to be investigated to overcome to some extent against DoS and related issues in broadband networks.

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Message 1. SS → BS : Cert (SS. Manufacturer)
Message 2. SS → BS : T_S | Cert (SS) | Capabilities | SAID | SIG_{SS} (2)
Message 3. BS → SS : T_S | T_B | KU_{SS} (AK) | Lifetime | SeqNo | SAIDList | Cert (BS) | SIG_{BS} (3)

'Cert' stands for the X.509 certificates used. 'KUss (AK)' is the Authentication Key encrypted by SSs public key. Ts and Tb are timestamps of respectively the SS and BS. SeqNo and Lifetime are a sequence number and lifetime for the AK. SIGss and SIGbs are signatures for respectively the SS and BS. The SAID List defines the security associations ID´s to be used for communication. By adding the timestamps and signatures, freshness can be guaranteed for both messages. This way both SS and BS know that the message is fresh and not intercepted and replayed. The key management protocol (see figure 5) is also vulnerable for these attacks. Both the message from BS to SS and vice versa can be replayed to cause DoS or other unwanted behaviour.

HMAC stands for Hash Message Authentication Code, is a type of message authentication code (MAC) calculated using a cryptographic hash function in combination with a secret key. As with any MAC, it may be used to simultaneously verify both the data integrity and the authenticity of a message. What happens is that SS requests (or BS forces him to, using message 1) a new TEK in message 2. HMAC (1) can be used by SS to detect forgery attacks. HMAC (2) assures BS that the message is authenticate. HMAC (3) assures SS that message 3 is from BS and has not been modified.

Message 1. BS → SS: SeqNo | SAID | HMAC (1)
Message 2. SS → BS: SeqNo | SAID | HMAC (2)
Message 3. BS → SS: SeqNo | SAID | OldTEK | NewTEK | HMAC (3)

Because message 1 is optional, Tb2 will be set to 0 in message 2 by SS when it initiates re-keying. Tb2 in message 3 is generated by BS in responding to SSs request to assure SS the freshness and aliveness. When BS starts the rekeying, TB2 is generated in message 1 by BS and SS should include it in message 2 to assure BS the freshness and aliveness, but BS can omit it in message 3 by setting it to 0.

Message 1. BS → SS: T_{B2} | SeqNo | SAID | HMAC (1)
Message 2. SS → BS: T_{B2} | T_{S2} | SeqNo | SAID | HMAC (2)
Message 3. BS → SS: T_{S2} | T_{B2} | SeqNo | SAID | OldTEK | NewTEK | HMAC (3)

VII. Analysis

We will seem, per problem, at all answers by means of the principles stated over. For every explanation there is a table showing how they score on each criterion. A '+' means it scores well on that criterion, a '+/-' that it is doubtable and a '–' means a bad score. A '?' means no information was available for that criterion, for example no performance information because no simulations were ran.

a) DoS/Reply attack

[XMH06] depicts good quality development for authentication and authorization beside rerun assaults. Adding together the timestamp and signatures needs a sensible alteration to the normal. No data is obtainable concerning presentation but our anticipation would be a minute plunge in presentation. Even though the answer is deconcentrated, the argument in communication dimension in not radically. Yet, owing to the forward of timestamps and signatures, measurability might be exaggerated. [9]

VIII. Conclusion

From the above analysis, we are able to consider different issues pertaining to security aspect of broadband technology. When discussing the security of wireless technologies, there are several possible Perspectives. Different authentication, access control and encryption technologies all fall under the umbrella of security. Although relevant and important building blocks for overall security, these are not the focus of this paper. Instead, it will explore the problems at the implementation level of the current wireless access technologies and their Real world implications. As future technology of broadband is wireless communication, in that WIMAX plays a major role. In other way, in this research paper we would be discussing issues of security feature of WiMax and analyse one of the security features to work on it.

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Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 5 Version 1.0 April 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

A Compact Microstrip Patch Antenna for Wireless Communication

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Abstract - A single feed compact square microstrip antenna is proposed in this paper. Two L slits are introduced on the right edge of the patch to study the effect of the slit on radiation behavior with respect to a conventional microstrip patch. An extensive analysis of the return loss, radiation pattern and efficiency of the proposed antenna is shown in this paper. For the optimize value of the slit parameters antenna resonant frequencies are obtained at 2.16, 2.68,3.22&4.37 GHz with corresponding bandwidth 11.02 MHz, 13.07 MHz, 35.86 MHz , 48.56 MHz and return loss of about -23.4,-15.2,-30.6&-20.3 dB respectively. For the lowest esonant frequency (2.16 GHz) the size of the antenna has been reduced by 71.14 % when compared to aconventional rectangular microstrip patch. Thecharacteristics of the designed structure are nvestigated by using MoM based electromagnetic solver, IE3D. The simple configuration, low profile nature, reduced size and quad band characteristics of the proposed antenna makes it suitable to operate in the frequency ranges of 2.165-2.176, 2.673-2.686, 3.208-3.244 and 4.343-4.392 GHz.

Keywords : *Compact, patch antenna, slit, Quad band.*

GJRE- F Classification : *FOR Code: 0906*

A COMPACT MICROSTRIP PATCH ANTENNA FORWIRELESS COMMUNICATION

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A Compact Microstrip Patch Antenna for Wireless Communication

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Abstract- A single feed compact square microstrip antenna is proposed in this paper. Two L slits are introduced on the right edge of the patch to study the effect of the slit on radiation behavior with respect to a conventional microstrip patch. An extensive analysis of the return loss, radiation pattern and efficiency of the proposed antenna is shown in this paper. For the optimize value of the slit parameters antenna resonant frequencies are obtained at 2.16, 2.68,3.22&4.37 GHz with corresponding bandwidth 11.02 MHz, 13.07 MHz, 35.86 MHz , 48.56 MHz and return loss of about -23.4,-15.2,-30.6&-20.3 dB respectively. For the lowest esonant frequency (2.16 GHz) the size of the antenna has been reduced by 71.14 % when compared to aconventional rectangular microstrip patch. Thecharacteristics of the designed structure are nvestigated by using MoM based electromagnetic solver, IE3D. The simple configuration, low profile nature, reduced size and quad band characteristics of the proposed antenna makes it suitable to operate in the frequency ranges of 2.165-2.176, 2.673-2.686, 3.208-3.244 and 4.343-4.392 GHz.

Keywords : Compact, patch antenna, slit, Quad band.

I. Introduction

In recent years compact antenna with multiband characteristics is topic of interest for research work for application in wireless Communication system. One of the techniques to design a compact microstrip antenna [MSA] is cutting slots or slits on the radiating patch to increase the length of the patch of the surface current. Some articles on the design of compact MSA were studied by the author [1-4].MSAs are used in a broad range of applications from communication systems to biomedical systems, primarily due to several attractive properties such as light weight, low profile, low production cost, conformability, reproducibility, reliability, and ease in fabrication and integration with solid statedevices. The work to be presented in this paper is also a compact microstrip antenna by cutting two L slits on the right side of the patch [5-7]. Our aim is to reduce the size of the antenna as well as increase the operating bandwidth. The proposed antenna (substrate with εr=4.4) presents a size reduction of 71.14% when compared to a conventional square microstrip patch with a maximum bandwidth of 48.56 MHz. The simulation has been carried out by IE3D software which uses the MOM method [8]. Due to the Small size, low cost and low weight this antenna is a good candidate for the application of EMPS and WiMax technology.

II. Antenna Structure

The geometry of the square patch is shown in Figure1 which is a 20 mm x 20 mm. The antenna is fabricated on a substrate of FR4 epoxy with dielectric constant (εr) =4.4 and substrate height (h) =1.6 mm. Co-axial probe feed of radius 0.5 mm.

Fig. 1: Antenna 1 Configuration

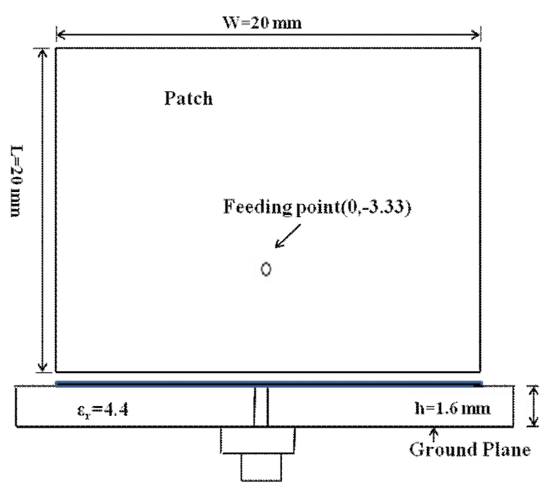

Fig. 2 : Antenna 2 Configuration

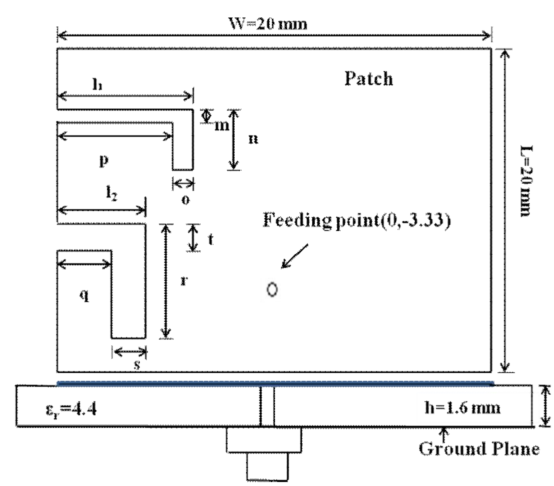

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FIGURE 2 SHOWS the configuration of antenna 2 which is designed with a similar substrate. The antenna is also a 20mm x 20 mm square patch. The location of coaxial probe-feed (radius=0.5 mm) is shown in figure 2.

III. Simulated Results

In this section, various parametric analysis of theproposed antenna are carried out and presented. Several slit parameters have been investigated toimprove bandwidth, gain and return loss performance of the antenna. Optimal parameter values of the two L slits are listed in Table 1and 2.

Table 1:

Parameters	p	m	n	o	l_1
Values(mm)	8.95	.5	5.2	1.1	10.05

Table 2 :

Parameters	q	r	s	t	l_2
Values(mm)	5.75	6.9	2	1	7.75

The simulated return loss of the conventional antenna (antenna 1) and the proposed antenna (antenna 2) are shown in Fig. 3 and fig 4 respectively. MHz respectively. In conventional antenna return loss found of about - 17.77 dB at 3.42 GHz and corresponding bandwidth is 50.54 MHz. Due to the presence of slot at the edge of the patch of antenna 2 multi frequency operation is obtained with large values of frequency ratio. For antenna 2 return losses -23.4 dB is obtained at 2.16 GHz, -15.2 dB at 2.68 GHz,-30.6 dB at 3.22GHZ and - 20.3 dB at 4.37 GHz and corresponding 10 dB bandwidth is 11.02 MHz, 13.07 MHz, 35.86 MHz and 48.56 MHz respectively.

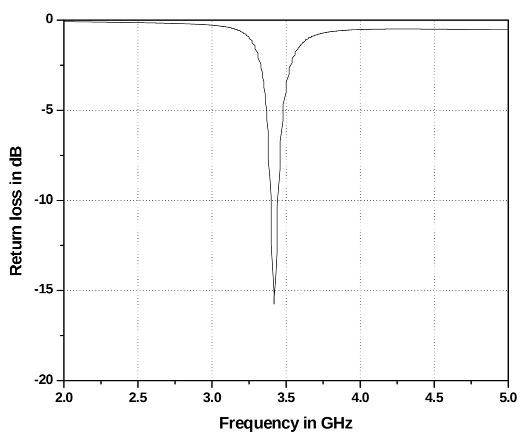


Fig. 3: Simulated return loss of the antenna1

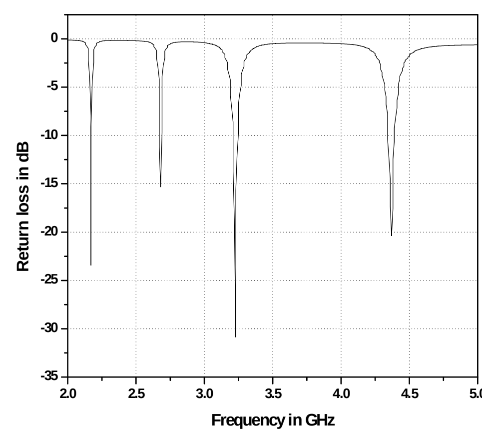
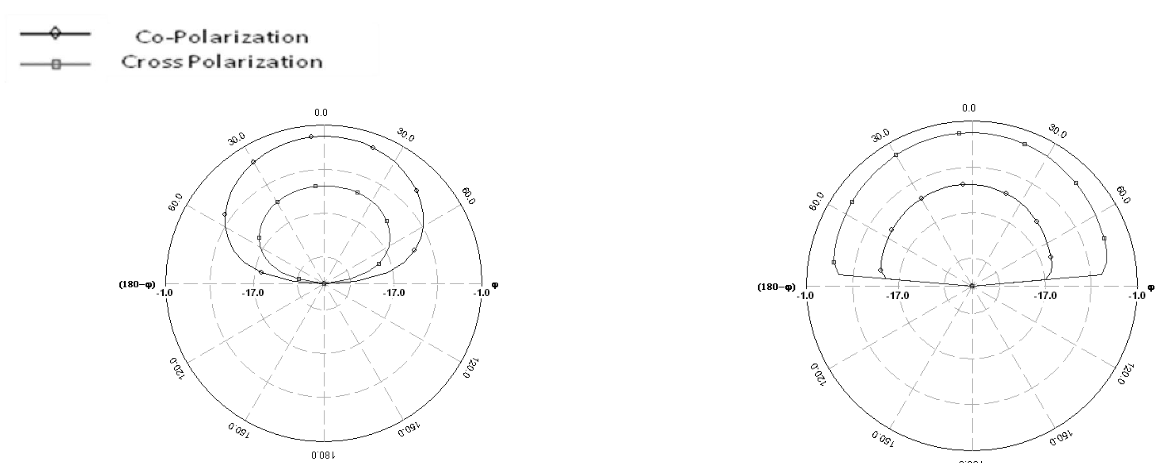


Fig. 4: Simulated return loss of the antenna2

The simulated E plane and H plane radiation patterns for antenna 2 are shown in Figure 5-8.



(a) E-field pattern

(b) H-field pattern

Fig. 5: Simulated normalize radiation pattern at 2.16 GHz

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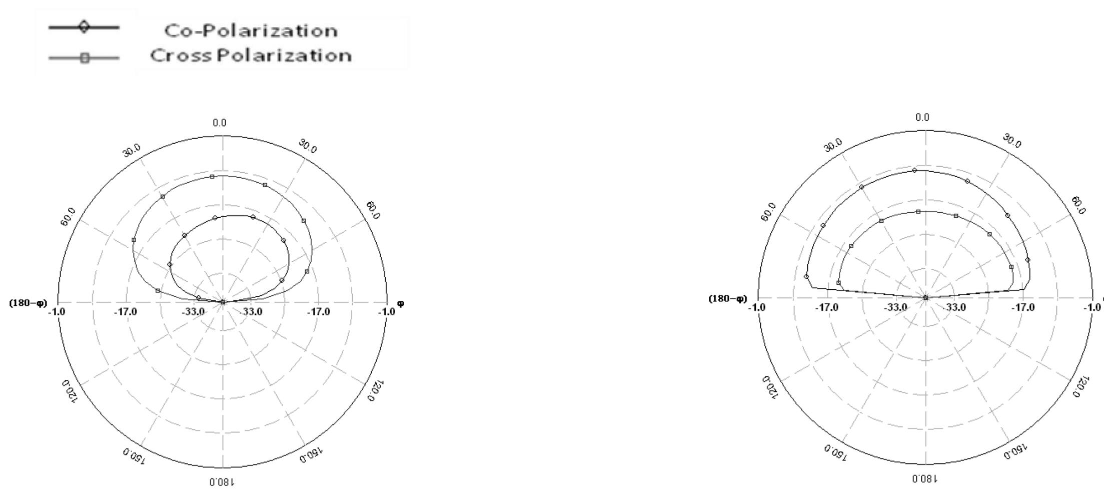
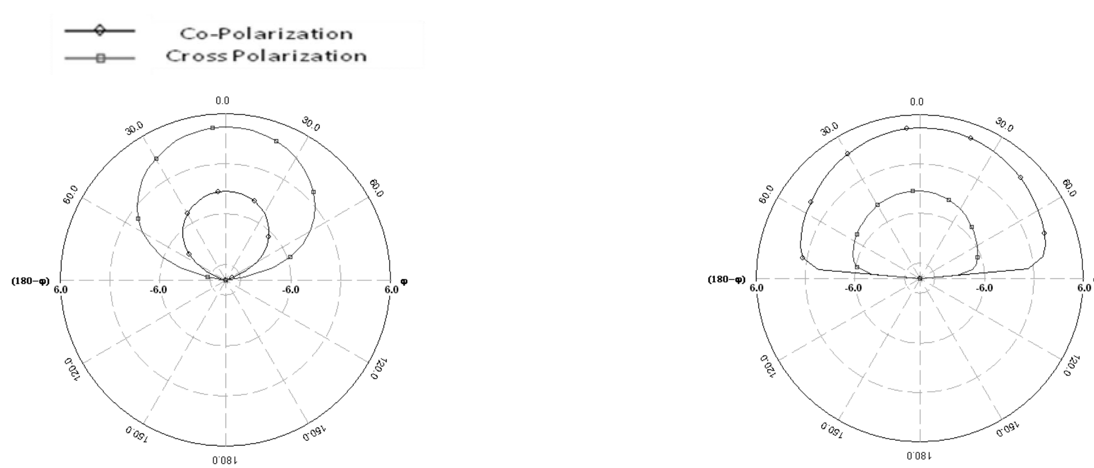


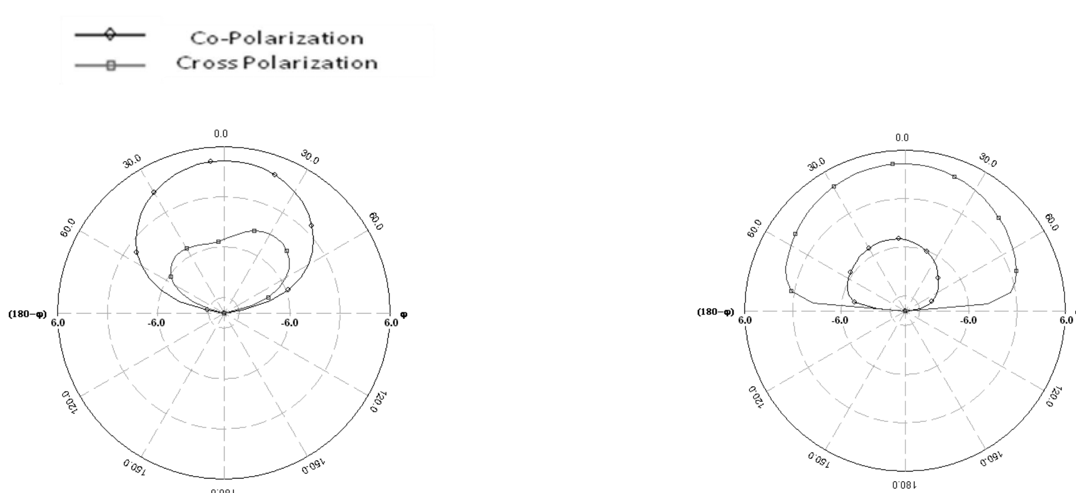
(a) E-field pattern (b) H-field pattern

Fig. 6: Simulated radiation pattern at 2.68 GHz



(a) E-field pattern (b) H-field pattern

Fig. 7: Simulated normalize radiation pattern at 3.22 GHz



(a) E-field pattern (b) H-field pattern

Fig. 8: Simulated normalize radiation pattern at 4.37 GHz

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IV. Experimental Results

Comparisons between the measured return loss with the simulated ones are shown in Fig.9 and 10. All the easurements are carried out using Vector Network Analyzer (VNA) Agilent N5 230A.The agreement between the simulated and measured data is reasonably good. The discrepancy between the measured and simulated results is due to the effect of improper soldering of SMA connector or fabrication tolerance.

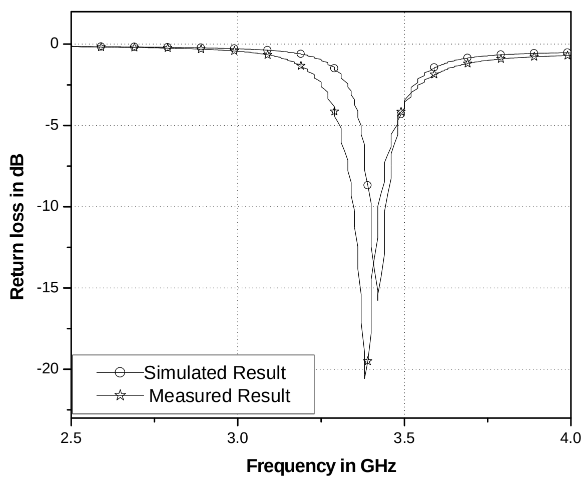

Fig. 9 : Comparison between measured and simulated return losses for antenna1

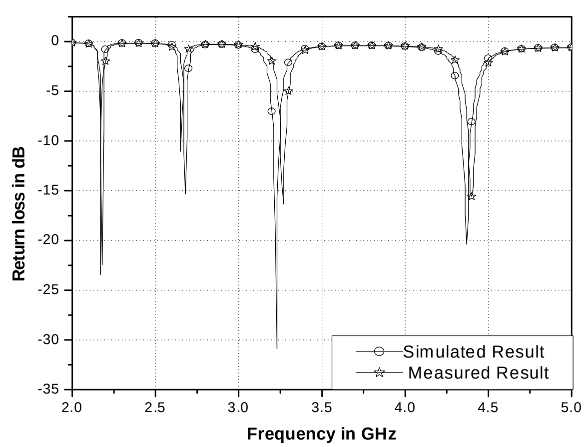

Fig.10: Comparison between measured and simulated return losses for antenna 2

V. Conclusion

A single feed single layer two L slits microstrip antenna has been proposed in this paper. It is shown that the proposed antenna can operate in four frequency bands. The slits reduced the size of the antenna by 71.14 % for the resonant frequency 2.16GHz and increase the bandwidth up to 48.56 MHz with a return loss of -30.6 dB and 3 dB beamwidth of 166.82 deg. An optimization between size reduction with multiband operation is maintained in this work.

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Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 5 Version 1.0 April 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Modeling of Dc Link Capacitor Voltage Balance in 3-Level Inverter Using Space Vector Modulation Technique

By Mr. Srinivas Dasam & Dr. BV Sankerram

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Abstract - A new simplified space vector PWM method for a three-level inverter is proposed in this paper. The three level inverter has a large number of switching states compared to a two-level inverter. In the proposed scheme, three-level space vector PWM inverter is easily implemented than as conventional two-level space vector PWM inverter. This paper presents a novel DC link balancing scheme for a back-to-back system with three-level diode clamped topologies. The proposed algorithm is improvement of the variable switching frequency control strategy formerly introduced with the threelevel back-to-back system and it relays on measurement of adjacent capacitor voltages which provide information about the potential variation in consecutive nodes of the three-level DC link network, Therefore, the proposed method can also be applied to multilevel inverters. In this work, a three-level inverter using space vector modulation strategy has been modeled and simulated.

Keywords : *Multi level Inverter, voltage balance, switching states, Dc-link, SVM, power factor.*

GJRE- F Classification : *FOR Code: 0906*

MODELING OF DC LINK CAPACITOR VOLTAGE BALANCE IN 3-LEVEL INVERTER USING SPACE VECTOR MODULATION TECHNIQUE

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Modeling of Dc Link Capacitor Voltage Balance in 3-Level Inverter Using Space Vector Modulation Technique

Mr. Srinivas Dasam [α] & Dr. BV Sankerram [σ]

Abstract - A new simplified space vector PWM method for a three-level inverter is proposed in this paper. The three level inverter has a large number of switching states compared to a two-level inverter. In the proposed scheme, three-level space vector PWM inverter is easily implemented than as conventional two-level space vector PWM inverter. This paper presents a novel DC link balancing scheme for a back-to-back system with three-level diode clamped topologies. The proposed algorithm is improvement of the variable switching frequency control strategy formerly introduced with the three-level back-to-back system and it relays on measurement of adjacent capacitor voltages which provide information about the potential variation in consecutive nodes of the three-level DC link network, Therefore, the proposed method can also be applied to multilevel inverters. In this work, a three-level inverter using space vector modulation strategy has been modeled and simulated.

Keywords : Multi level Inverter, voltage balance, switching states, Dc-link, SVM, power factor

I. Introduction

Recently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Hence, different circuit configurations namely multilevel inverters have became popular and considerable interest by researcher are given on them [1-2]. The output voltage waveforms in multilevel inverters can be generated at low switching frequencies with high efficiency and low distortion. In recent years, beside multilevel inverters various pulse width modulation (PWM) techniques have been also developed. Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently. This technique results in higher magnitude of fundamental output voltage available as compared to sinusoidal PWM. However, SVPWM algorithm used in three-level inverters is more complex because of large number of inverter switching states. One of the advantages of multilevel inverters is that the voltage stress on each switching device is reduced. In addition, multilevel waveforms feature have less harmonic content compared to two level waveforms operating at the same switching frequency. In this paper, modeling and simulation of a multilevel inverter using cascaded inverters with separated DC sources have been performed with R-L load using Simulink/ MATLAB package program. In multilevel inverters, it is easy to reach high voltage levels in high power applications with lower harmonic distortion and switching frequency, which is very difficult to get this performance with conventional two level inverters. Minimum level number of a multilevel inverter is three and three-level inverter structure is chosen in this work.

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a) *multilevel concept*

This paragraph has the aim to introduce to the general principle of multilevel behavior. Considering Figure 1.), the voltage output of a 3-level inverter leg can assume three values: 0 , E or 2E . In Figure 1.1c) a generalized n-level inverter leg is presented. Even in this circuit, the semiconductor switches have been substituted with an ideal switch which can provide n different voltage levels to the output. In this short explanation some simplifications have been introduced. In particular, it is considered that the DC voltage sources have the same value and are series connected. In practice there are no such limits, then the voltage levels can be different. This introduces a further possibility which can be useful in multiphase inverters, as it will be shown in the following. A three-phase inverter composed by n-level legs will be considered for the analysis. Obviously the number of phase-to-neutral voltage output levels is n. The number k of the line-to-line voltage levels is given by

$$k = 2n - 1 \tag{1}$$

Considering a star connected load, the number p of phase voltage levels is given by

$$p = 2k - 1 \tag{2}$$

For example, considering a 5-level inverter leg, it is possible to obtain 9 line-to-line voltage level (3 negative levels, 3 positive levels and 0) and 17 phase voltage levels. Higher is the number of levels better is the quality of output voltage which is generated by a greater number of steps with a better approximation of a sinusoidal wave. So, increasing the number of levels gives a benefit to the harmonic distortion of the generated voltage, but a more complex control system is required, with the respect to the 3-level inverter.

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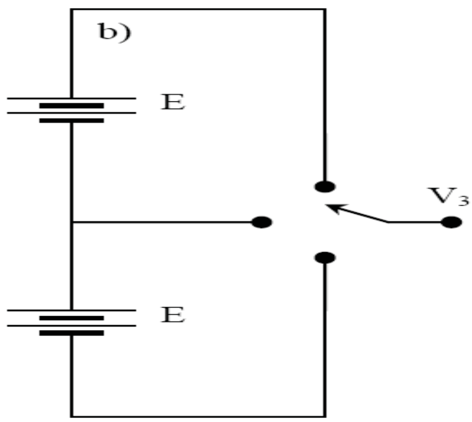

Fig.1 : 3-level diode-clamped leg of multilevel inverter

Diode-clamped Operating principle: In Figure 1 a 3-level diode-clamped leg is shown it is easy to extend the scheme to a generic n-level configuration. The DC bus voltage is split in two and four equal steps respectively by capacitor banks. In this way, no extra DC sources are needed with respect to the standard 2-level inverter. The voltage between two switches is clamped through the diodes in the middle of the structure, called *clamping diodes*. Anyway, to better understand how a diode-clamped works, it is preferred to use series connected diodes; in this way, the reverse voltage drop of all the diodes is the same and is equal to the voltage fixed by a capacitor. For a generic n-level diode-clamped the diode reverse voltage is given by (3)

$$Vr = E/n\text{-}1 \qquad (3)$$

In 3-level diode-clamped it is 2

Vr = E/2 this voltage drop is also the reverse voltage each switch has to block. Now it is clear that increasing the levels means a reduction of the stress over the components, considering the same DC bus voltage. Unfortunately, higher is the number of levels higher is the number of components. Increasing of one level involve the use of one capacitor, two switches and a lot of diodes more. In fact the number of clamping diodes used in a diode-clamped is related to the number of level by the following expression: N_{Diodes} = (n 1) (n 2)

Focusing the attention to the 3-level leg, it is possible to find the relationship between the state of the switches and the output voltage AO V. Before all consideration, a right switches configuration must avoid every kind of shortcut. So, it is simple to understand that all the switches cannot be simultaneously turned on.

Table1 : The relationship between the state of the switches and the output voltage

Switches state				
T_1	T_2	T^1_1	T^1_2	V_{AO}
1	1	0	0	E
0	1	1	0	E/2
0	0	1	1	0
1	0	0	1	Undefined

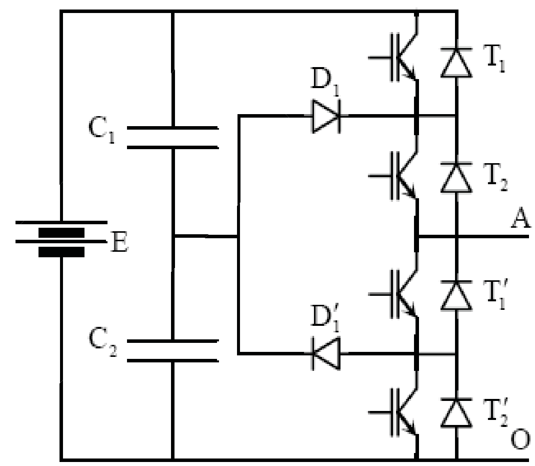

Fig2 : Three-level Capacitor-Clamped Multilevel inverter

There are also other dangerous configurations, but they can be avoided switching 1 T and 1 T′ in a complementary way. The same has to happen for 2 T and 2 T′. Considering these conditions there are only four possible configurations a 3-level diode-clamped leg can assume and they are shown in Table 1 with the agreement to identify switches on-state with 1 and off state with 0. Not all the four configuration leads to a proper leg output voltage, because when 1 T in on and 2 T is off there is no defined path for the load current because whether 2 T or 1 T′ are not conducting, so the current flows throughout the free-willing diodes and the output voltage de pendson it. As it is possible to see from Table1. There are no intra-phase redundant states in 3-level diode-clamped.

II. Analysis of Space Vector PWM Method for Three-Level Inverters

A schematic drawing of a multilevel inverter using cascaded inverters with separated DC sources is shown in Fig.2. Three-phase output voltage waveforms are generated by various switching combination of the switches in each H-bridge converter resulting three levels at the output phase voltage waveforms as

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+E/2,0,-E/2. The switching states of the inverter are summarized in Table2 where x represents the output phases, a, b and c [4].

Table 2 : The switching states of the inverter

V_{x0}	S_{X1}	S_{X2}	S_{X1}'	S_{X2}'
$V_{dc}/2$	1	0	0	1
0	1	1	0	0
0	0	1	0	1
$-V_{dc}/2$	0	1	1	0

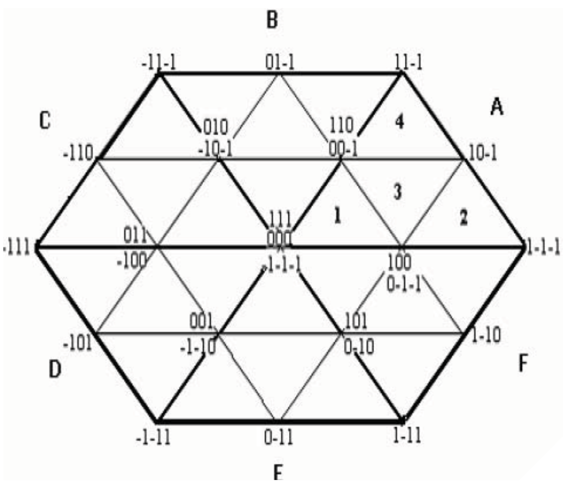

Fig.3 : Schematic diagram of proposed SVPWM

The principle of SVPWM method is that the command voltage vector is approximately calculated by using three adjacent vectors. The duration of each voltage vectors obtained by vector calculations; where V1, V2, and V3 are vectors that define the triangle region in which V* is located. T1, T2 and T3 are the corresponding vector durations and Ts is the sampling time. In a three-level inverter similar to a two-level inverter, each space vector diagram is divided into 6 sectors. For simplicity here only the switching patterns for Sector A will be defined so that calculation technique for the other sectors will be similar. Sector A is divided into 4 regions as shown in Fig.3 where all the possible switching states for each region are given as well. SVPWM for three-level inverters can be implemented by considering the following steps;

1. Determine the sector,
2. Determine the region in the sector,
3. Calculate the switching times, Ta, Tb, Tc
4. Find the switching states.

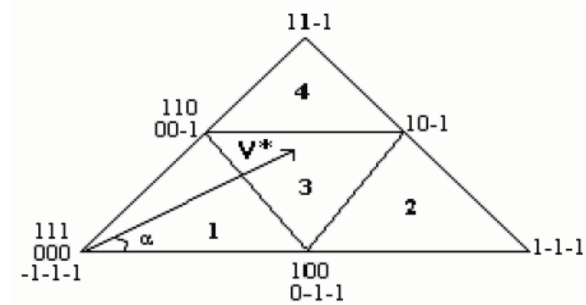

Fig3.(a) : Schematic diagram of proposed SVPWM

a) Determining the sector

α is calculated and then the sector, in which the command vector V* is located, is determined as;

If α is between $0° \le \alpha < 60°$, then V* will be in Sector A,

If α is between $60° \le \alpha < 120°$, then V* will be in Sector B,

If α is between $120° \le \alpha < 180°$, then V* will be in Sector C,

If α is between $180° \le \alpha < 240°$, then V* will be Sector D,

If α is between $240° \le \alpha < 300°$, then V* will be Sector E,

If α is between $300° \le \alpha < 360°$, then V* will be Sector F.

b) Determining the region in the sector: For that

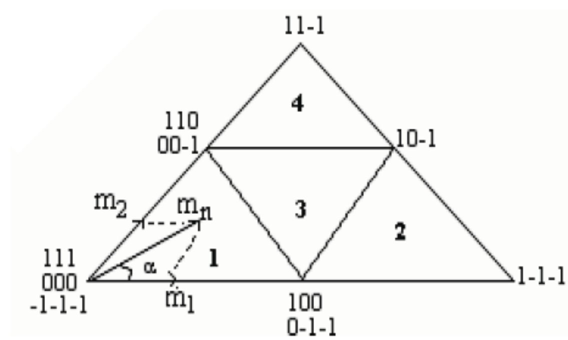

Fig.3(b) : Schematic diagram of proposed SVPWM

From Fig.4 (b) m2 and m1 can be calculated as;

$$a = m_2 = \frac{b}{\sin(\pi/3)} = \frac{2}{\sqrt{3}} b = \frac{2}{\sqrt{3}} . m_n . \sin\alpha$$

$$m_1 = m_n . \cos\alpha - \left(\frac{2}{\sqrt{3}} . m_n . \sin\alpha \right) \cos(\pi/3)$$

$$m_1 = m_n (\cos\alpha - \frac{\sin\alpha}{\sqrt{3}})$$

And then,

If m1, m2 and $(m1+m2) < 0.5$, then V* is in Region 1, If $m1 > 0.5$, then V* is in Region 2,

If $m2 > 0.5$, then V* is in Region 3,

If m1 and $m2 < 0.5$ and $(m1+m2) > 0.5$, then V* is in Region 4.

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c) Calculating the switching times, Ta, Tb, Tc

Ta, Tb, Tc switching times for Sector A is given in Table.3.

Table 3 : Switching times for Sector A.

	Region I	Region II
T_a	$1.1*m*T_s*\sin((\pi/3)-\alpha)$	$T_s(1-1.1*m*\sin(\alpha+\pi/3))$
T_b	$T_s/2(1-(2*1.1*\sin(\alpha+\pi/3))$	$1.1*T_s*m*\sin\alpha$
T_c	$1.1*T_s*\sin\alpha$	$T_s/2((2*1.1*m*\sin(\pi/3-\alpha))-1)$
	Region III	**Region IV**
T_a	$T_s/2(1-2*1.1*m*\sin\alpha)$	$T_s/2(2*1.1*m*\sin(\alpha)-1)$
T_b	$T_s/2(2*1.1*m*\sin(\pi/3+\alpha)-1)$	$1.1*m*T_s*\sin((\pi/3)-\alpha)$
T_c	$T_s/2(1+2*1.1*m*\sin(\alpha-\pi/3))$	$T_s(1-(1.1*m*\sin(\alpha+\pi/3))$

d) Finding the switching states

By considering the switching transition of only one device at any time; the switching orders given below are obtained for each region located in Sector A if all switching states in each region are used. Therefore, switching signals for Sector A are;

Region 1:-1-1-1, 0-1-1, 00-1, 000, 100, 110, 111

Region 2: 0-1-1, 1-1-1, 10-1, 100

Region 3: 0-1-1, 11-1, 10-1, 100, 110

Region 4: 00-1, 10-1, 11-1, 110

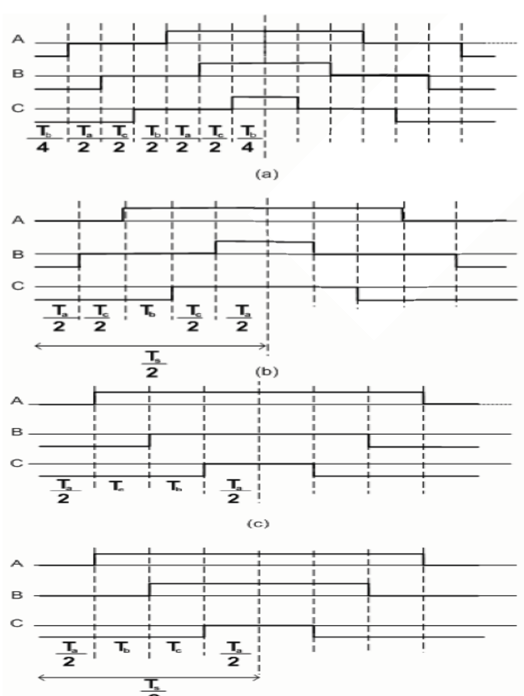

Fig.4 : Switching Signals of Sector A: (a) Region.1, (b) Region 2, (c) Region 3, (d) Region 4

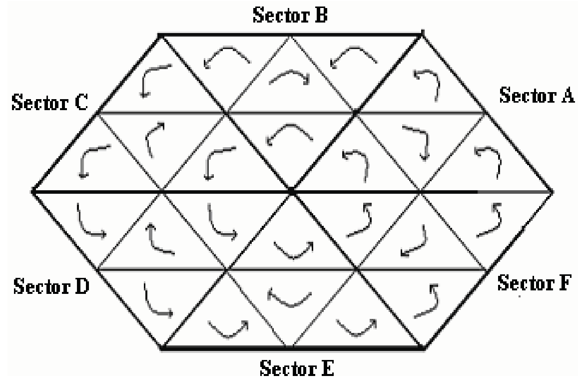

Fig.5 : switching sequence for three-level SVPWM inverter

III. Capacitor Balancing for Dicde Clamped three Level Diode

Voltage unbalance problem appears as the result of non-uniform switching of the semi-conductors from bottom and upper inverter's groups. Potentials difference on capacitors produce current in zero -point of the inverter (point between condensers of the bottom and upper group), which from one side causes supercharging one of the capacitances and from second unloading the other one (this phenomena takes place, when inverter's zero - point is separated from source neutral line). During following cycles of modulation, voltages on capacitors attain different levels in result of that compensated current is not shaped correctly. One from methods of assurance of stabilization is interference in switching strategy of the semiconductors [5]. One can reach this adding suitable constant component to reference current for every from three phases separately (this does not cause changes on effective exit voltages and currents of the inverter). This suitable constant component one can receive from measured voltages difference UC1 and UC2 on each capacitor. Second method of voltage stabilization is addition the same constant component to two triangular courses (Fig.3.). This gives finally the same effect but permits to obtain better formation of compensating currents.

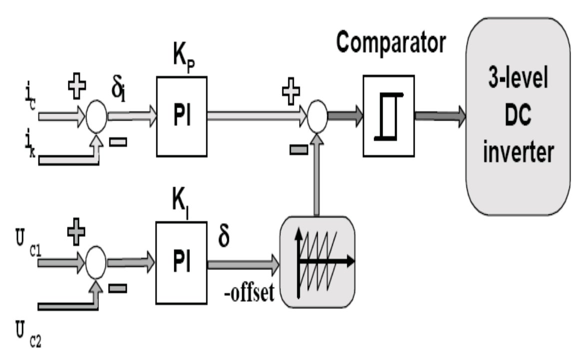

Fig.6 : Balancing circuit for 3- levels Diode clamped

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IV. Results & Discussion

Simulation of different modulation scheme for Multilevel Inverter.

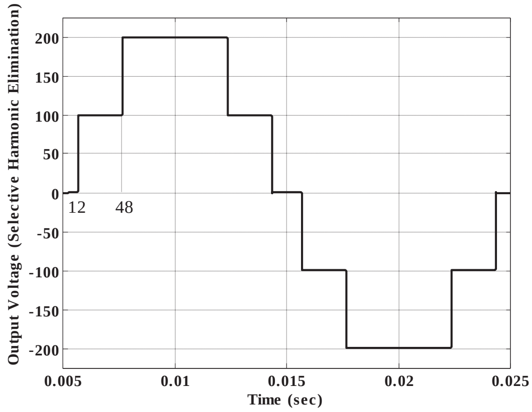

Fig. 7 : MATLAB Simulation for Selective harmonic elimination method

Different modulation scheme for multilevel inverter are explain in Chapter 2. Of these different schemes a) Selective Harmonic elimination b) SPWM method are simulated.

Fig7 gives simulation result for selective harmonic elimination method where for eliminating 3rd and 5th harmonic, switching angles are selected as $\alpha_3 = 12^o$ and $\alpha_5 = 48^o$ as discussed in 2.4 section. FFT for this method is given Fig. 8

In SPWM method of modulation for multilevel inverter numbers of carriers are used. Arrangements of these carriers come with different variants as explain in 8 Fig. 9 gives (a) carrier arrangement, (b) output voltage and (c) FFT for PH disposition (All carriers are in phase) SPWM method for 5-level inverter. (f_c = 1050 Hz, f_m = 50 Hz)

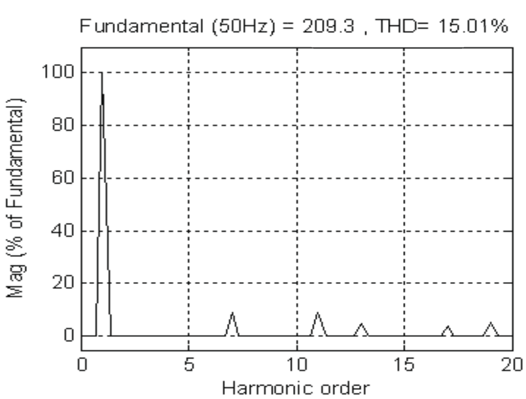

Fig.8 : MATLAB Simulation for FFT method

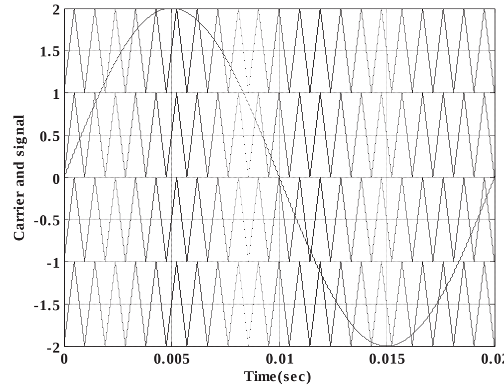

Fig.9(a)

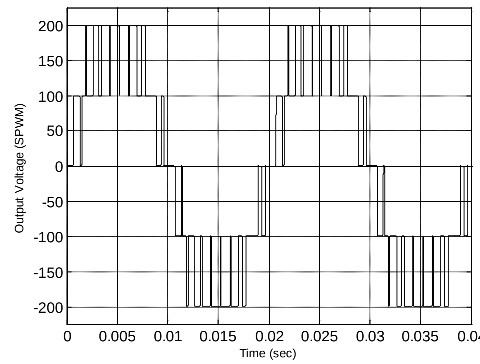

Fig.9(b)

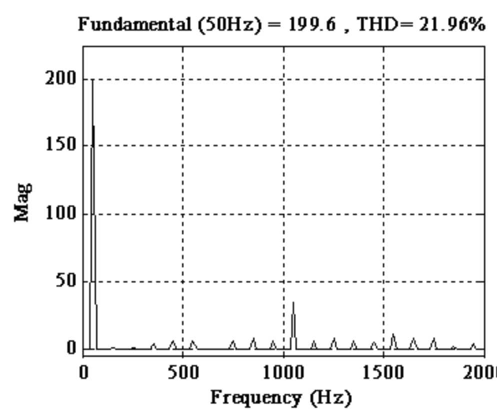

Fig9(c)

Fig. 9 : gives (a) carrier arrangement, (b) output voltage and (c) FFT for PO disposition (All carries above the zero reference are in phase, but in opposition with those below) SPWM method for 5-level inverter.(f_c = 1050 Hz, f_m = 50 Hz)

V. Conclusion

In this work all main topologies of multilevel inverter are explained. For controlling multilevel inverter different modulation scheme are used. Of these different modulation schemes SPWM method has gained more interest in industrial application In this thesis work a new mathematical model based SPWM scheme is proposed

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which calculate exact instant of crossing of reference sine waveform with carrier signal and modify sampled value of reference signal based on this information to achieve performance same as that with natural SPWM. Results obtain from MATLAB simulations validate the proposed scheme which give better performance of proposed scheme over the other scheme on the basis of output phase delay and output THD. The proposed control algorithm used in the three level inverter can be easily applied to multilevel inverters. It has been shown that high quality waveforms at the output of the multilevel inverter can be obtained even with 1 kHz of low switching frequency.

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Global Journal of Researches in Engineering (F) Volume XII Issue V Version I April 2012

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Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 5 Version 1.0 April 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

A Novel on Coordinated Voltage Control Scheme for SEIG-Based Wind Park Utilizing Substation Statcom and ULTC Transformer

By S.Radha Krishna Reddy , V. Rafi , Dr.Jbv Subrahmanyam & S.Md.Mazhar Ul-Haq

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Abstract - This paper presents a coordinated voltage control scheme for improving the network voltage profile and for minimizing the steady-state loading of the STATCOM to effectively support the system during contingencies. The paper addresses implementation issues associated with primary voltage control and optimal tracking secondary voltage control for wind parks based on self-excited induction generators which comprise STATCOM and under-load tap changer (ULTC) substation transformers. The voltage controllers for the STATCOM and ULTC transformer are coordinated and ensure the voltage support.

Keywords : Communication time delay, optimal tracking secondary voltage control (OTSVC), primary voltage control (PVC), short circuit ratios (SCRs), STATCOM, transient stability margin, under-load tap changer (ULTC).

GJRE- F Classification : FOR Code: 0906,090602,100599

A NOVEL ON COORDINATED VOLTAGE CONTROL SCHEME FOR SEIG-BASED WIND PARK UTILIZING SUBSTATION STATCOM AND ULTC TRANSFORMER

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A Novel on Coordinated Voltage Control Scheme for SEIG-Based Wind Park Utilizing Substation Statcom and ULTC Transformer

S.Radha Krishna Reddy [α] , V. Rafi [σ], Dr.Jbv Subrahmanyam [ρ] & S.Md.Mazhar-Ul-Haq [ω]

Abstract - This paper presents a coordinated voltage control scheme for improving the network voltage profile and for minimizing the steady-state loading of the STATCOM to effectively support the system during contingencies. The paper addresses implementation issues associated with primary voltage control and optimal tracking secondary voltage control for wind parks based on self-excited induction generators which comprise STATCOM and under-load tap changer (ULTC) substation transformers. The voltage controllers for the STATCOM and ULTC transformer are coordinated and ensure the voltage support. In steady-state operation, the voltage is controlled by only stepping the tap changer when the voltage is outside the dead band region of the ULTC to minimize the number of taps changes. Thus, the STATCOM will be unloaded and ready to react with higher reactive power margin during contingencies. In the paper, the effects of the short circuit ratio of the interconnection and the inherent communication delay between the wind park and the remote bus on the performance of the controllers and the maximum critical clearing time of fault are considered. Simulation results are presented to demonstrate the performance of the controllers in steady-state and in response to system contingency situations.

Index Terms : Communication time delay, optimal tracking secondary voltage control (OTSVC), primary voltage control (PVC), short circuit ratios (SCRs), STATCOM, transient stability margin, under-load tap changer (ULTC).

Nomenclature

SEIG	*self-excited induction generator*
ULTC	*under-load tap changer*
LDC	*line drop compensation*
PVC	*primary voltage control*
MCCT	*maximum critical clearing time*
FRT	*fault ride through*
WAMS	*wide-area measurement system*
OTSVC	*optimal tracking secondary voltage Control*

I. Introduction

Voltage control is important for the integration of wind parks and their interconnections to achieve a required voltage response and fault ride through (FRT) capability according to the grid codes. The voltage control is divided into three hierarchical levels: primary, secondary, and tertiary control [1]–[4]. The large penetration of wind parks based on self-excited induction generator (SEIG) is often comprised of a central compensator, a STATCOM that controls the voltage by means of reactive power, and also under-load tap changing (ULTC) transformers are used to control the voltage. This makes the application of secondary voltage control schemes to wind parks an interesting approach to improve the operation of the transmission system. Hence, a strategy to perform secondary voltage control by a coordinated use of the ULTC and STATCOM for providing a better voltage support and a larger dynamic margin during system contingencies are needed. Coordinated control methods for ULTCs and compensator devices are proposed in [5].

The ULTC provides a slow voltage control and the tap changing causes transient responses in the power system. Thus, the objective of the coordinated control of the ULTCs and a compensating device is to minimize the number of unnecessary tap operations and to provide a better voltage profile. In [5] and [6], an artificial neural network is used in the coordinated control of the ULTC and STATCOM to minimize the number of tap changes and for increasing the reactive power capability margin of the STATCOM in system contingency situations. Among voltage regulating devices, the ULTC has a larger impact on the voltage profile since it controls the sending voltage. One of the major measures of the ULTC operation is the line drop compensation (LDC) method, which estimates and allows compensation for the line drop at varying load currents [7], [8]. The LDC method has been widely applied to the ULTC operation. This paper presents a new approach to a coordinated voltage control for the STATCOM and the ULTC transformer. Using this control the STATCOM will be unloaded and ready to react with a higher reactive power margin in case of system contingencies. The performance of primary voltage control (PVC) and optimal tracking secondary voltage control (OTSVC) with and without the new coordinated method used by the STATCOM and the ULTC are compared considering steady-state and dynamic measures such as voltage response, voltage recovery,

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the steady-state loading of the STATCOM, the voltage profile, and the maximum critical clearing time (MCCT) of fault as an indication of the transient stability margin. Subsequently, the influence of a communication time delay on the transient stability margin is evaluated in order to demonstrate the effectiveness of the coordinated OTSVC for improving the system voltage profile and the transient response.

II. SEIG Wind Park Model

The wind park model analyzed in this paper is shown in Fig. 1 and consists of 12*1.5-MW SEIG wind turbines compensated with a STATCOM. The wind turbines are connected to the medium voltage bus via a 0.575/25-kV transformer, and then connected to the 120-kV system at bus B120 through a25-MVA 25/120-kV ULTC transformer. The reactive power absorbed by the SEIG is partly compensated by capacitor banks connected to each wind turbine, the rest of the compensation

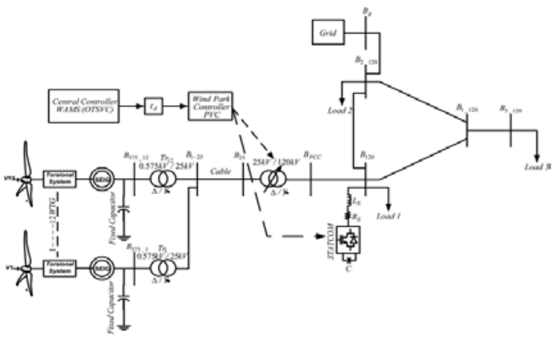

Fig. 1 : Layout of the wind park model.

to maintain the bus voltage close to 1 p.u. is provided by the centralized STATCOM rated at 12 MVAr with a 3% droop setting. The control consists of a local wind park control that communicates with the transmission system through a communication link, which is used to transmit data signals obtained from a wide-area measurement system (WAMS).

a) *Self Excited Induction Generator Model*

For the SEIG in Fig. 1, a dynamic model in the stationary - reference frame as described in [9] is used.

b) *Under Load Tap Changer Model*

The control scheme for the ULTC transformer is based on the tap-changing device and a motor drive to move the taps in a controlled sequence of steps with a constant time delay shorter than 10 s. The system performs secondary voltage control when the voltage exceeds the specified dead band within the specified time delay [1]. The discrete equations of the ULTC control system are as follows:

$$n(t+1)=n(t)-d*f(e(t);T(t)) \quad (1)$$

$$T(T+1)=g(e(t);T(t)) \quad (2)$$

$$F(e,T)=\{1 \text{ , IF } e>\varepsilon \text{ and } T\geq t=Td\} \quad (3)$$

$$e=V-Vref \quad (4)$$

where is the tap position of the ULTC, is the step size of the tap position, is the voltage error, is the time delay, is the controlled voltage, is the threshold of dead band, is the counter, and is the reference voltage. Equations (1)–(5) state that each tap position varies with step size of the tap position at time , when the voltage deviates from the specified dead band during the specified time delay.

c) *Statcom Model*

The STATCOM is used to generate or absorb reactive power by controlling the magnitude of the dc link and ac voltage while keeping the angle very small to allow active power flow to compensate solid state switching and coupling transformer losses. The active and reactive powers in the mathematical model of the STATCOM are described in [10].

1) Average Model of the STATCOM: For the simulations an average model of the STATCOM as shown in Fig. 2 is used as it will speed up the simulation time by factor of 20 compared to a more detailed model. In this average model, the switching converter in the detailed model is replaced with a controllable voltage source. The three phase output from a performed Park Transformation is used directly as input signals to the converter. In this way PWM, a detailed model of the VSC and third-harmonic injection is removed compared to a more detailed model, Decoupled current control of a STATCOM. which could have been set up. Further, the dc-link voltage control is in this model replaced with the STATCOM active power control.

The current is decoupled in two control loops, controlling the direct and the quadrature current, for controlling the active power and the reactive power exchange between the converter and the ac-system, respectively. The output of the current regulators are the voltage signals and , which are added to the feed forward signals of the Park Transformed three phase terminal voltages. To achieve higher performance, the voltage drops across the converter inductors are also added to the controlling voltage signals. PVC or OTSVC will be alternatively employed as the outer control loops of the STATCOM to determine the reference quadrature STATCOM current. The determined direct and quadrature-controlling voltages are finally transformed from the - reference frame to three phase voltages, which are used directly to control the controllable voltage sources.

III. System Voltage Control

a) *Wind Park Voltage Control and Communication Time Delay Modeling*

For the wind park central compensator (the STATCOM), a reactive current reference signal is generated using a voltage set point supplied by the remote supervisory control, for which the time delay is taken into account as shown in Fig. 1. Using PI-controllers, a 3% voltage droop is implemented. Parameters were selected using an off-line least square minimization method [16]. The impact of the communication delays are of great concern in WAMS, particularly when a large number of signals are combined to provide some type of control function. Communication links can be classified into wired communication (telephone lines, fiber optics, and power lines) or wireless (microwave, radio, and satellites). The communication delays vary based upon the kind of link. The local control PVC is not affected by the communication delays as it is normally less than 10 ms and often ignored in controller design and stability analysis of the power system [11]. The experimental research presented in [11] has characterized the time delays associated with different communication links. All communication delays are higher than 100ms, the satellite link showing the highest time delay. This delay can be higher than 700 ms when a large number of signals are to be routed and remote signals from different areas are waiting for synchronization [11], [12]. Much smaller delays have been reported for fiber-optics links, typically in the order of 38 ms for one way, while the time delay for using modems via microwave is over 80 ms.

b) Voltage Control Schemes

PVC is the basic approach for the voltage regulation of the high voltage bus to which the wind farm is connected. Besides the normal voltage control based on voltage and current measurements for enhancing the wind park performance, the STATCOM controller here is extended with auxiliary damping control loops, based on rotor speed deviation and active power variation measurements. The two loops are structured based on an analytical approach for synchronizing power and damping power. A lead–lag control structure is chosen for the two loops. A more detailed description of the damping control loops are given in [18]. Hence, in order to increase the system damping, it is necessary to add additional control blocks with adequate input signals.

i. *Primary Voltage Control*

There are two damping control loops specified based on the rotor speed deviation and the variation of active power in a specified time interval as shown in EL MOURSI *et al*.: COORDINATED VOLTAGE CONTROL SCHEME FOR SEIG-BASED WIND PARK 249 PVC algorithm comprising (a) PVC and (b) damping control signals. The damping power control loop signal should be included in phase with the rotor speed deviation . Therefore, different control algorithms can be synthesized depending on the desired type of friction. There are different possible functions for the friction that fulfill the following general condition:

Some of them are:

1) Linear friction:

2) Colombian friction:

3) High order polynomial friction:

4) Combination of the above. Fig. 4. Performance of the damping control loops.

250 IEEE TRANSACTIONS ON SUSTAINABLE ENERGY, VOL. 2, NO. 3, JULY 2011 Fig. 5. Coordinated OTSVC scheme for STATCOM and ULTC.

5) Similar structure to case (1)–(4), but with parameters adaptable in accordance with the evolution of the system variables. Once the injected friction function is selected, the expression of the control law is designed using (7) based on the control mode. The STATCOM is controlling the bus terminal voltage , thus the control law is (7) The damping loops utilize the integral time absolute error of the rotor speed and the active power. They are set by the following objective functions: The rotor speed deviation. The active power deviation in a specified time interval. The target is to minimize the objective functions in order to improve the system response. Therefore, adopting the parameters of the control loops should be tuned to achieve an appreciated system response. The damping control loops consist of a gain block, a signal washout block, and a two-stage phase compensation blocks. It is preferable that the additional control signal is local to avoid the impact of communication time delay. The damping signal is fed through a washout control block to avoid affecting the steady-state operation, and an additional lead–lag control block is used to improve the dynamic system response. The washout block performs as a high-pass filter which allows signals associated with oscillations to pass unchanged. The STATCOM with the damping control loops is tested while the system shown in Fig. 1 is subjected to three phase faults at PCC at s and cleared after 200 ms. The damping control loops demonstrate superior performance for damping system oscillation .

ii. *Optimal Tracking Secondary Voltage Control*

In order to address some of the shortcomings of line drop compensation, OTSVC is proposed [13]–[17]. By this method all the voltages at the major load buses are considered, and the control algorithm, shown in controls the voltages at all buses in an optimal way by minimizing the voltage deviation from nominal 1.0 p.u. considering a maximum operating voltage of the wind park to be 1.1 p.u. The central control system considers all the bus voltage values as input to a comparator block. The voltages are compared with a reference value equal to 1 p.u. in order to determine the voltage deviation at all grid buses. These voltage deviations are checked according to a voltage violation condition, to be able to decide which bus voltages should be changed. The voltage with the largest error is taken as

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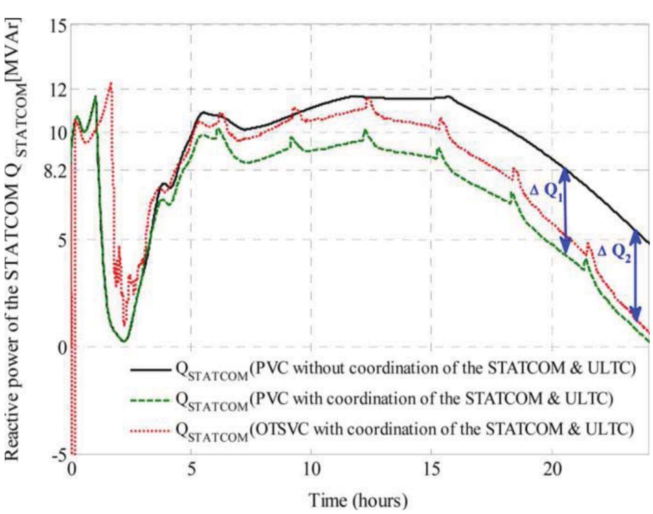
the control margin, which are then added to the secondary voltage reference, and transmitted to the STATCOM and ULTC. The measured voltages are filtered using a low-pass filter (LPF) with a time constant of 10 s to minimize the number of tap changes from the ULTC transformer and the loading on the STATCOM.

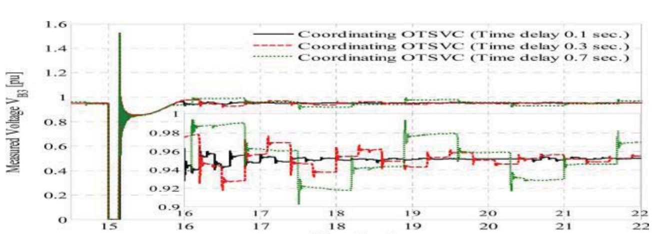
IV. System Characteristics

The system is modeled and simulated using MATLAB Sim- Power Systems in order to investigate the performance of the proposed controllers, under steady-state operation and during system contingencies. The PVC and OTSVC are tested taking into consideration the impact of changing short circuit ratios (SCRs) and the communication time delays. It is assumed that the wind park comprises either 6 or 12 WTGs.

a) Steady-State Operation Without Coordination of STATCOM and ULTC

First some steady-state simulation results using the OTSVC control strategy are presented. The wind park comprises six WTGs which are simulated at different system strength of SCRs, and the voltage profiles are compared with alternatively employing PVC and OTSVC The performance of the OTSVC strategy demonstrates better performance than the PVC in improving the network voltage profile. One disadvantage of using the OTSVC is, however, that the line currents increase since the reactive power compensation increases, and this would also increase the line losses. Further, we can note that the reactive power consumed by the wind park is inversely proportional to the SCR, due to the larger system impedance.





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b) Steady-State Operation With Coordination of STATCOM and ULTC

Then the coordination of the STATCOM and the ULTC transformer under steady-state is examined using either PVC or OTSVC. The simulations are performed using periodic load data, as shown in Fig. 6. This simulation case assumes that the load level varies from 50% to 250%. The simulation is carried out with 12 WTG connected at SCR shows how the STATCOM reactive power changes with the load, and it is noted that the STATCOM reactive power is much higher when the transformer tap is fixed and PVC is applied compared to when employing coordinated PVC or OTSVC. The loading of the STATCOM is reduced to nearly 50% at and in 252 IEEE TRANSACTIONS. The voltage control without the coordination of the STATCOM and the ULTC is not sufficient for controlling the bus-voltages due to the time response of the systems. The STATCOM normally reacts to a voltage deviation in a few milliseconds whereas the ULTC take some seconds to react. Consequently, the STATCOM may go to its limit in the steady-state voltage deviation and there by loose its primary function, The coordination is done by using the following settings: 1) The STATCOM reference voltage is set to be equal to the calculated ULTC reference voltage based on either PVC or OTSVC voltage control. 2) The dead band of the ULTC has to be known and the ULTC should operate when the controller voltage exceeds the ULTC dead band. The STATCOM react continuously due to the ULTC time delay for doing the tap changes. 3) The measured voltage signal to the ULTC are filtered an LPF with a time constant equal to 10 s to allow the STATCOM to react instantaneously to support the system for voltage deviations exceeding the dead band of the ULTC. steady-state operation so it is able to react with a higher reactive power margin at contingency situations. shows the improvement of the voltage profile in the whole network grid when applying the coordinated OTSVC.

c) Variation of Wind Speeds

The system is then simulated changing the wind speed for four wind turbines from 7 to 11 m/s. The measurements of the active power generation of the wind park and the loading of the STATCOM are undertaken to examine the performance of the coordinating controllers with changes of wind park generation, as shown in Figs. 9 and 10.The simulation results conclude that the coordinated voltage controller is able to minimize the loading of the STATCOM by stepping the ULTC, therefore improving the reactive power dynamic margin by and for the coordinated PVC. OTSVC, respectively.

d) Performance During Load Excursion

Next the performance of the different control methods is shown for a load excursion. In this case,

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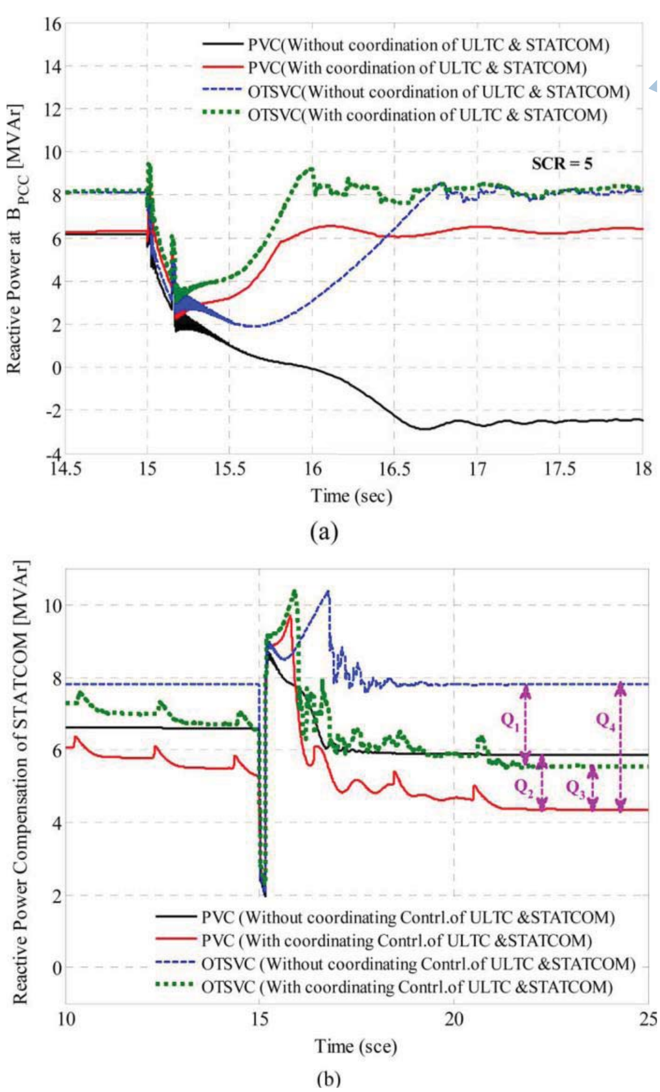
load 3 is increased by 100%. Again the system is controlled to ensure that the deviation of the voltages at all grid busses with reference to the voltage 1 p.u. is kept at a minimum. Again the OTSVC shows the best performance with regard to the voltage profile, but also to ensure that the loading of the STATCOM is less than for the other control methods (see Figs. 11 and 12). In this case, the maximum regulation margin was selected to bus B3_120, which was 0.06 p.u. in this case

e) Performance Following Disturbances

Then the performance of the OTSVC compared to the PVC following a disturbance in the form of a three phase to ground fault at bus B3_120 with duration of 150 ms is analyzed. The performance is analyzed both with and without the coordinated control between the STATCOM and the ULTC transformer. The assumed time delay associated with the OTSVC is set to 100 ms (corresponding to a fiber-optic solution) for the first simulations and the SCR of the system is set to 5 (simulations have shown that for a short circuit less than 4 the system never recovers). The SCR influence the system in two ways: The voltage drop along the lines is larger for weaker



connections, and the recovery time is larger. The initial voltage drop is dependent of the impedances between the voltage source and the impedance to the point of measurement and the fault location. For smaller SCR, the initial voltage drop is lower, since the wind park is electrically further away from the faulted bus and the load bus. As the wind park is moved further away from the load bus, the ability to aid the voltage recovery is reduced, due to the higher reactive power requirements of the line. In the analysis important measures such as the voltage dip, the voltage response, the reactive power reserve from the STATCOM, and the maximum critical clearing time (MCCT) of the fault are examined, since these can be used as indicators for the transient stability margin. the voltage at PCC is shown for the four control cases, and it is seen that the PVC without coordinated control of the STATCOM and the ULTC fails to control the system to recover after the fault. The three other control methods control the system in a way so the systems recover. The reactive power flow at the PCC and the reactive power supplied from the STATCOM is shown in Fig. 14. The coordinated STATCOM and ULTC transformer controls using either OSTVC or PVC minimize the loading of the STATCOM, thus the coordinated controls demonstrate better performance for ensuring a faster voltage response, voltage recovery and increasing the MCCT for faults. Therefore, the coordinated voltage control algorithms are recommended for enhancing the fault ride though (FRT) capability.

f) Impact of SCR and Communication Delays on the Transient Stability Margin

Finally, the impact of the SCR and the time delay on the transient stability margin is examined. The MCCT is examined for different SCR and the results are shown in Table III at a constant time delay for the OTSVC at 0.1 s. The results show again the better performance when using the coordinated control, the coordinated OTSVC with the best performance. In Table IV, the influence of the time delay of the communication system is shown for the network grid with different SCR. It is seen that an increased time delay has a negative impact on the voltage recovery. At the 700-ms delay for the OTSVC, the PVC is initially dominant, and only after the voltage has nearly completely recovered the OTSVC signal causes some small deviations around the reference value as shown in . This suggests that a decoupling of the two modes would be favorable for mitigation of this impact as shown in . This is most easily accomplished by inserting a low pass filter on secondary control signal, and in this way decouple the PVC from the OTSVC. Alternatively, a reduced bandwidth of the secondary control could be used.

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V. Conclusion

This paper has shown a new coordinated secondary voltage control for wind park substations where both a STATCOM and an ULTC transformer are present. The coordinated voltage control controls the ULTC transformer steps to maximize the capacity margin of the STATCOM and in this way the capacity dynamic margin is increased with up to 70% during system contingency situations and at the same time the number of tap-changes is minimized. The coordinated control for both PVC and OTSVC shows better performance for improving the voltage profile in steady-state conditions, for minimizing voltage dips, improving the voltage recovery after faults, and increasing the MCCT, with the coordinated OTSVC having the best performance of them all. Different SCRs and time delays of the OTSVC influence the performance of the controller and also the transient stability margin. However, only at a delay ofs more than 700 ms, the system response becomes unacceptable, and it should be possible to make the control system with a shorter delay or accomplished by inserting a low pass filter on the secondary control signal and in this way decouple the PVC from the OTSVC. Alternatively, a reduced bandwidth of the secondary control could be used.

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Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 5 Version 1.0 April 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

PWM Strategies for Multilevel Inverter and DC Link Capacitor Voltage Balancing For an Induction Motor Drive

By Mr. Srinivas Dasam & Dr. BV Sankerram

Abstract - Multilevel PWM techniques are extensions of twolevel PWM methods; the multiple levels in these inverters offer extra degrees of freedom and greater possibilities in terms of device utilization and effective switching frequency. Though the SPWM and its variations are popular PWM techniques in multilevel inverters, implementing them in a digital platform is tedious, as the pulse-widths can only be defined by transcendental equations. A dc link capacitor voltage balancing scheme is proposed for an induction motor drive. The motor is fed from with three-level inverters generating a five level output voltage structure. The proposed inverter vector locations exhibit multiplicity in the inverter switching combinations which is suitably exploited to arrive at a capacitor voltage balancing scheme. This allows the use of a single dc link power supply for the combined inverter structure. The lower order harmonic components in the output voltage waveform are eliminated by raising the carrier frequency.

GJRE- F Classification : FOR Code: 0906,090602,100599

PWM STRATEGIES FOR MULTILEVEL INVERTER AND DC LINK CAPACITOR VOLTAGE BALANCING FOR AN INDUCTION MOTOR DRIVE

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Abstract - Multilevel PWM techniques are extensions of two-level PWM methods; the multiple levels in these inverters offer extra degrees of freedom and greater possibilities in terms of device utilization and effective switching frequency. Though the SPWM and its variations are popular PWM techniques in multilevel inverters, implementing them in a digital platform is tedious, as the pulse-widths can only be defined by transcendental equations. A dc link capacitor voltage balancing scheme is proposed for an induction motor drive. The motor is fed from with three-level inverters generating a five level output voltage structure. The proposed inverter vector locations exhibit multiplicity in the inverter switching combinations which is suitably exploited to arrive at a capacitor voltage balancing scheme. This allows the use of a single dc link power supply for the combined inverter structure. The lower order harmonic components in the output voltage waveform are eliminated by raising the carrier frequency.

I. Introduction

Three-level inverters have attracted the attention of researchers since their introduction by Nabae et at. [1] in 1981. Though simple and elegant, neutral-clamped circuit topology has a few disadvantages. Neutral point fluctuation is commonly encountered as the capacitors connected to DC-bus carry load currents. Also, there is ambiguity regarding the voltage rating of the semiconductor devices, which are connected to the neutral point. This calls for a conservative selection of devices for reliable operation, which, however, increases cost. Various alternative circuit topologies have been suggested in the literature. H-bridge topology [2], [3] eliminates the problem of neutral fluctuation, but requires three isolated power supplies. Soh and Hyun [4] have suggested an improvisation of the conventional neutral clamped inverter in which a capacitor is connected across the neutral clamping diodes to ensure dynamic balancing of the voltage across the DC bus capacitors. This method alleviates the problem but does not eliminate it. Three-level inversion may also be achieved with two 2-level inverters, driving an open-end winding induction motor from either end [5], [6]. The inverters in this case require isolated power supplies to eliminate the harmonic currents of the triplen order in the individual motor phases Recently, Somasekhare t al. [7] have suggested an open-end winding induction motor drive, which obviates transformer isolation. But the DC bus utilization is slightly lower in this scheme when compared to the schemes proposed by Stemmler and Guggenbach [5] and Shivkumar et al. [6] The DC link capacitors in this circuit do not carry the load currents and hence the voltage fluctuations in the neutral point are absent. Also, the circuit configuration needs two isolated power supplies compared to H-bridge topology, which requires three isolated power supplies to achieve 3-level inversion. However, the power semiconductor switches in one bank (three in number) in one of the inverters of this circuit have to be rated for the full DC link voltage.

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a) Proposed 3-level inverter configuration

In the proposed 3-level inverter topology circuit, the cascade connection of two 2-level inverters accomplishes 3-level inversion (Fig. I). The output phases of Inverter 1 are connected to the DC input points of the corresponding phases in Inverter2. Each inverter is powered with an isolated DC power supply, with a voltage of ~j2 (Fig. I) when i) the top switch of that leg in Inverter2 is turned on, and ii) the bottom switch of the corresponding leg in Inverter1 is turned on.

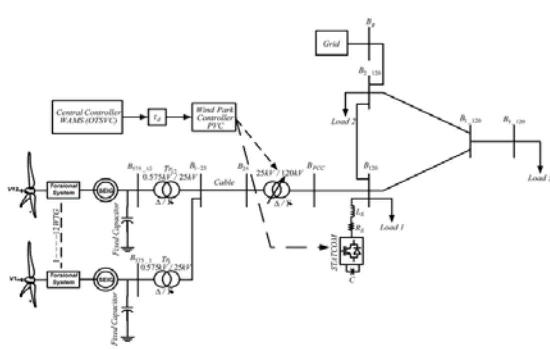

Fig.1 : Cascade connection of two 2-level inverters accomplishes 3-level inversion

Thus, the DC input points of individual phases of Inverter2 may be connected to a DC link voltage of ~j2 by turning on the top or the bottom switch of the corresponding phase leg in Inverter I. Additionally, the pole voltage of a given phase in Inverter2 attains a voltage of zero, if the bottom switch of the

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corresponding leg in Inverter2 is turned on. In this case, the DC input point of that phase for Inverter2 is floating as the top and bottom switches are switched complementarily in any leg in a 2-level inverter. This means that individual inverters are operated with a DC link voltage of 150 V. The motor is run in open loop using the V If control scheme. To demonstrate the working principle of this inverter scheme, space vector, modulation has been employed, which was implemented using look-up table approach. The space vector combinations at each space vector location have been chosen in such a way that both the inverters are switched with only one transition during the subinterval period.

II. Three-Level Inverter Scheme with Common-Mode Voltage Elimination for an Induction Motor Drive

A three-level inverter configuration with common mode voltage elimination is already presented in [10]. Only those switching combinations, which generate zero common mode voltage in the inverter poles, are used to switch the three-level inverters from both sides, thus resulting in zero common mode voltage across the machine phases [10]. Thus, appropriate selection of switching states, of individual three-level inverters, result into the total elimination of alternating common mode voltage from the inverter pole voltages as well as common mode voltages from the phase windings of the induction motor [10]. As the common modes voltages are absent in this scheme, individual three-level inverter structure can be supplied from single dc link as shown in Fig.1. The three-level structure is realized by cascading two conventional two-level inverters, resulting in a simple power bus structure for the proposed power circuit [9], [10]. The unbalance in the dc link capacitor voltages for the proposed open-end winding induction motor drive.

III. Switching Combinations and their Effect on dc Link Capacitor Voltages

As explained in the previous section, the inverter space vector locations have multiple switching combinations of inverter-1 and inverter-2 voltage space vectors (Fig.2). The central voltage location being referred as zero voltage vector (ZV), the voltage vector locations at the periphery of inner hexagon are referred as small voltage vectors (SV), the intermediate voltage vectors on outer periphery are referred as middle voltage vectors (MV), while the largest voltage vectors on outer periphery are referred as large voltage vectors (LV).

a) *Back-to-Back Intertie*

When interconnecting two diode-clamped multilevel inverter to-gather with a "dc capacitor link," as shown in Fig.2 the left-hand side converter serves as the rectifier for utility interface, and right-hand side converter serves as the inverter to supply the ac load. Each switch remains switching once per fundamental cycle. The result is a well-balanced voltage across each capacitor while maintaining the staircase voltage wave, because the unbalance voltages across each other tend to compensate each other. Such a dc capacitor link is categorized as the "back-to-back intertie." The purpose of the back-to-back intartie is to connect two asynchronous systems. It can be treated as 1) a frequency changer, 2) a phase shifter, or 3) a power flow controller. The power flow between the two systems can be controlled bidirectionally.

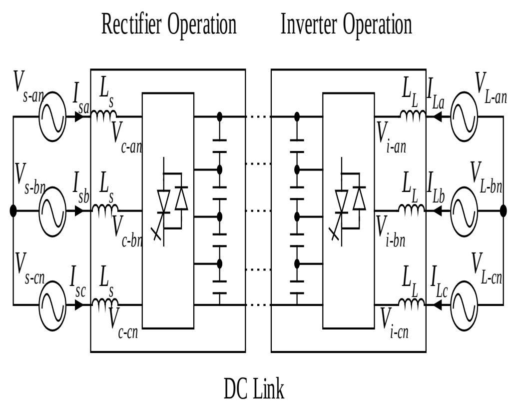

Fig.2 : General Structure of a back-to-back intertie system using two diode-clamped multilevel inverter.

b) *Utility compatible Adjustable Speed Drives*

An ideal utility compatible system requires unity power factor, negligible harmonics, no EMI, and high efficiency. By extending the application of the back-to-back intertie, the multilevel inverter can be used for a utility compatible adjustable speed drive (ASD) with the input from the utility constant frequency ac source and the output to the variable frequency ac load. The major differences, when using the same structure for ASD's and for back-to-back intertie, is the control design and size of capacitor. Because the ASD need to operate at different frequencies, the dc link capacitor needs to be well-sized to avoid a large voltage swing under dynamic condition.

c) *Converter Topology*

Figure.3 shows the two leg FCMLI topology for obtaining the different levels of voltage across the load. Although the dc source voltage sources are shown to be two, it is basically the same source. Initial values of capacitor voltages are considered to be the same and are given by a ratio of the dc source voltage V_{dc}. Switches S & S' on each leg are complementary to each other. These switching states are considered as depicted in Table

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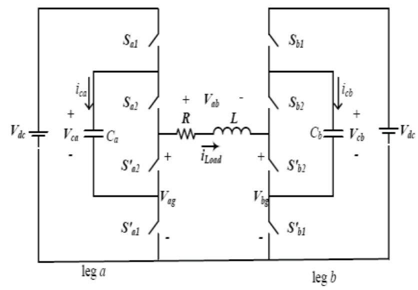

Fig.3 : FCMLI topology

Table1 : Switching states to determine state indicator

S1	S2	State
ON	ON	3
ON	OFF	2
OFF	ON	1
OFF	OFF	0

Voltage V_{bg} on *leg b* is 180 degrees out of phase with the voltage V_{ag} on leg a. Hence, the resultant voltage V_{ab} across the load is a multi level stair case waveform as shown in below figure

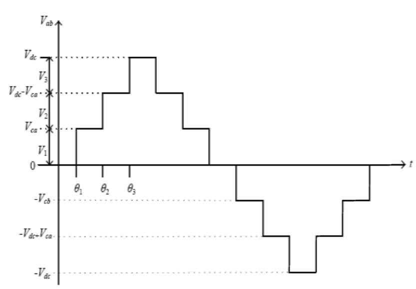

Fig.4 : Seven-level staircase voltage V_{ab}

Now that different voltage levels are obtained, the capacitor currents in terms of the load current can be tabulated as in Table2.

Table2 : Output voltages and capacitor currents

State	V_{ag}	V_{bg}	i_{ca}	i_{cb}
3	V_{dc}	$-V_{dc}$	0	0
2	$V_{dc}-V_{ca}$	$-V_{dc}+V_{cb}$	i_{Load}	$-i_{Load}$
1	V_{ca}	$-V_{cb}$	$-i_{Load}$	i_{Load}
0	0	0	0	0

$$V_{ab}(t) = \sum_{n=1,3,5}^{\infty} \frac{4}{n\pi}(V_1 Cosn\theta_1 + V_2 Cosn\theta_2 + V_3 Cosn\theta_3) Sin(n\omega t)$$

Where 'n' is the order of the harmonic and 'w' is the angular frequency. The voltage levels of the dc sources are equal and labeled to be V_{dc}. Also, the voltage of the capacitors is same and intended to be regulated at the modulation index in general is defined as:

Modulation Index M: V_m/V_{dc}

Where, Vm is the magnitude of the fundamental component of the output voltage.

Theta Calculations

Considering only the fundamental component and eliminating the 3rd and the 5th order harmonics, the following equations are used to calculate θ1, θ2, and θ3 for different values of the modulation index *'M'*. Here *'p'* is considered to be three.

$$V_{dc} * M = \frac{4}{\pi}\frac{V_{dc}}{3}(Cos\theta_1 + Cos\theta_2 + Cos\theta_3)$$

$$\frac{4}{3\pi}\frac{V_{dc}}{3}(Cos3\theta_1 + Cos3\theta_2 + Cos3\theta_3) = 0$$

$$\frac{4}{5\pi}\frac{V_{dc}}{3}(Cos5\theta_1 + Cos5\theta_2 + Cos5\theta_3) = 0$$

IV. Proposed Scheme for dc Link Capacitor Voltage Balancing

The inverter voltage vectors belonging to ZV, NSV, MV, and LV groups can be effectively used to maintain the voltage balance across the dc link capacitors. The input to the voltage-balancing scheme can be either the difference in the capacitor voltages, or the load current drawn from middle node, as the voltage unbalance can be determined. Each inverter voltage vector locations from groups NSV and MV have two switching combinations.

a) Hysteresis Controller Based Closed Loop DC Link Balancing Scheme

With the voltage-balancing scheme implemented in the above manner, a gradual deviation in the dc link voltages is observed. The possible reasons for this are, the use of the asynchronous PWM, the unequal time durations of the MV and NSV inverter vectors in consecutive switching intervals, unbalanced load currents etc. As discussed in the previous section, the switching combinations belonging to USV and LSV group can charge the lower and the upper capacitor, respectively. Thus, if the difference in the two capacitors of the dc link is monitored, the switching combinations from USV or LSV groups can be selected for inverter switching, which will bring back the deviation in the capacitor voltages to zero. This is done using a hysteresis controller. The input to the controller is the difference between the dc link capacitor voltages; the normal control band is set depending upon the maximum deviation that can be allowed in the dc link voltages. The controller outputs, 0 if the is within the

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normal band, 1 if is greater than the control band and 1 if the is less than the control band. The schematic of the closed loop voltage balancing scheme is shown in Fig. 5. The output of the controller along with "SEQ" signal is used to select the appropriate value of the signal "state," which is given to a digital logic.

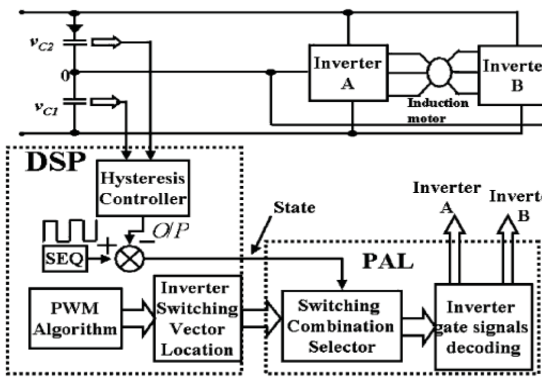

Fig5 : Hysteresis Controller Based Closed Loop DC Link Balancing Scheme

V. Dc link Capacitor Voltage Balancing During Inverter Operation in Over-Modulation and 12-Step Mode

It is to be noted that only the inverter vectors belonging to USV or LSV groups have strong capability to charge/discharge the dc link capacitors. During motor operation in over-modulation range, the inverter vectors belonging to MV and LV groups are switched for maximum duration, in a switching interval, as compared to the inverter voltage vectors belonging to SV group. The extreme case is the 12-step operation, wherein the inverter vectors from the SV group are not switched at all. Under steady state and dynamic operation, in over-modulation, the controller can maintain the capacitor voltage balance by switching MV and LV vectors. The SV vectors are switched for less time duration, the time required to bring back the capacitor voltages to the balanced state, is more during over modulation operation. In extreme case, the inverter vectors from SV group are not switched in 12-step mode. If there is mismatch in the capacitor voltages due to the asynchronous PWM or asymmetric loads, the capacitor voltages are balanced by reducing the modulation index momentarily. This allows the switching of the inverter vectors belonging to SV group and the dc link capacitor voltages are brought back to the balanced state as shown in the simulation results of Fig. 6. Thus while, USV vectors were having charging effect on C1 and discharging effect on C2 in motoring mode, they have discharging effect on C1 and charging effect on C2 in regenerative mode. Thus, the controllers need to sense the power direction, to suitably switch the switching combinations belonging to the vector group, which will reduce the error in the dc link capacitor voltages. Determining the operating mode (i.e., motoring/generating) requires current sensing. The determination of current direction for currents drawn from dc link involves hardware sensors or can be judged from direction of power flow

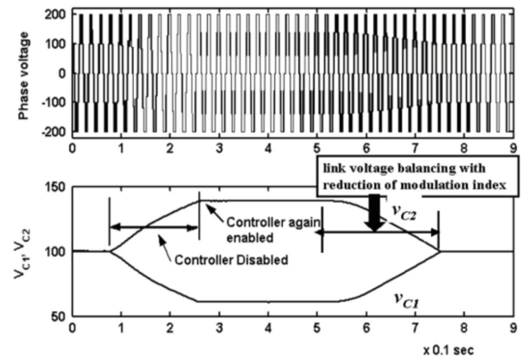

Fig. 6 : DC link balancing with momentary reduction in modulation index.

If the motor is operating in regenerative mode, the actions taken by the controller will worsen the voltage balance. An additional hysteresis comparator is used to sense this change. The control band of this comparator is placed above the control band of the main inner comparators. Thus, with motor operating in regenerative mode, the outer comparators of hysteresis controller gets activated if the dc link voltage unbalance exceeds the outer comparator settings and the switching combinations belonging to the USV or LSV vector group, which reduces the voltage unbalance, are selected for inverter switching. As shown in simulation results of Fig.6, the motor is initially operating in motoring mode and the load torque is made negative thus driving the motor in regenerative mode. The voltage balancing controller is disabled which will cause rapid growth in dc link unbalance. When the voltage-balancing scheme is enabled again, the capacitor voltages are brought back to the normal value, similar to the case with motor operating in motoring mode.

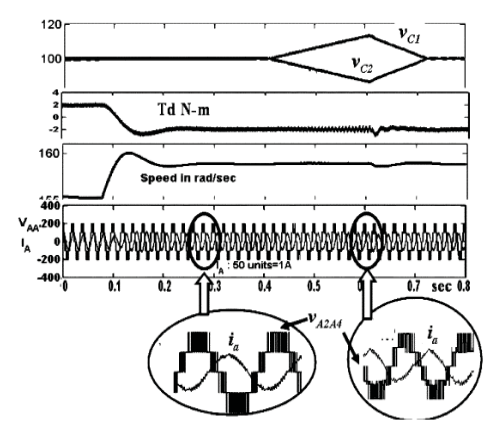

Fig. 7 : Capacitor voltages when the closed loop dc link voltage balancing scheme is turned off in regenerating mode

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VI. Simulation Results

The performance of these methods is studied through Matlab simulation.. It is clear that there is a reduction in THD.

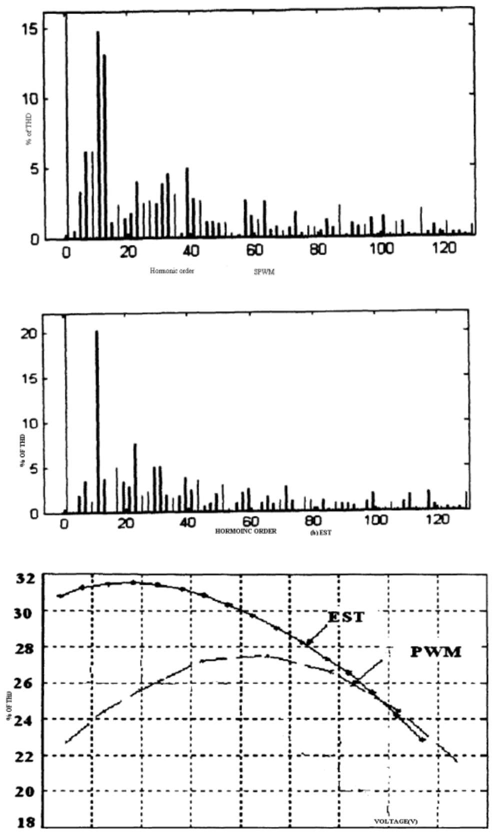

Fig.8a,b,c : Capacitor voltages for the closed loop dc link voltage

The three-level structure is realized by cascading the conventional two two-level inverters, resulting into simple power bus structure for the proposed scheme. Thus, the proposed inverter structure does not require any clamping diodes which are required in NPC inverter topology. The proposed scheme has more multiplicity in the inverter voltage vector locations as compared to conventional single inverter fed drive which are effectively used to balance the dc link capacitor voltages without disturbing the SVPWM modulation. Thus, a single front-end rectifier of rating nearly half to that of a conventional two-level inverter can be used, with two capacitors for splitting the dc link voltage. The proposed capacitor voltage balancing scheme is based on altering the switching combinations of the inverter voltage vectors, having exactly opposite affect on the capacitor voltages, for consecutive sampling durations. A simple closed loop hysteresis controller is used to balance the dc link capacitor voltages throughout the modulation range of the drive. With these values of firing angles, the capacitor voltages, the output voltage and the load current at different values of power factor were observed under constant power operation of 200 W by varying the load, using MATLAB Simulink. The values of the load resistance and inductance under different power factor conditions and modulation indices are given in following Tables Load resistance (R) and inductance (L) at different power factors when M=0.7

Table3 : Load resistance (R) and inductance (L) at different power factors when M=0.7

Power Factor	R (Ω)	L (mH)
0.3	6.1224	3.09
0.4	10.884	3.969
0.5	17.006	4.68
0.6	24.48	5.196
0.7	33.33	5.412
0.8	43.537	5.196
0.9	55.102	4.24

These values are found from the power calculations and the power factor formulae given by,

$$P = \frac{V_m^2}{R^2 + L^2\omega^2}\frac{R}{2} = 200$$

$$tan\Phi = \frac{L\omega}{R}$$

where, *'P'* is the output power, „ " is the power factor angle and *'V_m'* is the magnitude of the fundamental component of the output voltage obtained from the above equation. The fundamental frequency is considered to be 1 kHz. The simulation results showing the capacitor voltages, load current and the output voltage for M=0.7 and M=0.877 at a power factor of 0.8 are shown in Figs.9 to 14 respectively. Capacitor voltage V_{cb} is similar to that of V_{ca}, voltage across the capacitor *Ca* for both the modulation indices.

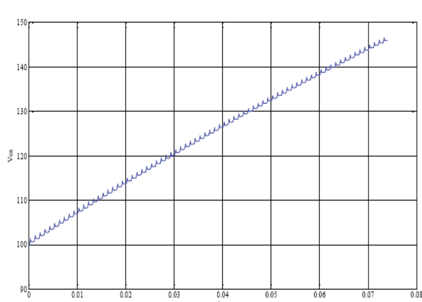

Fig. 9 : Capacitor voltage *Vca* at *M*=0.7 & PF=0.8

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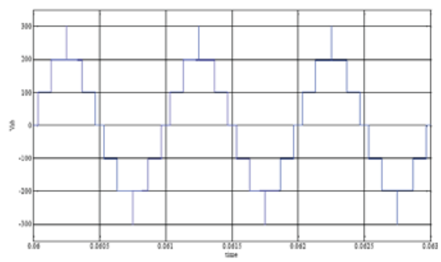

Fig. 10 : Output Voltage *Vab* at *M*=0.7 & PF=0.8

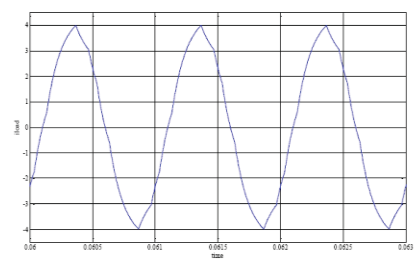

Fig. 11 : Load current *iload* at *M*=0.7 & PF=0.8

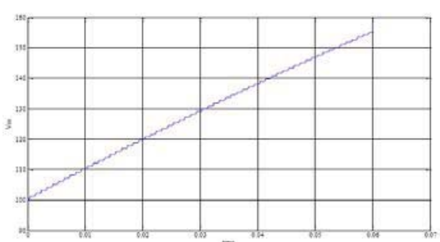

Fig.12 : Capacitor voltage *Vca* at *M*=0.877 & PF=0.8

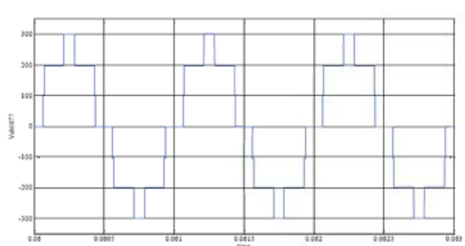

Fig. 13 : Output Voltage *Vab* at *M*=0.877 & PF=0.8

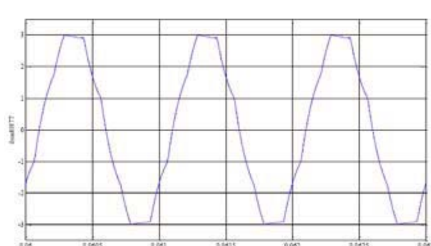

Fig. 14 : Load current *iload* at *M*=0.877 & PF=0.8

Next aspect that was looked into was the effect of power factor on output voltage and load current. Figures15 to 18 shows the same at power factor 0.7 for two different modulation indices *M*=0.7 and *M*=0.877.

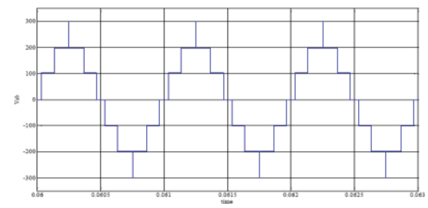

Fig. 15 : Output voltage *Vab* at *M*=0.7 & PF=0.7

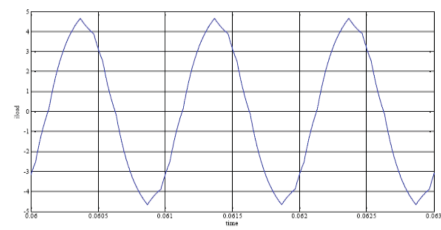

Fig.16 : Load current *iload* at *M*=0.7 & PF=0.7

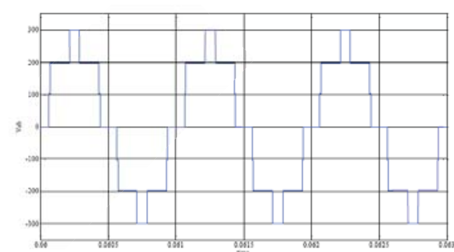

Fig.17 : Output voltage *Vab* at *M*=0.877 & PF=0.7

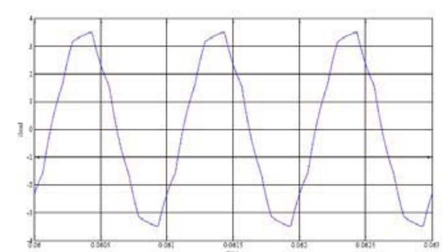

Fig.18 : Load current *iload* at *M*=0.877 & PF=0.7

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Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 5 Version 1.0 April 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Remodelling RC4 Algorithm for Secure Communication for WEP/WLAN Protocol

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Abstract - Wireless Local Area (WLAN) has become a hot spot of application in the field oftelecommunication these years. To secure WLAN for data transmission, RC4 algorithm is able to provide the advantages of fast performance in the resource constrained environment. This paper analyzes the security of RC4 algorithm, presents a way to enhance the security of RC4 algorithm and analysis the affection of the enhanced algorithm by using MD5/hash function.

Keywords : RC4, WEP, WLAN.

GJRE- F Classification : FOR Code: C.2.1,G.1

REMODELLING RC4 ALGORITHM FOR SECURE COMMUNICATION FOR WEPWLAN PROTOCOL

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Remodelling RC4 Algorithm for Secure Communication for WEP/WLAN Protocol

Laxmi Mounika.Nannaka [α], Hepzybah.Singarapu [σ] & Ramadevi.Puli [ρ]

Abstract - Wireless Local Area (WLAN) has become a hot spot of application in the field of telecommunication these years. To secure WLAN for data transmission, RC4 algorithm is able to provide the advantages of fast performance in the resource constrained environment. This paper analyzes the security of RC4 algorithm, presents a way to enhance the security of RC4 algorithm and analysis the affection of the enhanced algorithm by using MD5/hash function.

Keywords : RC4, WEP, WLAN.

I. Introduction

Wireless Local Area Network (WLAN) is the network that utilizes radio frequency technology instead of traditional coaxial. WLAN is widely used in many conditions, especially when it's difficult to install traditional network. As the openness and sharing of wireless channel nature, the security of wireless data stream becomes particularly prominent [1].IEEE802.11 standard for WLAN defines two types of authentication open system authentication and shared key authentication, and uses RC4 stream encryption algorithm of the Wired Equivalent Protection (WEP) protocol to enhance its security. However, the facts show that the WEP protocol has not met the desired level of safety. On the contrary, WEP itself also has fatal security flaws, tampering with the data for a variety of active attacks and passive eavesdropping on the data provided to facilitate aggression. WEP uses the Initial Vector (IV) to avoid duplication of key stream. Beginning in 2001, several serious weaknesses were reported and they demonstrate that WEP protocol is vulnerable in a number of areas. In essence, the problem is not in RC4 itself but in the way to generate the key and in how to use the key for RC4 encryption. Many hackers and computer security experts have discovered the WEP design flaws, which indicate that IEEE802.11 standards can only provide limited support to confidentiality. WEP provides a 40-bit key, which may be sufficient to keep away a common hacker but incapable to ward off a professional hacker. Either a 40-bit key or a 128-bit key can be easily cracked within two or three hours. RC4 is probably the most widely used stream cipher nowadays due to its simplicity and high efficiency. This paper focuses on the research to enhance RC4 algorithm. The rest of the paper is organized as follows. RC4 algorithm is introduced in Section 2. In Section 3, we present the RC4 encryption and decryption. The weakness of RC4 is presented in Section 4. In Section 5, we provide analysis of the main attack. Section 6 introduces the improvement of RC4. Section 7 concludes this paper.

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II. Rc4 Algorithm

The principle of RC4 algorithm consists of two Components: key-scheduling algorithm (KSA) and pseudo-random number generation algorithm (PRGA). The key function of KSA is to complete initialization of RC4 Key, while the key function of PRGA is to produce pseudo-random number. The pseudo code for RC4 algorithm (KSA and PRGA) is shown below.

```
KSA
Begin
for i=0 to 255
Si=i; Ki=K[i mod n];
End
For k=0;for i=0 to 255
j=(j+Si+Ki) mod 256
swap(Si,Sj)
end for
end
PRGA
begin
i=0;j=0;
while(true)
i=(i+1) mod 256 j=(j+Si) mod 256;
swap(Si,Sj); t=(Si+Sj) mod 256
K=St;
end loop; end
```

Stream ciphers and block ciphers are two classes of encryption algorithms. Stream ciphers encrypt a one-bit plaintext at a time, using a timedependent encryption transformation. Block ciphers encrypt groups of plaintext characters using a fixed encryption transformation. Stream Ciphers and block ciphers have their respective characteristics, but stream ciphers are almost always faster and use far less code than block ciphers do. RC4 is a variable key-size stream

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cipher based on a 256-byte secret internal state and two one-byte indexes. The data is encrypted by XORing data with the key stream which is generated by RC4 from a base key. For a given base key, KSA generates an initial permutation state denoted by S0. PRGA is a repeated loop procedure and each loop generates a one-byte pseudo-random output as the stream key. At each loop, a one-byte stream key is generated and it is XORed with one-byte of the plaintext, in the meantime a new 256-byte permutation state S as well as two one-byte indices i and j are updated, which defined by (Sk+1, ik+1, jk+1) = PRGA(Sk, ik, jk) where ik+1and jk+1 are the indices and Sk+1 is the state updated from ik, jk, and Sk by applying one loop of PRGA.

III. Rc4 Encryption and Decryption

The encryption process of WEP is shown in Figure1, WEP uses 40-bit or 104-bit encryption key connected with 24-bit IV to generate 64-bit or 128-bit seed key, and then send the seed key to a random generator PRNG, encrypt the plaintext with pseudo-random sequence [2]. System uses CRC32 (32-bit cyclic checksum) for integrity verifying to ensure that the message will not be modified during transmission that sends IV, plaintext and integrity check value (ICV) to the other [3]. The decryption process of WEP is shown in Figure 1. The decryption key sequence is generated in the same way that generates encryption key, XORed with cipher text to get the plaintext. Compare ICV with integrity check value

ICV ' calculated by CRC32, if the encryption key is the same as decryption key, and ICV '= ICV, then the receiver gets the original plaintext data. Many encryption algorithms are widely available in wired networks. They can be categorized into a symmetric key encryption. In symmetric key encryption and secret key encryption, only one key is used to encrypt and decrypt data and the key should be distributed before transmission between entities. It is also very efficient since the key size can be small, while the functions used for encryption are hardware operations, and the encryption time can be very short. However, in large communication networks, key distribution can be a significant problem. Asymmetric key encryption or public key encryption is used to solve the key distribution problem. This uses two keys, one for encryption and another for decryption, and there is no need for distributing them prior to transmission. Public key encryption is based on mathematical functions, computationally intensive and not very efficient for small wireless devices.

Generally, most encryptions used in wireless devices are based on symmetric key encryption, such as RC4. RC4 is a stream cipher designed by Ron Rivest in 1987 and it is widely used in many applications today and in wireless networks such as IEEE 802.11 WEP and CDPD. With a unique key, a stream of pseudo-random numbers is generated, and then the encryption of data XORs the pseudo-random numbers from the stream with the data. RC4 is known to be fast and efficient, for it can be written using only a few lines of codes and requires only 256 bytes of random access memory (RAM). Hence, it is one of the best encryption schemes during the past decade. RC4 is standardized to provide security services in WLAN using the WEP protocol. However, Fluhrer and many researchers have discovered several vulnerabilities in the RC4 algorithm. The weaknesses in RC4 and loopholes in the WEP protocol have resulted in a new standard for security in WLAN (IEEE 802.11i) proposing a new protocol based on the advanced encryption standard (AES). AES is a block cipher designed by Joan Daemen and Vincent Rijmen that has a variable key length of 128, 192, or 256 bits to encrypt data blocks of 128, 192, or 256 bits long. Both block and key length are extensible to multiples of 32 bits. AES encryption is fast and flexible, and it can be implemented on various platforms especially in small devices and smart cards. Also, AES has been rigorously tested for security loopholes for a few years before it was standardized by NIST.Figure 1 shows the process of encryption and the reverse of this is decryption.

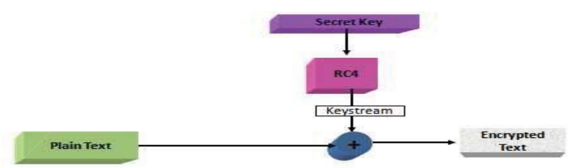

Figure 1 : WEP Encryption

IV. Rc4 Weakness

The algorithm loopholes and key management loopholes are the weaknesses of RC4 algorithm.

a) Algorithm Loopholes

WEP uses RC4 algorithm to enhance the security, but there are still some problems. First of all, RC4 is a stream encryption algorithm. If one bit lost, the entire data packet must be discarded, and the sender need to retransmit the lost data packet until the receiver accept the data packet, and WEP algorithm must reinitialize IV after sending each data packet.

Secondly, RC4 algorithm has the following characteristics: assuming CT1, CT2 as the cipher text, PT1, PT2 as the plaintext, we get the relationship that CT1=PT1 XOR RC4 (key), CT2=PT2 XOR RC4(key), CT1 XOR CT2=PT1 XOR PT2. As RC4 uses the same key, if we know PT1, and then we can *3624 2010 Chinese Control and Decision Conference* get PT2. If there is enough plaintext, through "dictionary" we will decrypt almost all the data [4]. 802.11 uses 24-bit IV to ensure that each data packet uses a different key, but if the standard 802.11 runs in 11Mbps network in a single

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base station, the whole key space will exhaust in less than an hour, and in a larger network with multiple base stations the time to exhaust the key space will be much shorter. The phenomenon of the IV re-emergence results in the degradation of RC4 algorithm performance, and the WEP becomes much more vulnerable to be attacked.

At present, most of the 802.11 WLANs are used as a datalink layer in TCP / IP networks, and each packet contains a transmission that contains a large number of known plaintext information which will allow hackers to restore transmission frames for each part of the key stream. Hackers can get enough information to use RC4 encryption algorithm to calculate the seed of the original information.

b) Key Management Loopholes

In the WEP mechanism for key generation and distribution, there is no provision for key management. The use of the key is not clearly defined, and the key is used rather confused.

The data encryption keys are mainly two kinds default key and key-mapping key. Default key is to configure the default settings. Key-mapping key is for different senders and the receivers to send and receive data packet by using key encryption to deal with the key. In order to get this key, each systemust maintain a key table to keep the communication used for their key-mapping keys record. In each communication, receiver finds in the table to get whether it is shared by users themselves and the communication key used for information encryption and decryption. Otherwise, we use the default key with the selected key ID,and encrypt key-mapping keys for the selection of superior to any other keys. The use of keymapping keys can enhance the security, but in fact people rarely use this key. As the network expands, the space will be used to store the key growing; on the other hand this key needs to use other methods to send which is much more difficult to achieve. For the users' man-made factors, in fact people use mainly the key ID for the 0 default key. From the above analysis we can see that most users use the key ID for the 0 default key. In this way, it increases the possibility of key reuse between sites, while the mechanism of the WEP key reuse has no restriction, and once the second key is manually loaded, it rarely updates. As the use of WEP mechanism devices is to store the key, so if the device is lost, it is possible for hackers to use.

V. Attack

As RC4 is probably the most widely used stream cipher nowadays due to its simplicity and high efficiency, the attack on RC4 is also a hot research topic. The attack can be mainly divided into two types, force attack, key stream distinguisher.

a) Force Attack

Brute Force Attacks, a brute force attack on encrypted messages, otherwise known as a "known plaintext attack", consists of decrypting an intercepted message with every possible key and comparing the result to the "known" plaintext. The "known" text is essentially guessed, but is easily deduced from the fact that communication sessions often begin with the same sequence of bytes. For an attack of this kind to be successful, only a small number of "known" bytes are necessary, making the guessing process significantly easier.

b) Key Stream Distinguisher

The key stream generator can not be really random, so that we can distinguish the key stream generated and true random key sequence, which is a theoretical attack model. Distinguisher is an effective algorithm to distinguish the really random sequence from the generated key stream. The distinguisher between what we call key stream generated by RC4 and really random key stream is to provide some basis and method to confirm the RC4 key stream generated in which specific key word is not random, and find the non-random key stream in order to attack. Golic [5] found the weakness of RC4 linear changes, and Fluhrer and McGrew [6] moved on with the result. Maintin and Shimir[7] give the attack method on this point.

VI. Improvement

Modern cryptographic technique is divided into two types, symmetric encryption system and public key encryption system. Symmetric encryption system communicating parts need a safe way to ensure key sharing; public key encryption system communicating parts have their own pair of keys.

In general, data processing efficiency of public key encryption system is not as high as symmetric encryption system, but the key is easier to manage. Therefore, we use public key encryption system for both parts to consult and then consult the key, use symmetric cryptography for data encryption and decryption. This maximizes the advantage of two types of cryptography. Key of variable or constant length is given to MD5 and the output of MD5 is 128 bits. Among those 128 bits only 40 bits are taken(any 40 bits) and given as input to RC4. The input and output of RC4 is 40 bit.

In RC4, the key is generated and it is XORed with plain text. This project uses the concept of stream cipher, where the data is encrypted bit by bit(encryption is fast when compared with block cipher). Stream cipher is used because this algorithm is used in Wi-Fi where continuous transmission is desired.

Elgamal, as a typical public key encryption system, is widely used, and we use Elgamal for key agreement to resolve the RC4 key management issues. Elgamal encryption is an asymmetric key encryption algorithm for public-key cryptography. Elgamal encryption consists of three components: the key generator, the encryption algorithm, and the decryption algorithm. The RC4 algorithm encryption improved data processing is shown in Figure 2.

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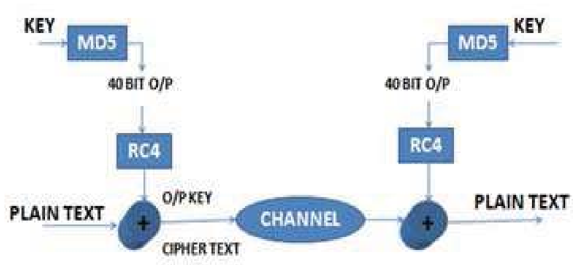

Assault for different lengths IV has different analysis lengths. If the IV length is 4 byte, the probability that each IV can be used for the first byte correlation analysis is only 4.32×10-5, and the number of weak IV that needs to analyze a byte KC in the key is l .33×106. In order to improve the RC4 security, we use a 256-bit key.

In the analysis of 8 byte RC4 pseudo-random streams, we get the result that the first output bit has 36% probability to equal with the approximate; the second bit has 35.9% probability, and so on.

The 48th bit has 0.4% probability. Therefore, in order to ensure the difficulty of cryptanalysis, in the improved RC4 method, we don't use the first 48 bit pseudo-random stream to avoid the attack by using the bias of the first few bits in output stream. In the 11Mbps network, the transmission of 1500 byte data packets will come up with the situation that different packets use the same IV in about 5 hours: 11(Mbps)/(1500Byte/packet*8bit/Byte) = 917 packet/s 2_{24} = 1677216

1677216/917 = 5.1 h

Using the improved RC4 in the 11 Mb/s networks, the time that different packets use the same time IV in the transmission of 1500 Byte data packets is about 54 days.

2_{32} = 4294967296

4294967296/917 = 1301 h = 54 d

VII. Concluːions

WLAN has some security weakness due to RC4 weakness, linear weakness and IV weakness. The improved RC4 can raise the security level of RC4, so does the WLAN, and it can be used as temporary method as it's easy to update. The new block encryption algorithm, such as RC5, will be used as the security solution for its high encryption level in future.

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Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 5 Version 1.0 April 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Design of multiplierless 2-D sharp wideband filters using FRM and GSA

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Abstract - One of the efficient and most popular technique for designing sharp 1-D linear phase FIR filters is the Frequency Response Masking (FRM) approach. It is an effective method for the design of high speed , low power, sharp FIR digital filters with a small number of non-zero coefficients. Very recently, a modified McClellan transformation(T1 and T2) is proposed (Jie-Cherng Liu and Yang-Lung Tai, 2011) for converting 1-D linear phase FIR digital filter to 2-D digital filter, in which the transformation is completely multiplierless. So the resulting 2-D filter contains the same number of multipliers as the 1-D digital filter. In this paper, our aim is to design a 2-D linear phase FIR filter which is completely multiplierless , by designing a multiplier free 1-D linear phase FRM FIR filter and using multiplierless transformation.

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GJRE- F Classification : FOR Code: 0906

DESIGN OF MULTIPLIERLESS 2-D SHARP WIDEBAND FILTERS USING FRM AND GSA

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Design of multiplierless 2-D sharp wideband filters using FRM and GSA

Manju Manuel [α], Remya Krishnan [σ], Elizabeth Elias [ρ]

Abstract - One of the efficient and most popular technique for designing sharp 1-D linear phase FIR filters is the Frequency Response Masking (FRM) approach. It is an effective method for the design of high speed , low power, sharp FIR digital filters with a small number of non-zero coefficients. Very recently, a modified McClellan transformation(T1 and T2) is proposed (Jie-Cherng Liu and Yang-Lung Tai, 2011) for converting 1-D linear phase FIR digital filter to 2-D digital filter, in which the transformation is completely multiplierless. So the resulting 2-D filter contains the same number of multipliers as the 1-D digital filter. In this paper, our aim is to design a 2-D linear phase FIR filter which is completely multiplierless , by designing a multiplier free 1-D linear phase FRM FIR filter and using multiplierless transformation. This paper presents a novel population-based optimization algorithm called Gravitational Search Algorithm(GSA) (Rashedi, 2009) for the design and optimization of FRM FIR digital filter whose coefficients are synthesized in the conventional Canonic Signed-Digit (CSD) format. Simulation results show that GSA gives a better performance than the Genetic Algorithm(GA).

Keywords : Frequency Response Masking, T1 and T2 Transformations, Canonic Signed-Digit(CSD), Gravitational Search Algorithm(GSA), Two-Dimensional (2-D) Filter,

I. Introduction

The field of the two dimensional filters and their design methods have been investigated by many researchers for more than three decades and have been deployed in a variety of application scenarios. Different techniques exist for the design of 2-D linear phase FIR filters which include windowing, frequency sampling, linear programming and Chebyshev techniques (Lim, 1990). These techniques produce a better approximation to an ideal response for a given filter, but the design of the filters requires large amount of computation and it becomes complex for higher order filters. Another method called Frequency transformation method (Lim, 1990) for the design of 2-D linear phase FIR filter from a 1-D linear phase FIR filter, is simple and has high computational efficiency. As the time required by the transformation method is less, it helps to design higher order filters with modest computation time, meeting the filter specifications closely. For the implementation of a filter whose impulse response is (N×N) point, N2 multiplications per output value are required using direct convolution, but a filter obtained by McClellan transformation can be implemented with a number of multiplications per output value which is proportional to N (Mersereau, 1976). Very recently Liu and Tai (Jie-Cherng Liu and Yang-Lung Tai, 2011) have proposed two multiplierless transformation (T1 and T2) which are capable of designing a 2-D filter with circular contour even at wideband radius. This is bestowed with the feature that, using a single transformation, a 1-D filter can be converted to its 2-D equivalent without any optimization procedures or complicated computations.

In this paper, we propose the design of a sharp multiplierless 2-D circularly symmetric, wideband filter using the transformations proposed in (Jie-Cherng Liu and Yang-Lung Tai, 2011). Sharpness is achieved by using FRM for the design of the 1-D filter. FRM technique provides a cost - effective way for the design of high speed, low power FIR digital filters, which leads to very low hardware complexity, round off noise and coefficient sensitivity (Y. C. Lim, 1986). The 1-D FRM filter is made multiplierless by representing it in the Canonic Signed Digit (CSD) space. The T1 and T2 transformations are completely multiplierless. When the digital filter coefficients are quantized to the Signed-Power-Of–Two space(SPT), multipliers can be replaced by a series of shift and add operations (R.Hartley, 1996) during the implementation. Among the various SPT forms, the CSD representation is a minimal one. The advantages of CSD representation are that it decreases the number of additions/subtraction needed and handle negative multipliers (R.Hartley, 1996). After the quantization of the infinite-precision multiplier coefficient values, the resulting 1-D FRM FIR digital filter will no longer meet the initial design specifications. As a result, optimization methods have to be introduced to obtain finite precision digital filters that satisfy the design specifications closely. Over the last decades, there has been a growing interest in algorithms inspired by the behavior of natural phenomena (D.H. Kim, 2007), (K.S. Tang,1996), (M. Dorigo, 1996). There are different heuristic algorithms in the literature which resemble various physical and biological processes, such as Genetic Algorithm, Simulated Annealing (S. Kirkpatrick, 1983), Artifical Immune System (J.D. Farmer, 1986), Ant Colony Search Algorithm, Particle Swarm Optimization (J. Kennedy, 1995) etc. for solving different optimization problems. In this paper, a new population based algorithm named Gravitational Search Algorithm (GSA) (Rashedi, 2009) has been used, which is based on Newtonian law of gravity and law of motion. We propose a discrete optimization based on modified GSA. This algorithm is modified in such a way that during the

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process of optimization, the candidate solution turns out to be integers. This multiplierless 1-D filter is in-turn converted to a 2-D multiplierless filter by using multiplierless transformation like T1 or T2. It is found that the magnitude response specifications using this algorithm are better than those obtained with other optimization algorithms like integer coded GA (Manoj, 2009). The paper is organized as follows. Section II gives an overview of frequency response masking. In Section III, the T1 and T2 transformation is briefed. Section IV gives an overview of the GSA algorithm. The design of 1-D multiplierless FRM linear phase filter is discussed Section V. Section VI illustrates the proposed design of multiplier-less 2-D FRM filter using the modified GSA algorithm. The results and discussions are done in Section VII and Section VIII gives the conclusions.

II. Frequency Response Masking

As the filter length is inversely proportional to the width of the transition band, higher order filters are needed for the implementation of narrow transition width FIR filters. Frequency response masking technique is an effective method for the design of high speed, low power, sharp FIR digital filters. It is suitable for implementing linear phase, arbitrary passband sharp FIR filters (Y. C. Lim, 1986) with a few number of non-zero coefficients. The computational complexity of the FRM is considerably small compared with the complexity of the filter designed using the traditional minimax approach having equivalent frequency response. Since multipliers are the most power consuming elements in a filter, reducing the number of multipliers is equivalent to reducing the power consumption and chip area. Due to these advantages, FRM has been deployed in a wide range of applications like FPGA, audio processing, beam-forming etc (Lu, W.S, Hinamoto, 2008). The basic block diagram of the overall FRM filter using several subfilters is shown in Fig(1).

The narrow transition width of FRM results from the interpolated version of prototype filter Fa(zM), derived by replacing each delay element of Fa(z) by M delay elements and Fc(zM) is its complementary version obtained by subtracting the output of Fa(zM) from a suitably delayed version of the input. There are two parallel branches each of which is composed of an interpolated model filter in cascade with masking filters FMa(z) and FMc(z) respectively. Interpolation leads to the imaging of the frequency response along with reduction of the passband and transition band by a factor of M. Masking filters are used to select the useful part of Fa(zM) and Fc(zM). Addition of two masked responses gives the response of a sharp wideband FIR filter.

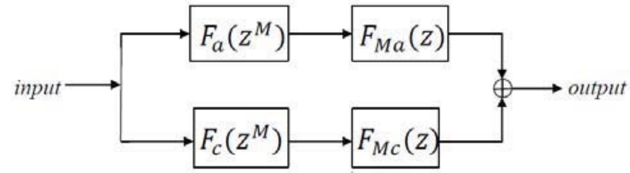

Fig.1 : Block diagram of FRM Approach.

III. Frequency Transformations

Generalised McClellan transformation converts 1-D linear phase filter H(Ω) into a 2-D linear phase filter H(ω1,ω2) by means of the substitution of variables (Mersereau, 1976).

$$H(\Omega) = \sum_{n=0}^{N} a(n)cos\Omega n \qquad (1)$$

where

$$a(n) = \begin{cases} h(0), for\ n = 0 \\ 2h(n), otherwise \end{cases}$$

h(n) is the 1-D prototype filter coefficients. Approximating H(Ω) using n-th order Chebyshev polynomial,

$$H(\Omega) = \sum_{n=0}^{N} a(n)T_n\,[f(\omega_1,\omega_2)] \qquad (2)$$

where $f(\omega_1,\omega_2)=2(\cos(\omega_1/2)\cos(\omega_2/2))^2-1$ for obtaining circular symmetry.

To get a better matching of a specified contour, higher order McClellan transformation can be used. But as the order increases more parameters are needed, which increases the complexity. To overcome this difficulty, the original McClellan transformation is modified to a k-th order McClellan transformation (Jie-Cherng Liu and Yang-Lung Tai, 2011) given by

$$f(\omega_1,\omega_2) = 2[cos(\omega_1/2)\,cos(\omega_1/2)\,]^{2k} - 1 \quad (3)$$

To overcome the squarish effect of the contour produced by the McClellan transformation, a cascade term has been introduced to the k-th order McClellan transformation which results in T1 transformation and T2 transformation (Jie-Cherng Liu and Yang-Lung Tai, 2011).

For T1 transformation

$$f(\omega_1,\omega_2) = 2g_1(\omega_1,\omega_2) \times g_2(\omega_1,\omega_2) - 1 \quad (4)$$

Where

$$g_1\,(\omega_1,\omega_2) = (\cos(\omega_1/2)\cos\,(\omega_2/2))^{2k} \quad (5)$$

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For T2 transformation

$$f(\omega_1,\omega_2) = g_1(\omega_1,\omega_2) \times f_2(\omega_1,\omega_2) - 1 \quad (7)$$

where

$$f_2(\omega_1,\omega_2) = cos^2(\omega_1/2) + cos^2(\omega_2/2) \quad (8)$$

Besides, the deployment of k-th order T1 and T2 transformations, permits the reduction in the order of the 1-D prototype filter by a factor √k and √(k + ½) respectively. Fig.2 and 3 show the frequency mapping of T1 and T2 transformations respectively.

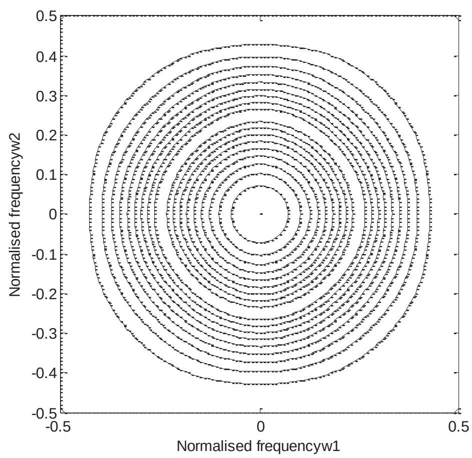

Fig.2 : Frequency mapping of T1 transformation.

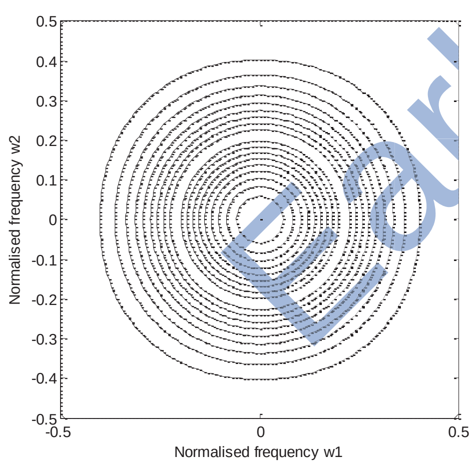

Fig.3 : Frequency mapping of T2 transformation.

IV. Gravitational Search Algorithm

Rashedi, proposed a new heuristic optimization algorithm named GSA in 2009. GSA is based on Newtonian Law of gravity and motion. GSA can be considered as an artificial world of masses, where every mass represents a solution of the problem. In this method, agents are considered as masses and every mass attract each other by the gravity force and this force causes a movement of all objects towards the object with heavier mass which is the optimum solution. Exploration and exploitation phase are carried out using the rules of gravity and mass interaction. The members of a population-based search algorithm undergo three steps in each iteration to realize the concepts of exploration and exploitation: self-adaptation, cooperation and competition. In the self-adaptation step, each member (agent) improves its performance. In the cooperation step, members collaborate with each other by information transferring. Finally, in the competition step, members compete to survive. The heavy masses which correspond to a good solution move more slowly than the lighter ones which guarantee the exploitation.

In GSA, each mass has four specifications: position in d-th dimension, inertial mass, active gravitational mass and passive gravitational mass. The position of a mass corresponds to the solution of the optimization problem and its gravitational and inertial masses are determined by the fitness function. Each mass represents a solution and the algorithm is navigated by properly adjusting gravitational and inertial masses. As the algorithm proceeds, the masses will be attracted by the heaviest mass which gives an optimum solution in the search space. GSA provides a good optimum solution for the problem in a higher dimensional search space.

V. Proposed Design of 1-D Multiplierless FRM Fir Filter

a) Problem Statement

The final objective of the work is to design a fully multiplierless 2D sharp filter. To this end, 1-D FRM

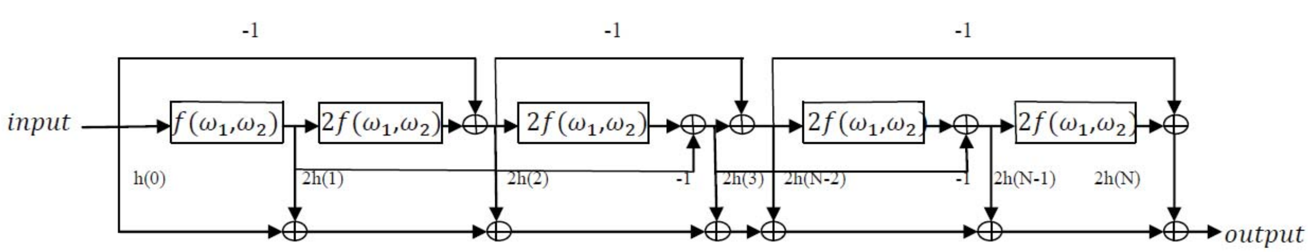

Fig.4 : Structure of 2-D filter.

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filter in the CSD space is mapped to the 2-D scenario using T1 and T2 transformations. First of all the 1-D continuous coefficient FRM filter is to be designed. The advantage of using FRM for the design of sharp FIR filter is the enormous saving in the computational complexity. If all subfilters have linear phase responses with Na and Nc either both even or both odd and (N-1)/M even, where N is the order of prototype filter and M is the interpolation factor, then the FRM filter has linear phase response These conditions stated in (Lu, W.S. Hinamoto 2003) have been used in our work to design the FRM filter with the linear phase. Once the band edges of the 1-D filter are obtained from the 2-D specifications, the continuous coefficient FRM filter is designed. The various sub-filters Ha(z), Hma(z) and Hmc(z) are designed using Parks- McClellan algorithm. The optimum interpolation factor is found in such a way that the total number of multipliers for the realization of the FRM filter is minimized. Direct rounding to the CSD space with restricted SPT terms cause the degradation of the frequency response specification of the 1-D FRM filter. This calls for the use of a discrete optimization. In this paper, we propose a new discrete optimization approach using the modified GSA. GSA has emerged as a good optimization tool and it offers relatively better performance compared to similar meta-heuristic algorithm. GSA is modified in such a way that during the exploitation and exploration phase, the candidate solution turns out to be integers. The design of 1-D FRM filter is modeled as a minimization problem as given in (M. Manuel, E. Elias, 2012). Here the objective function is defined as the approximation error as defined below

$$F(x) = \|H_d(\omega) - H(\omega,x)\|_2 \qquad (9)$$

where Hd(ω) represents the frequency response of the infinite precision FRM filter and H(ω,x) is the response of the optimized filter. x is obtained by concatenating the filter coefficients of the various sub-filters. To further reduce the computational complexity of the resulting discrete FRM filter, a constraint is also added to reduce the total number of SPT terms. The constraint is given by $n(x) \leq n_b$, where $n(x)$ denotes the average number of sub-filter coefficients, and nb represents the upper bound.

b) Encoding of Filter Coefficients

Since multipliers are the most power consuming elements in digital filters, multiplierless implementation of filters will lead to enormous saving in power and hardware complexity. Multiplierless implementation of linear phase FIR filters are possible by representing the filter coefficients in the CSD format. The redundancy in the multiplier coefficient representation caused by the non-unique nature of the SPT representation is removed by the use of CSD number system, which represents the multiplier coefficient values uniquely by reducing the number of non-zero digits. The multipliers can be represented by a series of shifts and additions or subtractions.

An infinite precision multiplier coefficient 'x'can be represented in CSD format as:

$$x = \sum_{i=1}^{B} b_i 2^{R-i} \qquad (10)$$

where B represents the wordlength of the CSD number and R represents a radix-point in the range 0< R<B. The CSD number obeys the following constraints

$$bi \in \{1,-1,0\}$$

$$bi \times bi+1 = 0$$

In our problem, the filter coefficients are encoded as signed integer indices of the look up table(LUT) locations of the nearest CSD equivalent as done in (M. Manuel, E. Elias, 2012). For this purpose, look up table is created as per the details provided in (M. Manuel, E. Elias, 2012). There are four fields for the LUT, namely CSD representation, decimal equivalent, index and the number of SPT terms. 2 bits are allocated for the integer part and 12 bits are provided for the fractional part. If a filter coefficient is negative, it is encoded as the negative of the index of its positive counterpart. Thus the candidate solution in the optimization problem turns out to be integers. In this work, a variable number of SPT terms have been used for obtaining the optimized filter. This allocation has a significant advantage compared to that using fixed terms (Lim, 1999). The look up table approach avoids the use of restoration algorithm (Ashrafzadeh, 1997) as needed in the ternary encoding of the CSD filter coefficients in the CSD space.

c) Proposed Modified GSA algorithm for the design of 1-D multiplierless FRM FIR filter

In our work, GSA has been tailor made to be suitable for the discrete optimization problem proposed. The various steps are briefed below

Step 1: Initialization of the agents

An agent is constituted by concatenating the CSD encoded filter coefficients of the sub-filters. Let N number of agents constitute a GSA system. Initialize the position of these agents by randomly perturbing the CSD encoded filter coefficients. Consider the position of the i-th agent

$$X_i = (x_i^1, x_i^2, \ldots\ldots, x_i^d, \ldots\ldots x_i^n) \qquad (11)$$

for i=1,2,…N. indicates the position of the i-th agent in the d-th dimension and n is the dimension of the search space. In our proposed design, each represents a typical encoded filter coefficient in the CSD space.

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Step 2 : Fitness evaluation and the best fitness computation

In our problem, the fitness function is identified with the approximation error as given by eq.(9). Compute the fitness for all agents in each iteration and also find the best and worst fitnesses at each iteration as given below. Since our optimization problem is a minimization type, we have

$$best(t) = \min_{j \in \{1,2,\ldots,N\}} fit_j(t) \tag{12}$$

$$worst(t) = \max_{j \in \{1,2,\ldots,N\}} fit_j(t) \tag{13}$$

Step 3 : Compute the gravitational constant G

Due to the effect of the decrease in the gravity, the true value of the gravitational constant depends on the age of the universe and there is a decrease in the gravitational constant G with the age. Gravitational constant G at each iteration 't'is computed by the following equation (R. Mansouri, 1999)

$$G(t) = G_0 e^{-(\frac{\alpha t}{T})} \tag{14}$$

G_0 is set to 100, α is taken as 20 and T is the total number of iterations.

Step 4 : Calculate the mass of the agents

For each filter coefficient, the gravitational and inertial masses are calculated at each iteration by the following equations. Consider $M_{ai} = M_{pi} = M_{ii} = M_i$, i=1,2,…N

$$m_i(t) = \frac{fit_i(t) - worst(t)}{best(t) - worst(t)} \tag{15}$$

$$M_i(t) = \frac{m_i(t)}{\sum_{j=1}^{N} m_j(t)} \tag{16}$$

where M_{ai}, M_{pi} and M_{ii} represents the active gravitational mass, passive gravitational mass and inertia mass respectively of the i-th agent (Rashedi, 2009).

Step 5 : Compute the acceleration of the agents

According to the law of motion, the acceleration of the i-th agent at time t in the d-th dimension is given by

$$a_i^{\,d}(t) = \frac{F_i^{\,d}(t)}{M_{ii}(t)} \tag{17}$$

$F_i^{\,d}(t)$ is the total force acting on agent 'i' in a dimension of d. To give a stochastic nature to the algorithm, it can be expressed as a randomly weighted sum of the d-th components of the forces exerted from other agents.

$$F_i^{\,d}(t) = \sum_{j=1, j\neq i}^{N} rand_j F_{ij}^{\,d}(t) \tag{18}$$

randj is a random number in the interval [0,1].

For controlling the exploration and exploitation, which decreases the performance of GSA, *'Kbest'* agents can be selected which attract each other. *'Kbest'* is the set of the first k agents with the best fitness value and the biggest mass. $F_{ij}^{d}(t)$ is the force acting on mass 'i' from mass 'j' at time t in the d-th dimension

$$F_{ij}^{\,d}(t) = G(t)\frac{M_{pi}(t) \times M_{ai}(t)}{R_{ij}(t) + \varepsilon}\left(x_i^{\,d}(t) - x_j^{\,d}(t)\right) \tag{19}$$

$R_{ij}(t)$ is the Euclidian distance between two agents i and j, ε is a small constant.

Step 6 : Update the velocity and position of the agents

The velocity of agent in the next iteration (t+1) can be represented as a fraction of its current velocity added to its acceleration. The new position and velocity of the agents can be calculated as

$$v_i^{\,d}(t+1) = rand_i \times v_i^{\,d}(t) + a_i^{\,d}(t) \tag{20}$$

$$x_i^{\,d}(t+1) = x_i^{\,d}(t) + v_i^{\,d}(t+1) \tag{21}$$

$$x_i^{\,d}(t+1) = \lfloor x_i^{\,d}(t+1) \rfloor \tag{22}$$

$\lfloor \quad \rfloor$ corresponds to the rounding to lower value.

This operation ensures that the new candidate solution turns out to be integers. Yet another modification is done to the new position so that any encoded filter coefficient falls within the boundary of the look up table. If $x_i^d(t+1) > v_{ub}$ then $x_i^d(t+1) = v_{ub}$ and if $x_i^d(t+1) < v_{lb}$ then $x_i^d(t+1) = v_{lb}$ where v_{ub} and v_{lb} represent the upper and lower bound of the CSD look up table respectively.

Step 7: Repeat step 2-6 until the iterations reach its limit. The best fitness is obtained and the position of the corresponding agent is the global solution. Obtain the best solution and it corresponds to the solution with the least approximation error. The best solution is decoded using the look up table to obtain the optimal FRM filter in the CSD space.

VI. Proposed Design of 2-D Multiplierless Filter

In this paper, the design of sharp wideband multiplierless 2-D linear phase filter is proposed. The block diagram of the proposed design is shown in Fig.5. From the specification of the required 2-D filter using inverse mapping , obtain the band-edges of the 1-D FRM filter. Then the continuous coefficient 1-D FRM filter

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is designed. The continuous coefficient FRM filter is converted to the CSD space using the proposed modified GSA algorithm as mentioned in section V.C. This 1- D sharp multiplierless filter is converted to the 2-D scenario using the frequency transformation named T1 and T2. T1 and T2 transformations provide an efficient method for the design of 2-D filter with circular contour and ensures better circularity as the order of the transformation increases. As the I-D linear phase FRM FIR filter is made multiplierless, the transformations result in a 2-D filter which is multiplier free. The realization of

a 2-D filter is given in Fig.4. In the realization h(n) represents the 1-D filter coefficient in the CSD space and f(ω_1, ω_2) corresponds to either the T1 or T2 transformation. Thus the realization is totally multiplierless.

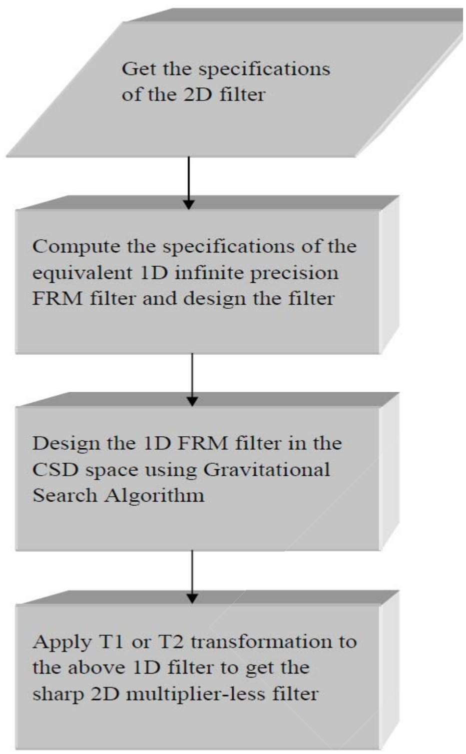


Fig.5 : Block diagram of the proposed design method

VII. Simulation Results

The proposed method was used to design a 2-D sharp wideband lowpass filter whose design specifications are given below:

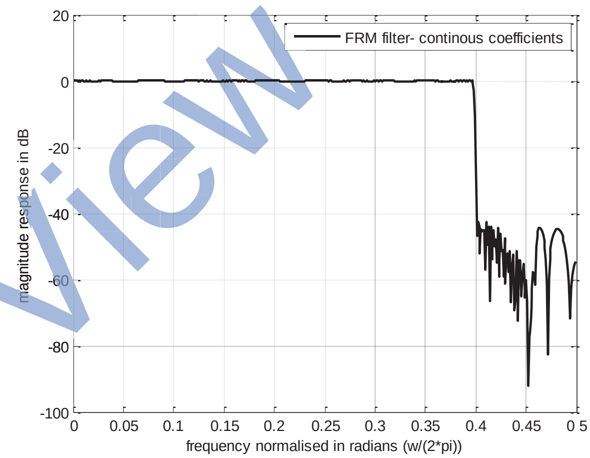
$$H(\omega_1,\omega_2,) = \begin{cases} 1 \pm \delta_p, & 0 \le \sqrt{\omega_1{}^2 + \omega_2{}^2} \le 0.8\pi \\ \pm\delta_s, & 0.81\pi \le \sqrt{\omega_1{}^2 + \omega_2{}^2} \le \pi \end{cases}$$

where δ_p=δ_s=0.01.

Case-1

By using T1 transformation with k=1, ω_p=0.8 and ω_s=0.81 . The bandedges of the 1D prototype filter to be designed are found as Ωp=0.7944 , Ωs= 0.8013 . Proposed GSA was used to design the 1-D multiplierless FRM filter and the maximum

number of iterations and the number of agents are taken to be 100 and 50 respectively. GA (Manoj, 2009) was also used for the above design for comparison purpose and parameters are Popkeep fraction= 0.2, MuteRate= 0.01, Elite count=5 and Iterations=100. Fig.6 shows the magnitude response of the continuous coefficient 1-D FRM filter, the magnitude response of the 1- D filter before and after GSA optimization are shown in Fig.7. The magnitude response and contour of the 2-D multiplierless lowpass filter using T1 transformation (k=1) is shown in Fig.8 and 9 respectively.



View

Fig.6 : Magnitude response of the continuous coefficient FRM filter

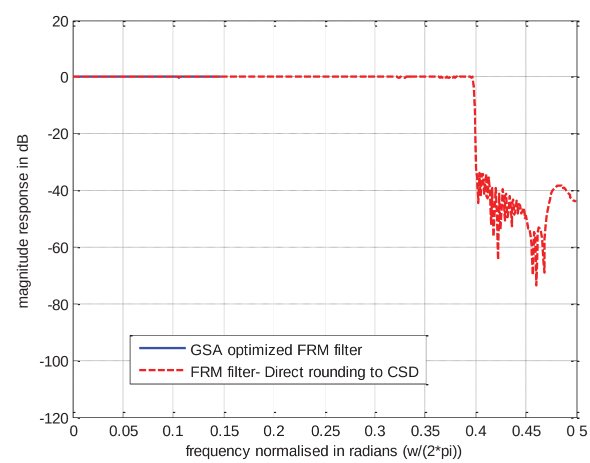


Fig.7 : Magnitude response of FRM filter direct rounding to CSD and GSA optimized

Comparison of the performance in terms of maximum passband ripple and minimum stopband attenuation are done in Table.1 for the two optimization techniques GSA and GA. It is found that our modified GSA gives better results than the GA.

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Table 1 : Performance Comparison of optimized FRM filter

Parameters of FRM filter	Infinite-precision	CSD rounded	GSA	GA
Maximum pass-band ripple	0.0904	0.1237	0.0939	0.168
Minimum stop-band attenuation	42.64	33.7	40.69	37.48

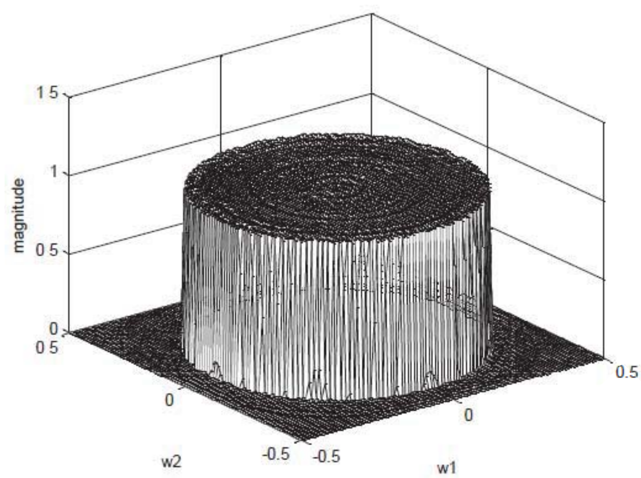

Fig.8 : Magnitude response of the 2-D low-pass filter using T1 transformation

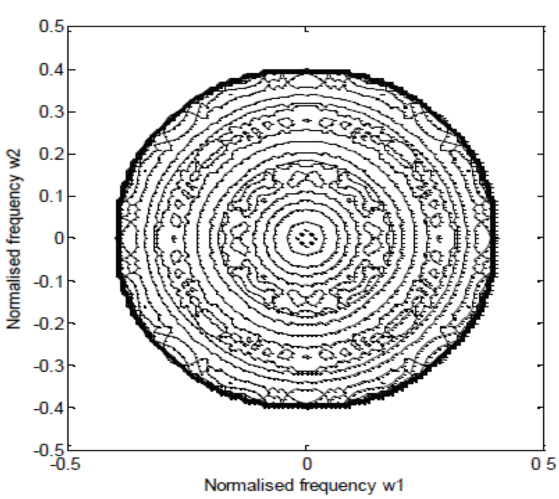

Fig.9 : Contour plot of the 2-D low-pass filter

Case-2

T2 transformation was also applied with the same specifications as above. The corresponding 1-D prototype filter specifications are Ωp= 0.8387π, Ωs= 0.8454π. Fig.10 shows the magnitude response of the continuous coefficient 1-D FRM filter. The magnitude response of the 1-D filter before and after optimization are shown in Fig.11. The magnitude response and contour of the 2-D multiplierless lowpass filter using T2 transformation (k=1) is shown in Fig.12 and 13 respectively. Performance comparison in terms of passband ripple and stopband attenuation for T2 transformation are done in Table. II.

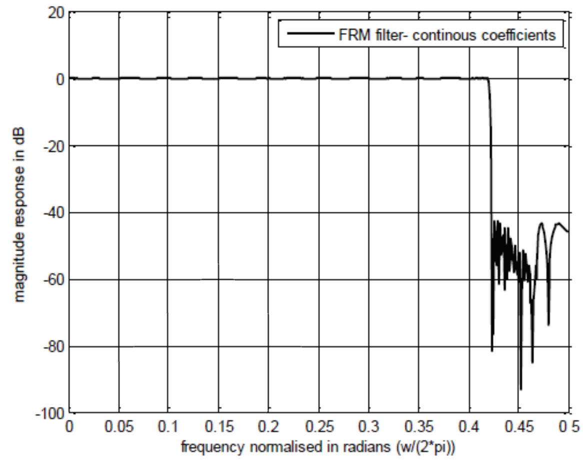

Fig.10 : Magnitude response of the continuous coefficient FRM filter

Table2: Performance Comparison of optimized FRM filter

Parameters of FRM filter	Infinite-precision	CSD rounded	GSA	GA
Maximum pass-band ripple	0.0992	0.1341	0.0982	1.1
Minimum stop-band attenuation	42.48	36.26	42.4	36.6

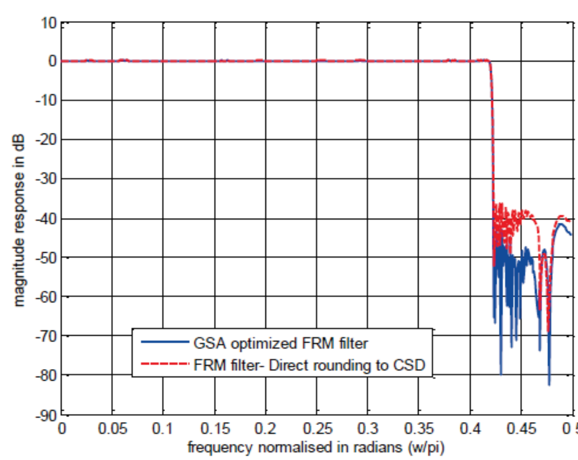

Fig.11 : Magnitude response of FRM filter direct rounding to CSD and GSA optimized

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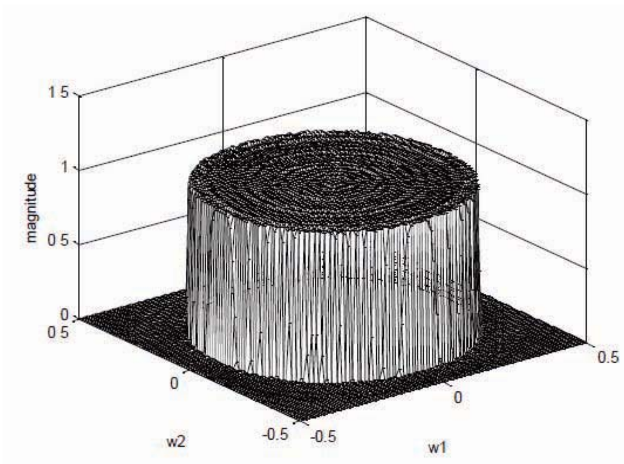

Fig. 12 : Magnitude response of the 2-D low-pass filter using T2 transformation

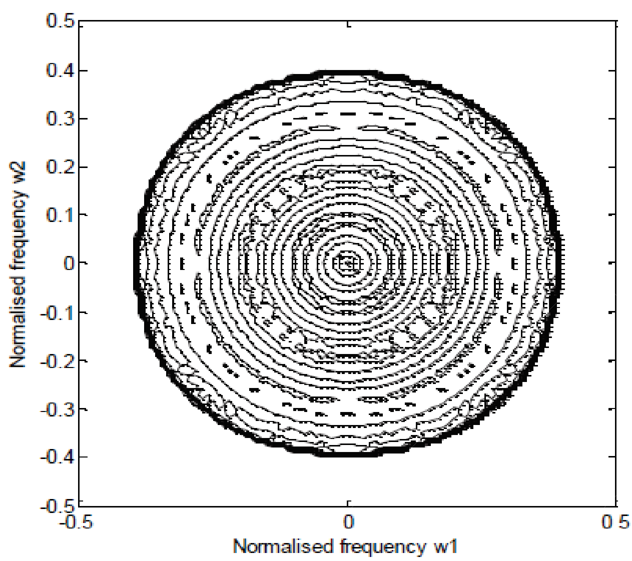

Fig. 13 : Contour plot of the 2-D low-pass filter

VIII. Conclusion

A new approach for the design of 2-D multiplierless sharp FIR filter is proposed. First of all a 1-D sharp FIR filter is designed using FRM technique. It results in a 1-D filter with sparse coefficients. The resulting 1-D filter is converted to the CSD space using a new discrete optimization. This optimization is based on a modified GSA. GSA has been modified in such a way that during the course of optimization the candidate solution turns out to be integers. This multiplierless 1-D filter is in-turn transformed to 2-D domain using the recently proposed T1 and T2 transformations. The resulting approach for the design of 2-D multiplierless filter is bestowed with the features of reduced computational complexity and computational time.

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Global Journal of researches in engineering
Electrical and electronics engineering
Volume 12 Issue 5 Version 1.0 April 2012
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Effect of Change in Dimensions of the Circular Antenna and Feedpoint on the Antenna Performance

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Abstract - Circular microstrip antennas have several interesting properties that makes it attractive in wireless applications. A circular microstrip antenna is designed in order to obtain the required parameter responses from 2.7 GHz to 2.9 GHz by using IE3D software based on the method of cavity model due to simplicity and ease of analysis. The circular microstrip antenna is fed by a coaxial probe (Teflon probe) and glass epoxy is used with the specified information include the dielectric constant of substrate (f_r = 4.2), the resonant frequency (f_r = 2.8 GHz) and substrate height (h=1.6mm). The circular microstrip antenna exhibits appropriate required parameters depend on the feedpoint position, size of the circular patch. A prototype of a circular microstrip antenna has been built and tested by spectrum analyzer. There is slight difference between the measured and simulated results caused by several factors that would be discussed in result part.

Keywords : *Circular microstrip antenna, coaxial probe.*

GJRE- F Classification : *FOR Code: 100501*

EFFECT OF CHANGE IN DIMENSIONS OF THE CIRCULAR ANTENNA AND FEEDPOINT ON THE ANTENNA PERFORMANCE

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Effect of Change in Dimensions of the Circular Antenna and Feedpoint on the Antenna Performance

Priyanka Sharma[α], Tarang Tripathi[α] & Dushyant Singh[σ]

Abstract - Circular microstrip antennas have several interesting properties that makes it attractive in wireless applications. A circular microstrip antenna is designed in order to obtain the required parameter responses from 2.7 GHz to 2.9 GHz by using IE3D software based on the method of cavity model due to simplicity and ease of analysis. The circular microstrip antenna is fed by a coaxial probe (Teflon probe) and glass epoxy is used with the specified information include the dielectric constant of substrate (ε_r = 4.2), the resonant frequency (f_r = 2.8 GHz) and substrate height (h=1.6mm). The circular microstrip antenna exhibits appropriate required parameters depend on the feedpoint position, size of the circular patch. A prototype of a circular microstrip antenna has been built and tested by spectrum analyzer. There is slight difference between the measured and simulated results caused by several factors that would be discussed in result part.

Keywords : Circular microstrip antenna, coaxial probe.

I. Introduction

A microstrip antenna in its simplest form consists of a radiating patch (of different shapes) on one side of a dielectric substrate and a ground plane on the other side. Microstrip antennas are used in communication systems due to simplicity in structure, conformability, low manufacturing cost, and very versatile in terms of resonant frequency, polarization, pattern and impedance at the particular patch shape and model [1].

The performance of the antenna is affected by the patch geometry, substrate properties and feed techniques [8]. In a circular microstrip antenna, the mode is supported by the circle shape on a substrate with height is very small compared to wavelength. Referring to the dimensions of the circular patch, only one degree freedom to control the radius, of the patch. This would not change the order of the modes but the absolute value of the resonant frequency [1].

In this paper, the circular microstrip antenna is being fed by a coaxial probe. The main advantage of this feed is that it can be placed at any desired location inside the patch to match with its input impedance. Impedance matching is necessary to ensure that the power transferred to the antenna is maximum [9].

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II. Methods of Analysis

There are three popular analytical techniques:

- The transmission line model
- The cavity model
- The MNM

In Transmission line model the microstrip radiator element is viewed as a transmission line resonator with no transverse field variations. In the cavity model, the region between the patch and the ground plane is treated as a cavity that is surrounded by magnetic walls around the periphery and by electric walls from the top and bottom sides. The MNM for analyzing the MSA is an extension of the cavity model. In this method, the electromagnetic fields underneath the patch and outside the patch are modelled separately [9].

To begin with the radius of the circular patch is calculated by using the cavity model method.

a) *Equations used*

Basically a circular microstrip antenna can only be analyzed via the cavity model and full-wave analysis. The cavity model also provides the method that the normalized fields within the dielectric substrate can be found more accurately and it does not radiate any power. According to the cavity model approach the radius of the antenna is [1]:

$$a = \frac{F}{\left\{1 + \frac{2h}{\pi\varepsilon_r F}\left[\ln\left(\frac{\pi F}{2h}\right) + 1.7726\right]\right\}^{\frac{1}{2}}}$$

Where

$$F = \frac{8.791 \times 10^9}{f_r\sqrt{\varepsilon_r}}$$

fr = resonant frequency

ε_r = dielectric constant

h = height of the substrate

Global Journal of Researches in Engineering (F) Volume XII Issue V Version I April 2012

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Using this expression the radius of the antenna was calculated to be 14.80mm. Simulation of the design was carried out by using IE3D software.

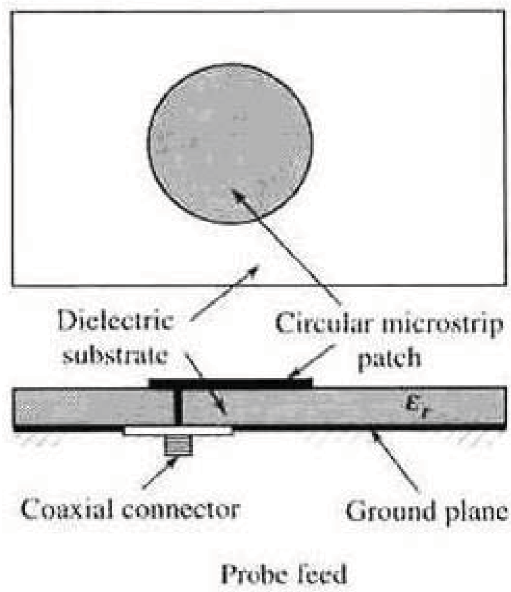
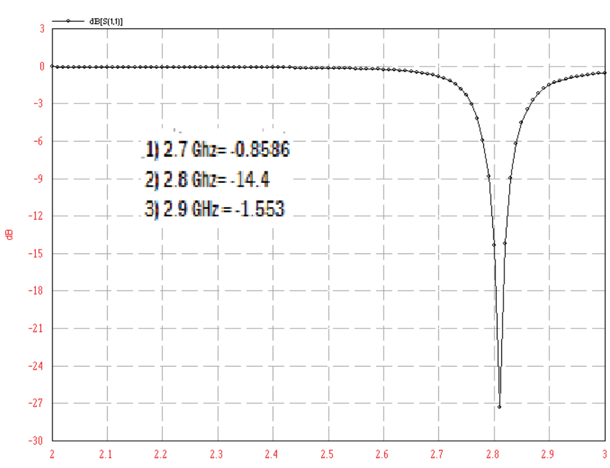


Figure 1 : Circular microstrip antenna configuration

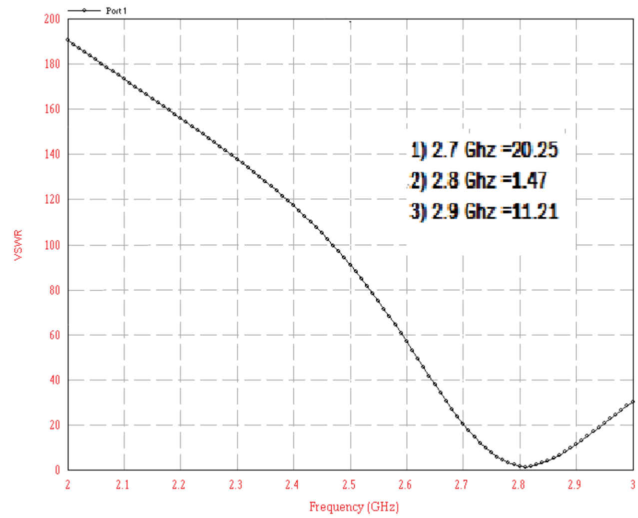
The flow of work then continues with the fabrication process. This process begins with the layout. After that, the etching process was carried out according to the dimensions from the simulation. Finally, the antenna was measured using a spectrum Analyzer to compare the simulation and the measurement results. Figure 1 shows the proposed circular antenna with the circular patch and the probe feed. This circular patch is printed on glass epoxy substrate having dielectric constant of 4.2 and thickness, h=1.6mm. The objective of the patch is to resonate at 2.8 GHz.

III. Results and Discussion

From the results of simulation it is found that the value of return loss is -14.4 dB & the value of VSWR is 1.47 at the resonant frequency of 2.8Ghz as shown in figure2(a) & (b) and the coordinates of feedpoint being (x=-2.6,y=-2.6).



(a)

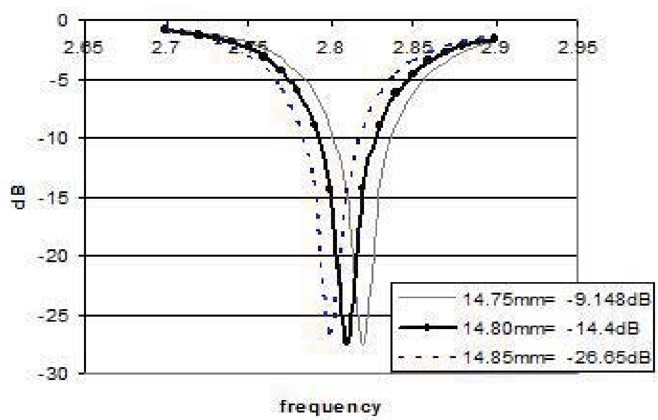


(b)

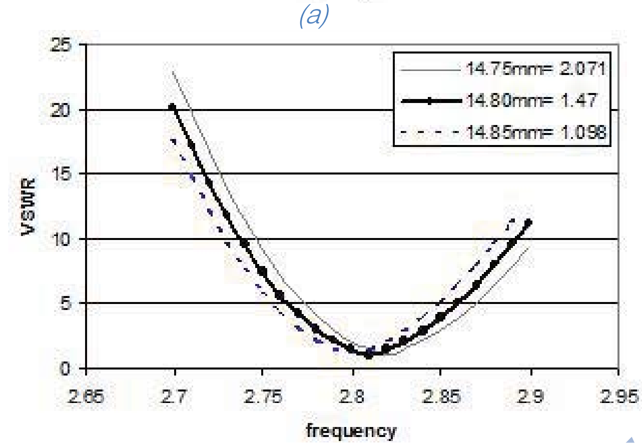
Figure 2 : Simulation result (a) Return loss and (b) VSWR

In this design the performance of the antenna in terms of the value of return loss & VSWR is dependent on two factors ; the feedpoint of the signal and the circle dimensions i.e the radius of the circle as calculated using the cavity model approach.

The figure 3 show a comparison by increasing and decreasing the radius of the circular antenna from the calculated values of 14.80mm and maintaining the feedpoint coordinate of (x=-2.6,y-2.6)constant.



(a)



(b)

Figure 3 : At different radius the values of (a) Return loss and (b) VSWR

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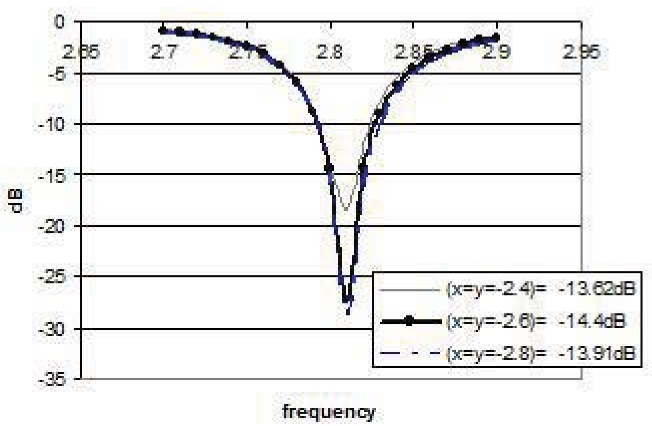
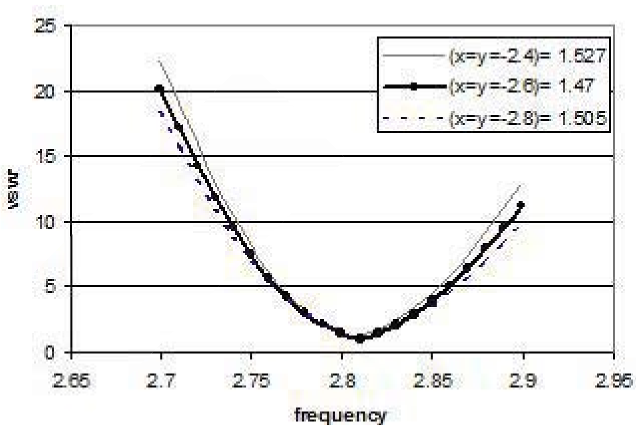
As the radius of the antenna is increased to 14.85mm while keeping feedpoint coordinates constant ,the value of the return loss decreases to -26.65 dB. Further higher values of the radius are chosen to observe the response of the antenna with the increase in the radius. Since the return loss is due to the mismatched load so the lowest of the return loss is required for the design. The VSWR value also changes. It decreases from 1.47 to 1.098 with the increase in radius from 14.80mm to 14.85 mm this shows that at the load the reflection coefficient is high.

As the radius is decreased from the original value of 14.80mm to 14.75mm, the value of return loss increases to -9.148 dB and the value of VSWR is increased to 2.071. The obtained results indicate that the performance of the antenna in terms of return loss and VSWR is satisfactory when increasing the radius of the circular patch keeping feedpoint constant but the decrease in radius leads to an unsatisfactory result.

The figure 4 shows comparison of the values of return loss and VSWR obtained by varying the feedpoint coordinates from (x=-2.6,y=-2.6) to(x=-2.4,y=-2.4) and (x=-2.8,y=-2.8) while maintaining the radius constant.



(a)

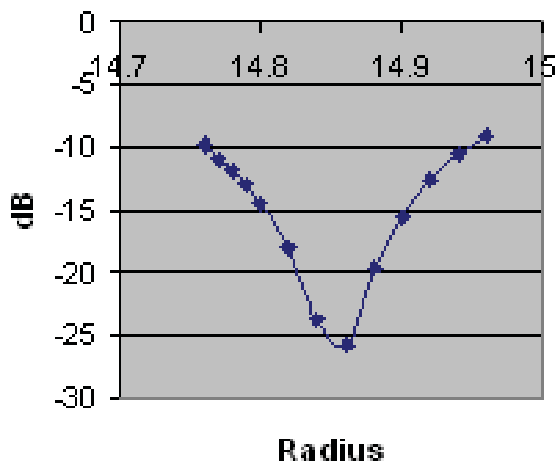


(b)

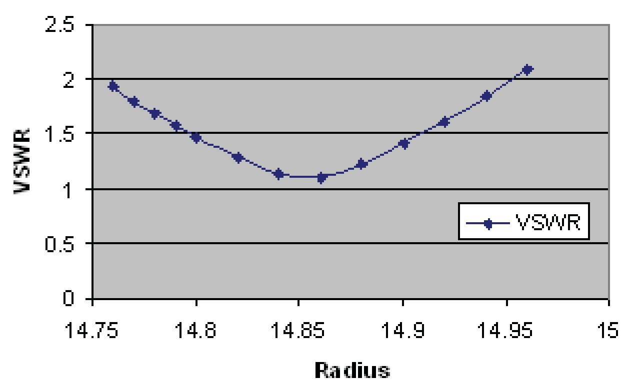
Figure 4 : At different feed points the value of (a) Return loss and (b) VSWR

As the feedpoint coordinates are changed from x=-2.6,y=-2.6 to x=-2.4 ,y=-2.4 ,the value of return loss increases from -14.4 db to -13.62 db and the value of VSWR increases from 1.47 to 1.527. Similarly if the feedpoint coordinates are changed to x=-2.8,y=-2.8 the value of return loss increases to -13.91 dB and VSWR increases to 1.504. So from the result obtained it can be inferred that the variation in the feeedpoint coordinate from the original coordinates leads to an unsatisfactory antenna performance.

Figure 5 shows the trend in the performance of the antenna in terms of the return loss & VSWR values for various other values of the patch radius. Figure 5(a) shows the trend in the return loss for various values of radius patch & figure 5(b) shows the value of VSWR for different radius value keeping the feedpoint coordinates constant at x = y = -2.6.



(a)



(b)

Figure 5 : At various radius the values of (a)Return loss (b)VSWR

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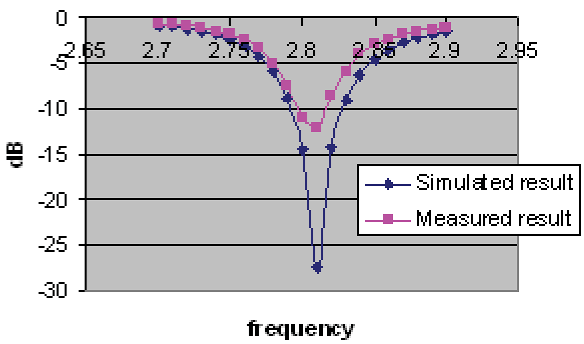
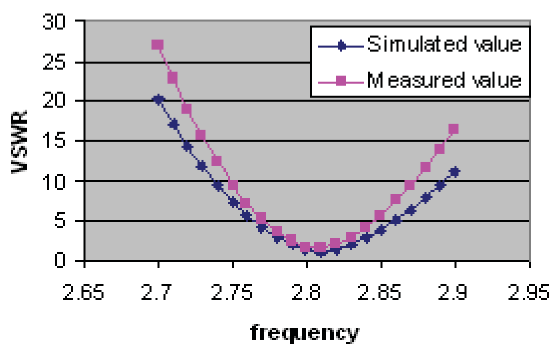
Now the antenna performance is measured using spectrum analyzer. From the results of the measurement of the values of return loss and VSWR it was observed that the values measured were slightly different from the values obtained from simulation. According to the measured result the return loss and VSWR were -10.94 & 1.792 respectively.

Figure 6 show the measured & simulated result on a single graph and the table 1 gives the value of measured & simulated results.



(a)



(b)

Figure 6 : Comparison between Simulated and measured Result for (a) return loss (b) VSWR

Table 1 : Comparison between simulated and Measured Results at the resonant frequency

Parameter	Simulted	Measured
Return loss	-14.4dB	-10.94dB
VSWR	1.47	1.792

There are several factors responsible for the difference between the simulated & practically obtained values. During fabrication, the improper handling can influence the obtained result such as during etching process; the circular patch might not be precisely obtained, since at higher frequency the MSA are very sensitive to diemensions of the patch.

The difference in the result could be due to parasitic components in the screw that are used to fix the antenna. Here the screws act as capacitor that exhibit fringing effect between the patch and ground plane. Due to this effect the amount of signal transmitted to air reduces .so there must be sufficient distance, larger than $\lambda/4$, between the patch & screws to avoid this problem.The skin effect due to solder leads used to connect the probe to the patch is another reason for the mismatch in the simulated and practical result.

Another reason is the loss due to the substrate properties. A higher dielectric loss will result in worst return loss and VSWR. So a good substrate with low value of loss must be chosen to prevent some loss in the antenna [5].

IV. Conclusion

Design of circular ring microstrip antennas has been investigated via the cavity model. A circular microstrip antenna with a probe feed is obtained and the required parameters at the frequency of 2.7 GHz to 2.9 GHz have been investigated successfully. From the simulated results it is found that the return loss is -14.4dB and VSWR value is 1.47 and from the measured values it is found that the return loss is -10.94dB and VSWR is 1.792 at the resonant frequency of 2.8 Ghz The microstrip antenna performance can be upgraded concerning the feed type, the size of the patch and the substrate used.

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8. Use the Internet for help: An excellent start for your paper can be by using the Google. It is an excellent search engine, where you can have your doubts resolved. You may also read some answers for the frequent question how to write my research paper or find model research paper. From the internet library you can download books. If you have all required books make important reading selecting and analyzing the specified information. Then put together research paper sketch out.

9. Use and get big pictures: Always use encyclopedias, Wikipedia to get pictures so that you can go into the depth.

10. Bookmarks are useful: When you read any book or magazine, you generally use bookmarks, right! It is a good habit, which helps to not to lose your continuity. You should always use bookmarks while searching on Internet also, which will make your search easier.

11. Revise what you wrote: When you write anything, always read it, summarize it and then finalize it.

12. Make all efforts: Make all efforts to mention what you are going to write in your paper. That means always have a good start. Try to mention everything in introduction, that what is the need of a particular research paper. Polish your work by good skill of writing and always give an evaluator, what he wants.

13. Have backups: When you are going to do any important thing like making research paper, you should always have backup copies of it either in your computer or in paper. This will help you to not to lose any of your important.

14. Produce good diagrams of your own: Always try to include good charts or diagrams in your paper to improve quality. Using several and unnecessary diagrams will degrade the quality of your paper by creating "hotchpotch." So always, try to make and include those diagrams, which are made by your own to improve readability and understandability of your paper.

15. Use of direct quotes: When you do research relevant to literature, history or current affairs then use of quotes become essential but if study is relevant to science then use of quotes is not preferable.

16. Use proper verb tense: Use proper verb tenses in your paper. Use past tense, to present those events that happened. Use present tense to indicate events that are going on. Use future tense to indicate future happening events. Use of improper and wrong tenses will confuse the evaluator. Avoid the sentences that are incomplete.

17. Never use online paper: If you are getting any paper on Internet, then never use it as your research paper because it might be possible that evaluator has already seen it or maybe it is outdated version.

18. **Pick a good study spot:** To do your research studies always try to pick a spot, which is quiet. Every spot is not for studies. Spot that suits you choose it and proceed further.

19. Know what you know: Always try to know, what you know by making objectives. Else, you will be confused and cannot achieve your target.

20. Use good quality grammar: Always use a good quality grammar and use words that will throw positive impact on evaluator. Use of good quality grammar does not mean to use tough words, that for each word the evaluator has to go through dictionary. Do not start sentence with a conjunction. Do not fragment sentences. Eliminate one-word sentences. Ignore passive voice. Do not ever use a big word when a diminutive one would suffice. Verbs have to be in agreement with their subjects. Prepositions are not expressions to finish sentences with. It is incorrect to ever divide an infinitive. Avoid clichés like the disease. Also, always shun irritating alliteration. Use language that is simple and straight forward. put together a neat summary.

21. Arrangement of information: Each section of the main body should start with an opening sentence and there should be a changeover at the end of the section. Give only valid and powerful arguments to your topic. You may also maintain your arguments with records.

22. Never start in last minute: Always start at right time and give enough time to research work. Leaving everything to the last minute will degrade your paper and spoil your work.

23. Multitasking in research is not good: Doing several things at the same time proves bad habit in case of research activity. Research is an area, where everything has a particular time slot. Divide your research work in parts and do particular part in particular time slot.

24. Never copy others' work: Never copy others' work and give it your name because if evaluator has seen it anywhere you will be in trouble.

25. Take proper rest and food: No matter how many hours you spend for your research activity, if you are not taking care of your health then all your efforts will be in vain. For a quality research, study is must, and this can be done by taking proper rest and food.

26. Go for seminars: Attend seminars if the topic is relevant to your research area. Utilize all your resources.

27. Refresh your mind after intervals: Try to give rest to your mind by listening to soft music or by sleeping in intervals. This will also improve your memory.

28. Make colleagues: Always try to make colleagues. No matter how sharper or intelligent you are, if you make colleagues you can have several ideas, which will be helpful for your research.

29. **Think technically:** Always think technically. If anything happens, then search its reasons, its benefits, and demerits.

30. Think and then print: When you will go to print your paper, notice that tables are not be split, headings are not detached from their descriptions, and page sequence is maintained.

31. Adding unnecessary information: Do not add unnecessary information, like, I have used MS Excel to draw graph. Do not add irrelevant and inappropriate material. These all will create superfluous. Foreign terminology and phrases are not apropos. One should NEVER take a broad view. Analogy in script is like feathers on a snake. Not at all use a large word when a very small one would be sufficient. Use words properly, regardless of how others use them. Remove quotations. Puns are for kids, not grunt readers. Amplification is a billion times of inferior quality than sarcasm.

32. Never oversimplify everything: To add material in your research paper, never go for oversimplification. This will definitely irritate the evaluator. Be more or less specific. Also too, by no means, ever use rhythmic redundancies. Contractions aren't essential and shouldn't be there used. Comparisons are as terrible as clichés. Give up ampersands and abbreviations, and so on. Remove commas, that are, not necessary. Parenthetical words however should be together with this in commas. Understatement is all the time the complete best way to put onward earth-shaking thoughts. Give a detailed literary review.

33. Report concluded results: Use concluded results. From raw data, filter the results and then conclude your studies based on measurements and observations taken. Significant figures and appropriate number of decimal places should be used. Parenthetical remarks are prohibitive. Proofread carefully at final stage. In the end give outline to your arguments. Spot out perspectives of further study of this subject. Justify your conclusion by at the bottom of them with sufficient justifications and examples.

34. After conclusion: Once you have concluded your research, the next most important step is to present your findings. Presentation is extremely important as it is the definite medium though which your research is going to be in print to the rest of the crowd. Care should be taken to categorize your thoughts well and present them in a logical and neat manner. A good quality research paper format is essential because it serves to highlight your research paper and bring to light all necessary aspects in your research.

Informal Guidelines of Research Paper Writing

Key points to remember:

- Submit all work in its final form.
- Write your paper in the form, which is presented in the guidelines using the template.
- Please note the criterion for grading the final paper by peer-reviewers.

Final Points:

A purpose of organizing a research paper is to let people to interpret your effort selectively. The journal requires the following sections, submitted in the order listed, each section to start on a new page.

The introduction will be compiled from reference matter and will reflect the design processes or outline of basis that direct you to make study. As you will carry out the process of study, the method and process section will be constructed as like that. The result segment will show related statistics in nearly sequential order and will direct the reviewers next to the similar intellectual paths throughout the data that you took to carry out your study. The discussion section will provide understanding of the data and projections as to the implication of the results. The use of good quality references all through the paper will give the effort trustworthiness by representing an alertness of prior workings.

Writing a research paper is not an easy job no matter how trouble-free the actual research or concept. Practice, excellent preparation, and controlled record keeping are the only means to make straightforward the progression.

General style:

Specific editorial column necessities for compliance of a manuscript will always take over from directions in these general guidelines.

To make a paper clear

· Adhere to recommended page limits

Mistakes to evade

- Insertion a title at the foot of a page with the subsequent text on the next page

- Separating a table/chart or figure - impound each figure/table to a single page
- Submitting a manuscript with pages out of sequence

In every sections of your document

· Use standard writing style including articles ("a", "the," etc.)

· Keep on paying attention on the research topic of the paper

· Use paragraphs to split each significant point (excluding for the abstract)

· Align the primary line of each section

· Present your points in sound order

· Use present tense to report well accepted

· Use past tense to describe specific results

· Shun familiar wording, don't address the reviewer directly, and don't use slang, slang language, or superlatives

· Shun use of extra pictures - include only those figures essential to presenting results

Title Page:

Choose a revealing title. It should be short. It should not have non-standard acronyms or abbreviations. It should not exceed two printed lines. It should include the name(s) and address (es) of all authors.

Abstract:

The summary should be two hundred words or less. It should briefly and clearly explain the key findings reported in the manuscript--must have precise statistics. It should not have abnormal acronyms or abbreviations. It should be logical in itself. Shun citing references at this point.

An abstract is a brief distinct paragraph summary of finished work or work in development. In a minute or less a reviewer can be taught the foundation behind the study, common approach to the problem, relevant results, and significant conclusions or new questions.

Write your summary when your paper is completed because how can you write the summary of anything which is not yet written? Wealth of terminology is very essential in abstract. Yet, use comprehensive sentences and do not let go readability for briefness. You can maintain it succinct by phrasing sentences so that they provide more than lone rationale. The author can at this moment go straight to

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shortening the outcome. Sum up the study, with the subsequent elements in any summary. Try to maintain the initial two items to no more than one ruling each.

- Reason of the study - theory, overall issue, purpose
- Fundamental goal
- To the point depiction of the research
- Consequences, including definite statistics - if the consequences are quantitative in nature, account quantitative data; results of any numerical analysis should be reported
- Significant conclusions or questions that track from the research(es)

Approach:

- Single section, and succinct
- As a outline of job done, it is always written in past tense
- A conceptual should situate on its own, and not submit to any other part of the paper such as a form or table
- Center on shortening results - bound background information to a verdict or two, if completely necessary
- What you account in an conceptual must be regular with what you reported in the manuscript
- Exact spelling, clearness of sentences and phrases, and appropriate reporting of quantities (proper units, important statistics) are just as significant in an abstract as they are anywhere else

Introduction:

The **Introduction** should "introduce" the manuscript. The reviewer should be presented with sufficient background information to be capable to comprehend and calculate the purpose of your study without having to submit to other works. The basis for the study should be offered. Give most important references but shun difficult to make a comprehensive appraisal of the topic. In the introduction, describe the problem visibly. If the problem is not acknowledged in a logical, reasonable way, the reviewer will have no attention in your result. Speak in common terms about techniques used to explain the problem, if needed, but do not present any particulars about the protocols here. Following approach can create a valuable beginning:

- Explain the value (significance) of the study
- Shield the model - why did you employ this particular system or method? What is its compensation? You strength remark on its appropriateness from a abstract point of vision as well as point out sensible reasons for using it.
- Present a justification. Status your particular theory (es) or aim(s), and describe the logic that led you to choose them.
- Very for a short time explain the tentative propose and how it skilled the declared objectives.

Approach:

- Use past tense except for when referring to recognized facts. After all, the manuscript will be submitted after the entire job is done.
- Sort out your thoughts; manufacture one key point with every section. If you make the four points listed above, you will need a least of four paragraphs.
- Present surroundings information only as desirable in order hold up a situation. The reviewer does not desire to read the whole thing you know about a topic.
- Shape the theory/purpose specifically - do not take a broad view.
- As always, give awareness to spelling, simplicity and correctness of sentences and phrases.

Procedures (Methods and Materials):

This part is supposed to be the easiest to carve if you have good skills. A sound written Procedures segment allows a capable scientist to replacement your results. Present precise information about your supplies. The suppliers and clarity of reagents can be helpful bits of information. Present methods in sequential order but linked methodologies can be grouped as a segment. Be concise when relating the protocols. Attempt for the least amount of information that would permit another capable scientist to spare your outcome but be cautious that vital information is integrated. The use of subheadings is suggested and ought to be synchronized with the results section. When a technique is used that has been well described in another object, mention the specific item describing a way but draw the basic principle while stating the situation. The purpose is to text all particular resources and broad procedures, so that another person may use some or all of the methods in one more study or referee the scientific value of your work. It is not to be a step by step report of the whole thing you did, nor is a methods section a set of orders.

Materials:

- Explain materials individually only if the study is so complex that it saves liberty this way.
- Embrace particular materials, and any tools or provisions that are not frequently found in laboratories.
- Do not take in frequently found.
- If use of a definite type of tools.
- Materials may be reported in a part section or else they may be recognized along with your measures.

Methods:

- Report the method (not particulars of each process that engaged the same methodology)
- Describe the method entirely
- To be succinct, present methods under headings dedicated to specific dealings or groups of measures
- Simplify - details how procedures were completed not how they were exclusively performed on a particular day.
- If well known procedures were used, account the procedure by name, possibly with reference, and that's all.

Approach:

- It is embarrassed or not possible to use vigorous voice when documenting methods with no using first person, which would focus the reviewer's interest on the researcher rather than the job. As a result when script up the methods most authors use third person passive voice.
- Use standard style in this and in every other part of the paper - avoid familiar lists, and use full sentences.

What to keep away from

- Resources and methods are not a set of information.
- Skip all descriptive information and surroundings - save it for the argument.
- Leave out information that is immaterial to a third party.

Results:

The principle of a results segment is to present and demonstrate your conclusion. Create this part a entirely objective details of the outcome, and save all understanding for the discussion.

The page length of this segment is set by the sum and types of data to be reported. Carry on to be to the point, by means of statistics and tables, if suitable, to present consequences most efficiently.You must obviously differentiate material that would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matter should not be submitted at all except requested by the instructor.

Content

- Sum up your conclusion in text and demonstrate them, if suitable, with figures and tables.
- In manuscript, explain each of your consequences, point the reader to remarks that are most appropriate.
- Present a background, such as by describing the question that was addressed by creation an exacting study.
- Explain results of control experiments and comprise remarks that are not accessible in a prescribed figure or table, if appropriate.
- Examine your data, then prepare the analyzed (transformed) data in the form of a figure (graph), table, or in manuscript form.

What to stay away from

- Do not discuss or infer your outcome, report surroundings information, or try to explain anything.
- Not at all, take in raw data or intermediate calculations in a research manuscript.

- Do not present the similar data more than once.
- Manuscript should complement any figures or tables, not duplicate the identical information.
- Never confuse figures with tables - there is a difference.

Approach

- As forever, use past tense when you submit to your results, and put the whole thing in a reasonable order.
- Put figures and tables, appropriately numbered, in order at the end of the report
- If you desire, you may place your figures and tables properly within the text of your results part.

Figures and tables

- If you put figures and tables at the end of the details, make certain that they are visibly distinguished from any attach appendix materials, such as raw facts
- Despite of position, each figure must be numbered one after the other and complete with subtitle
- In spite of position, each table must be titled, numbered one after the other and complete with heading
- All figure and table must be adequately complete that it could situate on its own, divide from text

Discussion:

The Discussion is expected the trickiest segment to write and describe. A lot of papers submitted for journal are discarded based on problems with the Discussion. There is no head of state for how long a argument should be. Position your understanding of the outcome visibly to lead the reviewer through your conclusions, and then finish the paper with a summing up of the implication of the study. The purpose here is to offer an understanding of your results and hold up for all of your conclusions, using facts from your research and generally accepted information, if suitable. The implication of result should be visibly described. Infer your data in the conversation in suitable depth. This means that when you clarify an observable fact you must explain mechanisms that may account for the observation. If your results vary from your prospect, make clear why that may have happened. If your results agree, then explain the theory that the proof supported. It is never suitable to just state that the data approved with prospect, and let it drop at that.

- Make a decision if each premise is supported, discarded, or if you cannot make a conclusion with assurance. Do not just dismiss a study or part of a study as "uncertain."
- Research papers are not acknowledged if the work is imperfect. Draw what conclusions you can based upon the results that you have, and take care of the study as a finished work
- You may propose future guidelines, such as how the experiment might be personalized to accomplish a new idea.
- Give details all of your remarks as much as possible, focus on mechanisms.
- Make a decision if the tentative design sufficiently addressed the theory, and whether or not it was correctly restricted.
- Try to present substitute explanations if sensible alternatives be present.
- One research will not counter an overall question, so maintain the large picture in mind, where do you go next? The best studies unlock new avenues of study. What questions remain?
- Recommendations for detailed papers will offer supplementary suggestions.

Approach:

- When you refer to information, differentiate data generated by your own studies from available information
- Submit to work done by specific persons (including you) in past tense.
- Submit to generally acknowledged facts and main beliefs in present tense.

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Segment Draft and Final Research Paper: You have to strictly follow the template of research paper. If it is not done your paper may get rejected.

- The **major constraint** is that you must independently make all content, tables, graphs, and facts that are offered in the paper. You must write each part of the paper wholly on your own. The Peer-reviewers need to identify your own perceptive of the concepts in your own terms. NEVER extract straight from any foundation, and never rephrase someone else's analysis.

- Do not give permission to anyone else to "PROOFREAD" your manuscript.

- Methods to avoid Plagiarism is applied by us on every paper, if found guilty, you will be blacklisted by all of our collaborated research groups, your institution will be informed for this and strict legal actions will be taken immediately.)
- To guard yourself and others from possible illegal use please do not permit anyone right to use to your paper and files.

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Topics	Grades		
	A-B	**C-D**	**E-F**
Abstract	Clear and concise with appropriate content, Correct format. 200 words or below	Unclear summary and no specific data, Incorrect form Above 200 words	No specific data with ambiguous information Above 250 words
Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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ISSN 9755861

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