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Keywords : *capacitor clamped DC-DC boost converter; flying capacitor multilevel inverter (FCMLI); phase disposition – pulse width modulation (PD-PWM); photovoltaic (PV); total harmonic distortion (THD).*

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An Investigation Study of Total Harmonic Distortion in a Flying Capacitor Multilevel Inverter With / Without Closed – Loop Feedback Schemes

Shanmuga Priyan.S[α] & Dr. Ramani.K[σ]

Abstract - This paper focuses on the investigation study of Total Harmonic Distortion (THD) in a seven-level Flying Capacitor Multilevel Inverter (FCMLI) with / without closed-loop feedback schemes. For that, a closed-loop model is designed for the existing FCMLI through this paper. Conventionally full bridge and half bridge inverter configurations are used for certain applications where DC-AC conversion is needed. But the main drawbacks of these inverters are high harmonic content and used only for limited power applications. In order to overcome this, a novel approach called closed-loop FCMLI will be proposed, which significantly increases the level number of the output waveform and thereby dramatically reduces the low-order harmonics and THD. The proposed system consists of a DC–DC power converter and a DC–AC multilevel inverter. In order to achieve low cost, easy control, high efficiency, and high reliability, a capacitor clamped DC–DC boost converter using minimal devices is introduced to interface the low-voltage Photovoltaic (PV) module. In this paper, a Phase Disposition – Pulse Width Modulation (PD-PWM) technique, applicable for proposed FCMLI is presented. With the use of multilevel inverter, resolution is increased and also the harmonics is highly reduced. The proposed seven level FCMLI not only achieves high power ratings, but also enables the use of renewable energy sources in an efficient manner. In order to justify the merits of the proposed system, it is interfaced with the single phase lamp load and analysed through simulation investigations.

Keywords : capacitor clamped DC-DC boost converter; flying capacitor multilevel inverter (FCMLI); phase disposition – pulse width modulation (PD-PWM); photovoltaic (PV); total harmonic distortion (THD).

I. Introduction

In Recent years, there has been an increasing interest in electrical power generation from renewable-energy sources, such as photovoltaic (PV) or wind-power systems [1], [2]. The benefits of power generation from these sources are widely accepted. They are essentially inexhaustible and environmentally friendly. Among the different renewable-energy sources possible to obtain electricity, solar energy has been one of the most active research areas in the past decades, both for grid-connected and stand-alone applications [3]–[4].

Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveform having large number of steps. The steps being supplied from different DC levels supported by series connected batteries or capacitors. The unique structure of multi-level inverter allows them to reach high voltages and therefore lower voltage rating device can be used. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave. It can be easily understood that as motor steps are included in the waveform the harmonic distortion of the output wave decrease, approaching zero as the number of levels approaches infinity.

Hence Multi- level inverters inverters offer a better choice at the high power end because the high volt- ampere ratings are possible with these inverters without the problems of high dv/dt and the other associated ones [5].

Nowadays different topologies have been reported for multi-level inverters. They are named as neutral point clamped (diode-clamped) inverter, flying capacitor (capacitor-clamped) inverter and cascaded multi-cell with separated dc source inverter [6]. Among them, the FCMLI does not require isolated DC sides and additional clamping diodes, the snubberless operation is possible and it is easy to be expanded to the multi-level. The FCMLI offers a great advantage with respect to the availability of voltage redundancies.

This inverter uses capacitors to limit the voltage of the power devices. They are defined as different combinations of capacitors allowing the charging or discharging of the individual flying capacitors in order to produce the same phase leg voltage. This advantage provides the special opportunity for controlling the individual voltage on flying capacitors [6]-[7]. Many studies have shown that under certain conditions, a simple open loop control guarantees natural balancing of the flying capacitor.

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In this paper, Proportional-Integral-Derivative (PID) controllers based closed loop system for seven level flying capacitor multilevel inverter and for capacitor clamped DC-DC boost converter have been proposed. This scheme maintains the output voltage stability, reducing the harmonic content in the output there by improving the overall system performance. This paper has been designed using a seven level flying capacitor multilevel inverter with the appropriate closed loop schemes there by THD can be significantly reduced which is confirmed through simulation investigation.

II. Proposed Topology of Closed Loop System

a) Architecture of Proposed System

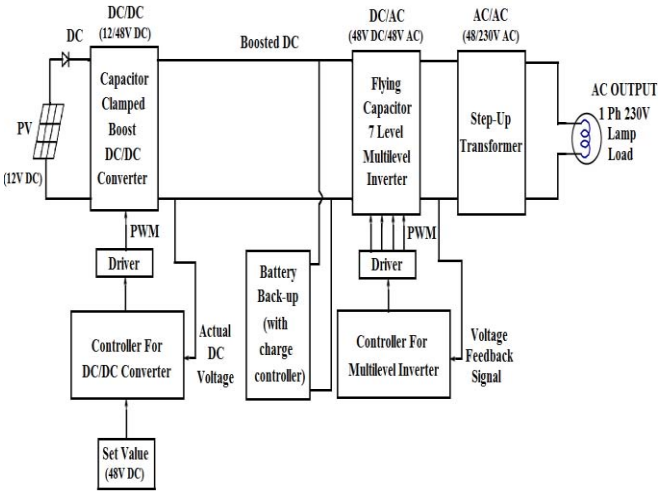

Figure 1 : Overall Block Diagram of Proposed System

For this proposed topology, DC input to the system is a solar energy which is harvested from the Sun based on the irradiation and insolation level. In this system a single stand-alone PV module of 12V capacity is used to obtain the DC voltage. Then this obtained DC voltage is given as the input to the Capacitor Clamped DC-DC Boost Converter. By the boost DC-DC converter topology, the 12V DC is boosted into 48V DC.

In order to maintain the constant DC voltage from the boost converter, a closed loop block is designed in which the actual DC voltage is compared with the 48V DC set value. Based on the error signal from the comparator, the PID controller produces the control signal to the PWM pulse generator block.

Then based upon the specified switching frequency of MOSFET, switching pulses are given to the single switch in the boost converter. Then the boosted DC voltage is given as the input to the seven level FCMLI which is used for 48V DC to 48V AC conversion.

For controlling the FCMLI, a closed loop block is designed which consists of voltage measurement, voltage controller - PID controller and Sin generator block. With the help of these blocks, a closed loop design is achieved for proposed FCMLI. Then this low voltage AC signal of 48V AC is given to the step-up transformer for stepping up the voltage level to 230V AC. Finally a resistive load – single phase lamp load is connected across the 230V AC output terminals.

b) System Composition

The described system in this paper is a standalone system which consisting of the following individual systems-:

i. For generating the DC voltage signal, a suitable stand-alone PV module is used.
ii. For boosting up the generated DC voltage, an appropriate Capacitor Clamped DC-DC boost converter is used.
iii. For maintaining the constant DC output from boost converter, a closed loop controller is used for DC-DC converter.
iv. For converting the boosted DC voltage into appropriate AC voltage, a FCMLI is used.
v. For improving the performance of MLI, a closed loop controller is used for FCMLI.
vi. For stepping up the generated AC voltage from MLI, a suitable step-up transformer is used.
vii. For connecting the developed system to the resistive load, a single phase lamp load is used.

c) System Specification

Table 1 : Technical Specification of a Proposed System

System Stages	Technical Specification
DC Input	PV Module – 12V DC
DC - DC Conversion	Capacitor Clamped DC-DC Boost Converter (12/48V DC)
DC Storage	Battery back-up of 48V – Series connection of 4 batteries (12V each)
DC - AC Conversion	Seven Level FCMLI 48V DC/48V AC Stepped Waveform
AC - AC Conversion	Step-up Transformer (48/230V AC) Nearly Sinusoidal Waveform
Connected Load	Single Phase 230V AC Lamp Load

d) Simulation Model of Proposed System

The overall Simulation diagram of the proposed closed loop system for FCMLI is shown in Figure 2.

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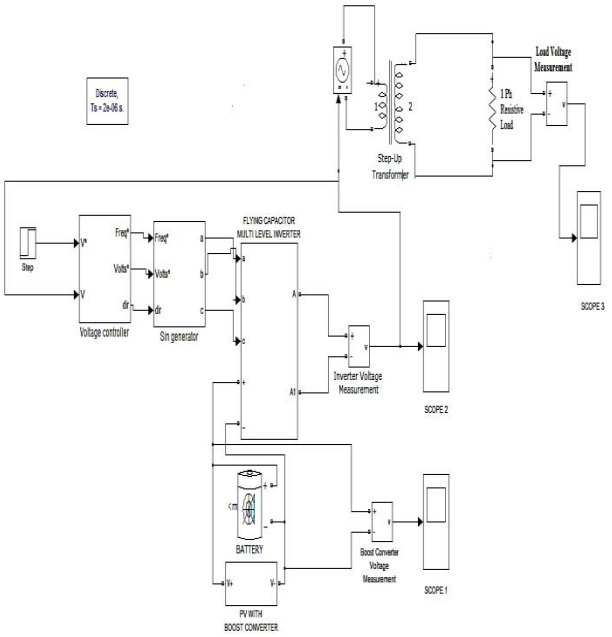

Figure 2 : Overall Simulation Model of Proposed System

III. Capacitor Clamped Dc-Dc Boost Converter

a) Significance of Usage

A Capacitor Clamped DC-DC Boost Converter with single switching element - MOSFET is proposed in this paper. Instead of using two or more than two number of switching devices as in the case of conventional half-bridge or full-bridge DC-DC converters, the proposed topology uses only one switching device there by fast switching with less switching loss is possible with this type of converter.

b) Basic Configuration

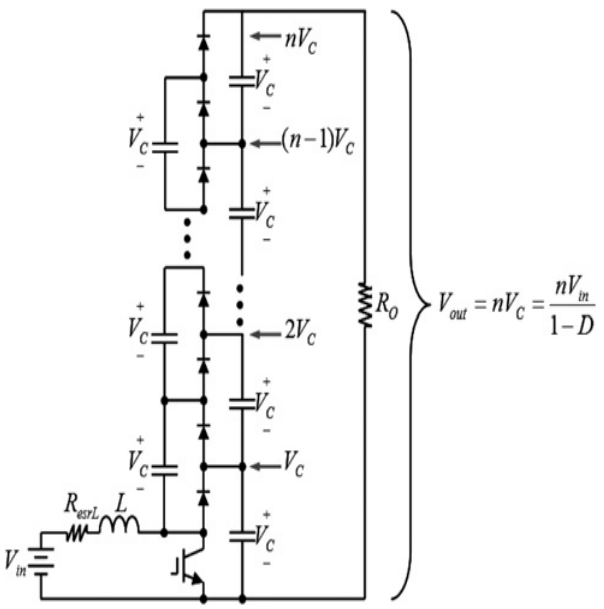

Figure 3 : Basic Configuration of DC-DC MBC for Nx or N+1 levels

The proposed circuit is based on the multilevel converter principle, where each device blocks only one voltage level achieving high-voltage converters with low-voltage devices. It is a Nx DC-DC converter based on one driven switch, 2N+1 diodes and 2N+1 capacitors. One advantage of the topology is that the number of levels can be extended by only adding capacitors and diodes and the main circuit does not need to be modified.

c) Circuit Description

The DC–DC Multilevel Boost Converter (MBC) is a PWM based DC–DC converter, which combines the boost converter and the switched capacitor function to provide different output voltages and a self-balanced voltage using only one driven switch, one inductor, 2N-1 diodes and 2N-1 capacitors for an Nx MBC.

The difference between the MBC and the conventional one is that in the MBC, the output is Vc times N, where N+1 is the converter's number of levels taking into account the zero level as shown in Figure 3. This behavior is achieved, thanks to the voltage multiplier in the boost converter's output that is driven by the only switch in the converter.

IV. Flying Capacitor Multilevel Inverter (FCMLI)

a) Basic Configuration

The FCMLI requires a large number of capacitors to clamp the device (switch) voltage to one capacitor voltage level. Provided all the capacitors are of equal value, the size of the voltage increment between two consecutive legs of the clamping capacitors defines the size of voltage steps in the output waveform, if the voltage of the main dc-link capacitor is Vdc the voltage of the innermost capacitor clamping the innermost two devices is Vdc/ (n-1).

The voltage of the next innermost capacitor will be Vdc/(n-1) + Vdc/ (n-1) = 2 Vdc/(n-1) and so on. Each next clamping capacitor will have the voltage increment of Vdc/(n-1) from its immediate inner one. The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assures that the voltage stress across each main device is same and is equal to Vdc/(n-1) for an n- level inverter.

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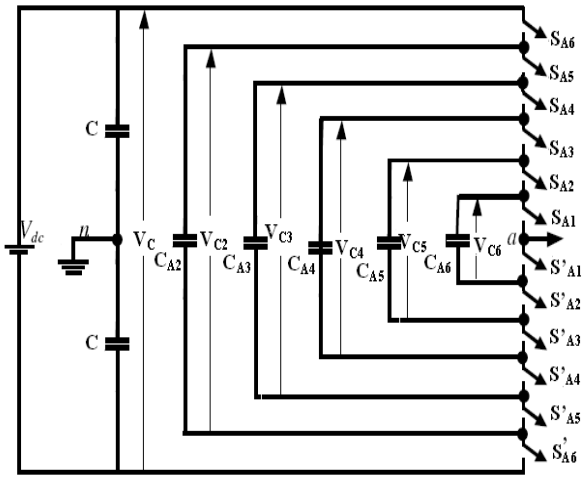

Figure 4 : One Phase Leg of a Seven Level lying Capacitor Multilevel Inverter

A one phase leg of seven-level inverter as shown in Figure 4. For a three phase inverter, two more legs of same construction are coupled to the same dc-link battery Vdc. In this figure each switch SA1 to SA6 and S'A1 to S'A6 consists of a power semiconductor device (e.g. GTO, IGBT) and an anti-parallel diode. Voltages VC, Vc2, Vc3, Vc4, Vc5, and Vc6 are Vdc, 5/6 Vdc, 2/3 Vdc, Vdc/2, Vdc/3, and Vdc/6 respectively, as n= 7.

b) Features of FCMLI

The FCMLI has the following features.

i. Voltage stresses across the devices are equal.
ii. Switching combination chosen affects the current rating of the capacitor
iii. Redundancy of switching combinations.
iv. Single capacitor voltage regulating circuit is required.

V. Results and Analysis

The proposed topology of closed loop system for Flying Capacitor Multilevel Inverter (FCMLI) consists of various models. They are

i. Photovoltaic Generation Model.
ii. Capacitor Clamped DC-DC Boost Converter Model.
iii. Open Loop FCMLI Model.
iv. Closed Loop FCMLI Model.

a) Photovoltaic Generation Model

The Simulation diagram for the PV Generation by a single stand-alone 12V PV module is shown in Figure 5.

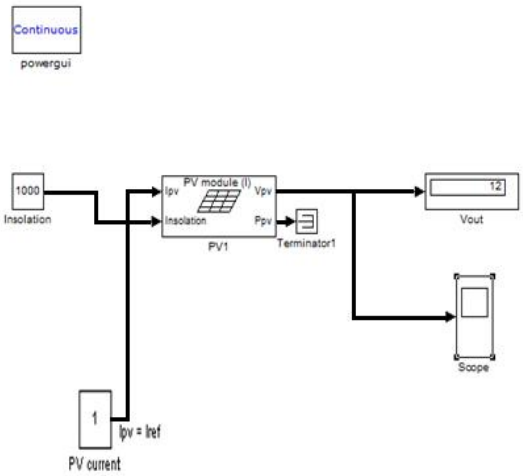

Figure 5 : MATLAB Model of Photovoltaic Generation

It consists of Insolation block, Single PV module block for DC voltage generation and display & scope blocks for displaying the output in numerical and graphical form respectively. The technical specifications of the PV module used in the proposed system are listed in the TABLE II.

Table 2 : Technical Specifications of Pv Module

S. No	Parameters	Specifications	Units
1	Short Circuit Current (Isc)	5.45A	Amperes
2	Open Circuit Voltage (Voc)	12V	Voltage
3	Current at Pmax	4.95A	Amperes
4	Voltage at Pmax	17.2V	Voltage
5	Insolation	1000 W/m^2 (Constant)	Watts / metre^2

The Simulated output is taken for 1000 watts/m^2 of Insolation and 25^{o}C of Temperature under Standard Test Condition (STC).

The corresponding output voltage waveform of 12V PV Panel is shown in the Figure 6.

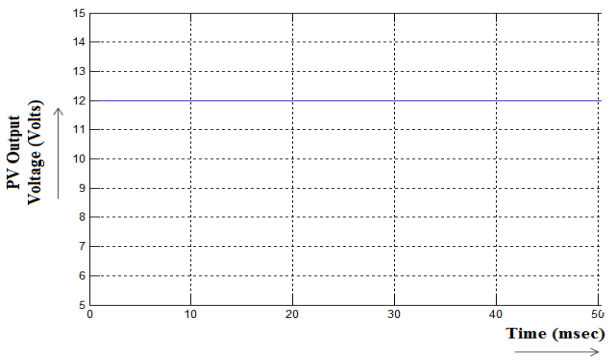

Figure 6 : Output Voltage Waveform of PV Module

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Thus from the PV Panel, a 12V DC of Unidirectional Voltage is produced. Then this low value of DC voltage is given to the Boost converter for achieving desired DC voltage for giving input to the Multilevel Inverter.

b) Capacitor Clamped Dc-Dc Boost Converter Model

From the PV module a 12V DC voltage is obtained. This unidirectional DC voltage is then given to the Capacitor Clamped DC-DC Boost Converter for boosting up the voltage up to 48V DC.

The Simulation diagram of the Capacitor Clamped DC-DC Boost Converter is shown in Figure 7.

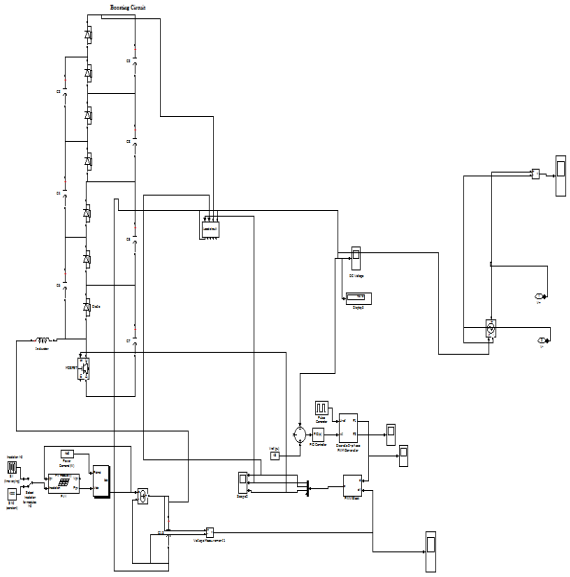

Figure 7 : MATLAB Model of Capacitor Clamped Boost Converter

It consists of various circuit elements such as Boost Inductor, MOSFET, Clamping Capacitor and free-wheeling diodes for boosting up the DC voltage from PV panel – 12V DC into 48V DC. It also consists of a comparator, PID controller, pulse generator and PWM block for producing pulses for MOSFET.

The corresponding output voltage waveform of the proposed Capacitor Clamped DC-DC Boost Converter is shown in Figure 8.

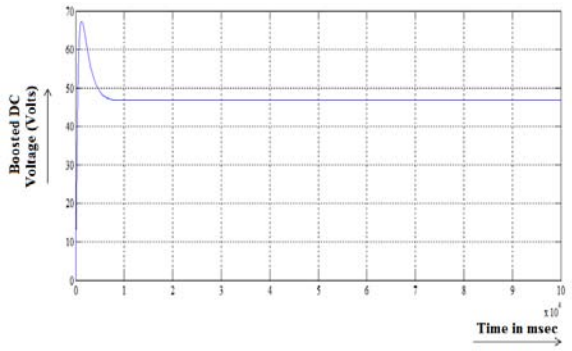

Figure 8 : Output Voltage Waveform of Boost Converter Model

From the above output, the main inference is initially the voltage signal is raised to nearly 60V DC and then it is settled down to the 48V of DC. The reason behind that is because of the presence of the boosting inductor in the initial stage of boost converter, the voltage raise takes place and after that based on the set value in comparator it falls to actual pre-defined value.

c) Open Loop FCMLI Model

From the Boost Converter Model, a 48V of DC is given to the Seven Level FCMLI for converting a DC voltage into stepped output waveforms.

The Figure 9 shows the corresponding overall simulation model of proposed Multilevel Inverter which includes the Inverter model and pulse generation model.

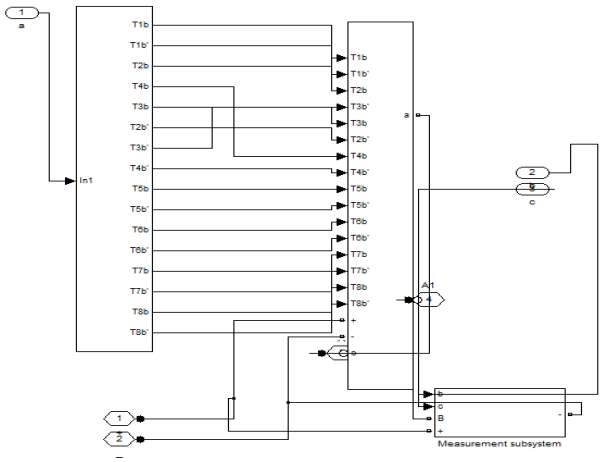

Figure 9 : MATLAB Model of FCMLI

The proposed Seven Level FCMLI will produce the seven levels of stepped AC output waveforms at its output. The switching sequence of various switches used in the Inverter model are determined by the PWM pulses from the pulse generation model. In this Pulse Generation Model, there are six number of carrier signals which are produced by Repeating sequence concept and these signals are compared with the Sinusoidal signal with the help of the relational operator (>=).

Here Multicarrier PWM in turn PD-PWM technique is employed for generating appropriate PWM pulse signals for respective switches in the MLI.

The Figure 10 shows the Pulse Generation Model Using Multicarrier PWM – PDPWM technique for Seven Level FCMLI.

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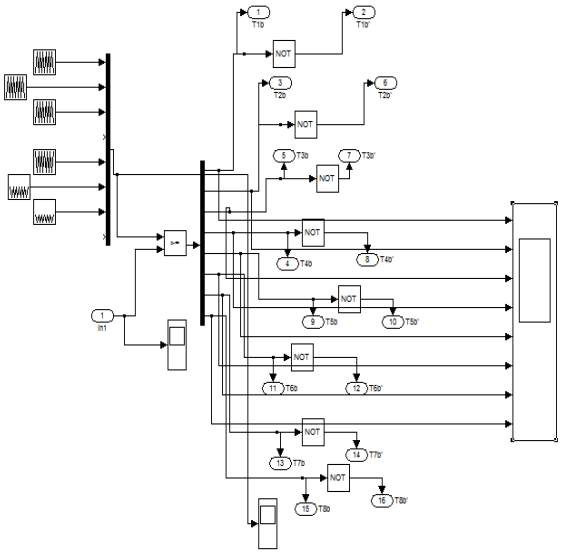

Figure 10 : Pulse Generation Model for Multilevel Inverter Using Multicarrier (PDPWM) Technique

The Figure 11 shows the six number of carrier signals in PD-PWM Pulse Generation Model.

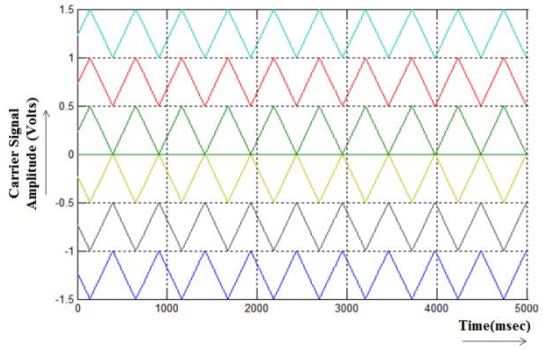

Figure 11 : Carrier Signals Used in Pulse Generation Model

The six carrier signals used in pulse generation model are generated based on the repeating sequence concept which is listed in the Table III.

Table 3 : Carrier Signal Generation For Pulse Generation Model

S. No	Carrier Signals	Time Values (Sec)	Output Values (Volts)
1	1st Carrier	[0 0.005/20 0.01/20 0.015/20 0.02/20]	[0 .5 0 .5 0]
2	2nd Carrier	[0 0.005/20 0.01/20 0.015/20 0.02/20]	[.5 1 .5 1 .5]
3	3rd Carrier	[0 0.005/20 0.01/20 0.015/20 0.02/20]	[1 1.5 1 1.5 1]
4	4th Carrier	[0 0.005/20 0.01/20 0.015/20 0.02/20]	[0 -.5 0 -.5 0]
5	5th Carrier	[0 0.005/20 0.01/20 0.015/20 0.02/20]	[-.5 -1 -.5 -1 -.5]
6	6th Carrier	[0 0.005/20 0.01/20 0.015/20 0.02/20]	[-1.5 -2 -1.5 -2 -1.5]

The Figure 12 shows the comparison of six number of carrier signals and the sinusoidal modulating signal. In which the sinusoidal signal is superimposed over the carrier signals for generating appropriate PWM pulses.

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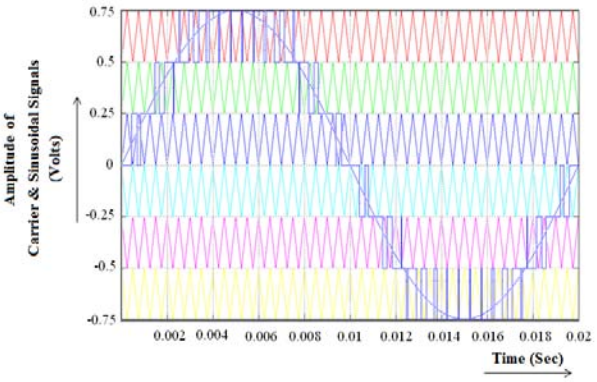

Figure 12 : PDPWM Modulation Scheme

The corresponding open loop output voltage waveform of proposed Multilevel Inverter is shown in Figure 13.

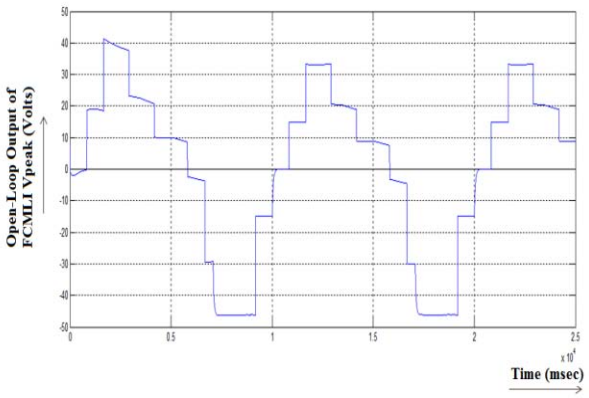

Figure 13 : Open Loop AC Output Voltage Waveform of FCMLI

From the Open loop output, it is observed that seven level stepped output waveform with the magnitude of nearly 48V is achieved but it is slightly distorted. Because of this the Total Harmonic Distortion (THD) of open-loop output is having more percentage values. Thus in order to reduce the THD level of Multilevel Inverter output and to improve the performance of the system, a closed-loop design is essential for Multilevel Inverter. By implementing the closed-loop system, the THD level can be reduced to certain extend.

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d) Closed Loop FCMLI Model

i. *Voltage Controller Model*

For designing closed-loop system for proposed MLI, various blocks such as Voltage Controller block, Sin Generator block are used.

The Figure 14 shows the voltage controller – PID controller model for closed-loop design of Seven Level FCMLI.

The various blocks used in the voltage controller model are Zero-order Hold, gain, Abs - absolute, comparator, discrete-time integrator, saturation and rate transition blocks.

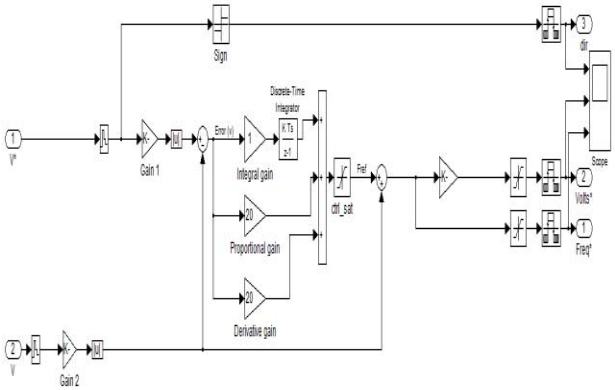

Figure 14 : Simulation Model of Voltage Controller in Closed-loop System

ii. *Sin Generator Model*

The output of the voltage controller model is given as the three input parameters of sin generator model. This model is used to produce the sinusoidal modulating signal which is used in pulse generation model for producing PWM output pulses.

The Figure 15 shows Sin Generator model for closed-loop design of Seven Level FCMLI.

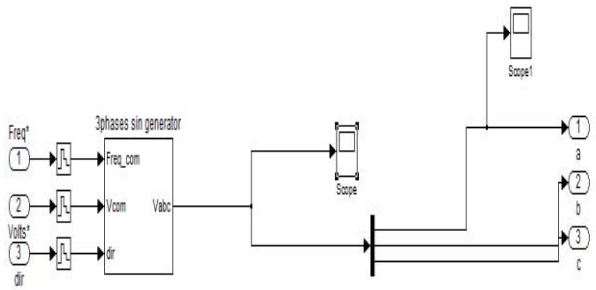

Figure 15 : Simulation Model of Sin Generator in Closed-loop System

The corresponding single phase sinusoidal outputs of Sin Generator Model are shown in the Figure 16.

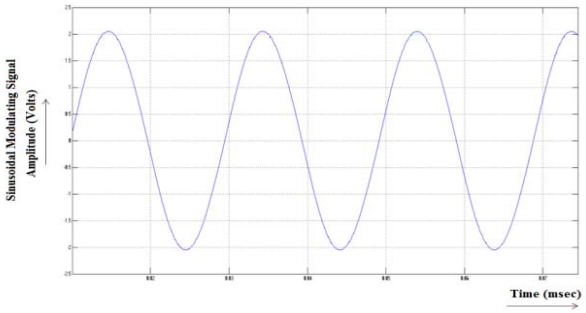

Figure 16 : Single Phase Sinusoidal Output of Sin Generator For Pulse Generation Model

Thus after the comparison of Sinusoidal modulating signal and generated carrier signals using PDPWM Technique in Pulse Generation Model, the appropriate PWM switching pulses are generated. These pulses are used to trigger the switching devices in proposed MLI in a proper sequence to produce the stepped AC waveform from the output of MLI.

In order to reduce the THD level of MLI output a closed-loop model is developed and its corresponding output voltage is shown in Figure 17.

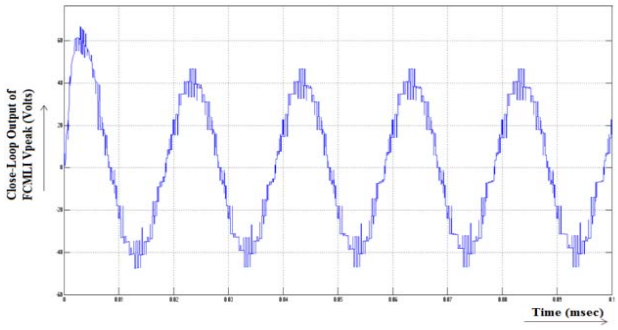

Figure 17 : Closed Loop AC Output Voltage Waveform of FCMLI

e) Load Voltage Waveform

For connecting a Single Phase resistive lamp load, the 48V AC stepped output waveform from the MLI is given to the 48/230V AC step-up transformer.

The Figure 18 shows the corresponding output voltage waveform of a step-up transformer (48/230V AC). This AC voltage is fed to the Single Phase Lamp Load.

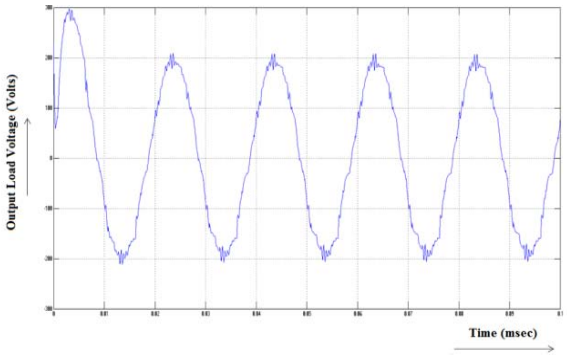

Figure 18 : Output Load Voltage Waveform

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f) Total Harmonic Distortion

The Total Harmonic Distortion (THD) is used to characterize the linearity of audio systems and the power quality of electric power systems.

The formula below shows the calculation for THD on a voltage signal. The end result is a percentage comparing the harmonic components to the fundamental component of a signal. The higher the percentage, the more distortion that is present on the mains signal.

$$THD = \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \ldots\ldots + V_n^2)}}{V_1} * 100\% \qquad (1)$$

The results of THD analysis performed for both open-loop and closed-loop systems are shown in the Figures 19 and 20.

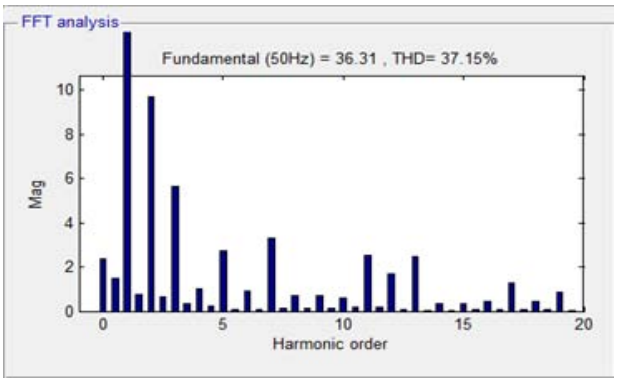

Figure 19 : Open Loop THD Result of Seven Level FCMLI

From the Figure 19, it is observed that THD value of **37.15%** is obtained for Open-Loop Multilevel Inverter. This value can be reduced by Closed-Loop design.

The result of THD analysis performed for closed-loop systems is shown in Figure 20.

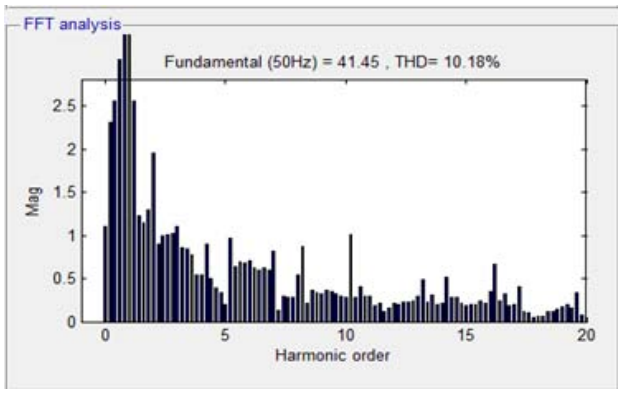

Figure 20 : Closed Loop THD Result of Seven Level FCMLI

From the Figure 18, it is observed that THD value of **10.18%** is obtained for Closed-Loop Multilevel Inverter. This is comparatively lesser value than the THD obtained in Open-Loop system.

VI. Conclusion

Thus the investigation study for seven level FCMLI was performed with / without closed-loop feedback schemes.

In the proposed method, a closed-loop system was implemented for a Seven Level FCMLI. The newly developed design will improve the system performance and maintains the voltage stability there by stable operation can be ensured without more disturbances. The closed loop controller is also designed for Capacitor Clamped DC-DC Boost Converter there by constant output voltage at the output of the boost converter can be achieved.

The performance was verified through simulation models by using MATLAB software tool. From the simulation study, the important conclusions are,

i. From the output of Stand-alone single PV Module, a unidirectional DC voltage of 12V DC was produced based on the panel parameters and Insolation level.
ii. From the output of Capacitor Clamped DC-DC Boost Converter, a boosted DC voltage of 48V DC is produced with the help of single switching device there by switching loss and circuit complexity are reduced.
iii. From the output of FCMLI, an AC output voltage of 48V AC stepped signals are obtained. There by THD level is reduced.

Investigation Report:

Seven Level Flying Capacitor Multilevel Inverter		
Feedback Schemes	With Closed-Loop Scheme	Without Closed-Loop Scheme
Total Harmonic Distortion (THD) in percentage	**10.18%**	**37.15%**

The main inference from the proposed concept is, for the developed Seven Level FCMLI system the THD value of open-loop model is 37.15% and for the closed-loop model is 10.18%. Thus the percentage of THD value can be minimized by implementing the closed-loop control for FCMLI there by better performance in its output can be achieved.

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