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Design of 8-Bit Arithmetic Processor Unit based on Reversible Logic

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Abstract - Reversible logic is emerging as an important research area in the recent years due to its ability to reduce the power dissipation, which is the main requirement in low power digital design. Energy dissipation is proportional to the number of bits lost during computation. The reversible circuits do not lose information and can generate unique outputs from specified inputs and vice versa. It has application in diverse fields such as low power CMOS design, optical information processing, cryptography, quantum computation and nanotechnology. This paper proposes a reversible design of an 8 -bit arithmetic processor. The architecture of the processor has been proposed, in which, each block is realized using reversible logic gates. The important blocks of the processor are control unit, arithmetic and logical unit and register file. Each module has been coded using Verilog then simulated using Modelsim and prototyped in Xilinx-Spartan 3E.

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Abstract - Reversible logic is emerging as an important research area in the recent years due to its ability to reduce the power dissipation, which is the main requirement in low power digital design. Energy dissipation is proportional to the number of bits lost during computation. The reversible circuits do not lose information and can generate unique outputs from specified inputs and vice versa. It has application in diverse fields such as low power CMOS design, optical information processing, cryptography, quantum computation and nanotechnology. This paper proposes a reversible design of an 8 -bit arithmetic processor. The architecture of the processor has been proposed, in which, each block is realized using reversible logic gates. The important blocks of the processor are control unit, arithmetic and logical unit and register file. Each module has been coded using Verilog then simulated using Modelsim and prototyped in Xilinx-Spartan 3E.

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I. Introduction

In modern VLSI system, power dissipation is very high due to rapid switching of internal signals. Landauer showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of every bit of information results in dissipation of KT*log2 Joule of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed.

Bennett showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [1]. A gate is considered to be reversible only if each and every input has a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate has same number of inputs and outputs.

II. Basic Reversible Gates

There exist many reversible gates in the literature. Among them 2*2 Feynman gate, 3*3 Fredkin gate, 3*3 Toffoli gate and 3*3 Peres gate are the most referred. The detailed cost of a reversible gate depends on any particular realization of quantum logic [2]. Generally, the cost is calculated as a total sum of 2*2 quantum primitives used. The cost of Toffoli gate is exactly the same as the cost of Fredkin gate and is 5. The only cheapest quantum realization of a complete (universal) 3*3 reversible gate is Peres gate and its cost is 4.

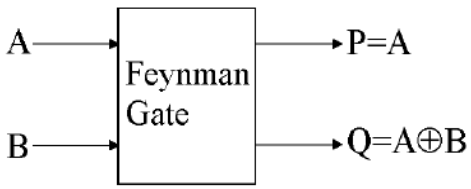

Figure 1: Feynman Gate

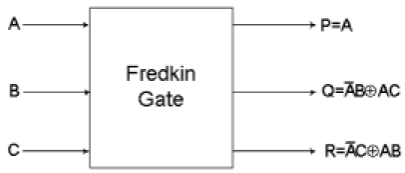

Figure 2 : Fredkin Gate

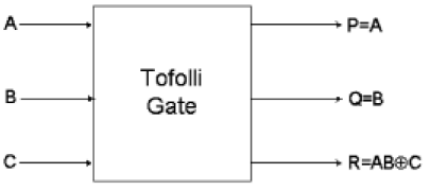

Figure 3 : Tofolli Gate

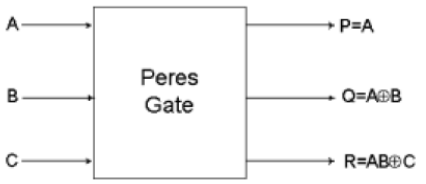

Figure 4 : Peres Gate

III. Processor Architecture

The architecture of the 8-bit reversible processor is shown in Figure.5. The various components included in the 8-bit reversible processor are as follows:

- Accumulator
- Temporary Register
- ALU Result Register
- Status Register
- Program Counter
- Instruction Register
- Register File of 16 registers
- Arithmetic And Logical Unit
- Control Unit

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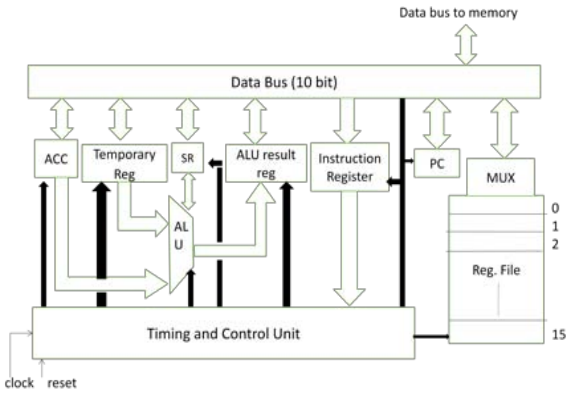

Figure 5 : Processor Architecture

The design of the various blocks of the processor is as follows:

a) Arithmetic and Logic Unit

The arithmetic and logic unit has 4-bit select inputs to select one from 16 operations as shown in Table.1. Two 8-bit data are given as input to the ALU. The logical operations include all basic logic gates. The various sub modules in the design are adder/subtractor, multiplier and a logical unit.

Table 1 : Operations in the ALU

I3	I2	I1	I0	Operation
0	0	0	0	Clear
0	0	0	1	A+B
0	0	1	0	A-B
0	0	1	1	A*B
0	1	0	0	A++
0	1	0	1	A--
0	1	1	0	Left Shift
0	1	1	1	Right Shift
1	0	0	0	Or
1	0	0	1	And
1	0	1	0	Not
1	0	1	1	Xor
1	1	0	0	Nor
1	1	0	1	Nand
1	1	1	0	Xnor
1	1	1	1	Preset

The 8-bit reversible adder/subtractor has been designed using Peres gates and Feynman gates [3]. HNG gates and Peres gates are used in the design of the 8-bit reversible multiplier [6].The left and right shifter blocks are designed using reversible multiplexers.

b) Register File

The register file includes 16 registers and two 4 to 16 decoders as shown in the Figure.6. The two select signals 'load' and 'enable' are used for loading data into and reading value of data from the individual registers of the register file respectively. The 4 to 16 decoder is designed using reversible Fredkin gates [4].

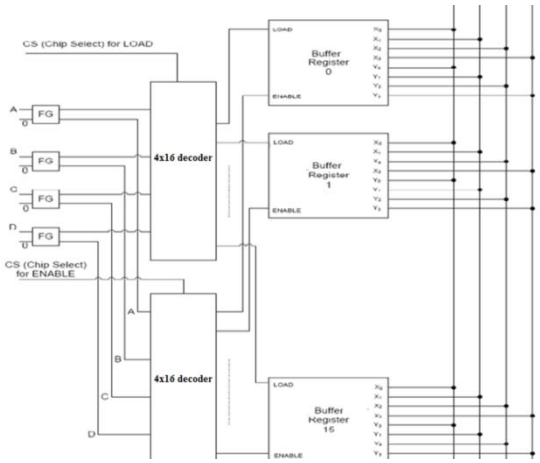

Figure 6 : Register File

c) Control Unit

The Figure. 7 shows the 10 bit instruction used in this design. The first two bits correspond to LOAD and ENABLE. The next 3-bits correspond to DEVICE ID of the memory component. The DEVICE ID assigned to each memory component is shown in Table.2. If the LOAD is 1, then the device specified by the DEVICE ID will take the input from the data bus. If the ENABLE is 1, the device specified by the DEVICE ID will output its content to the data bus. The lower 4-bits of the instruction carry useful information for both ALU and 16-bit Register File.

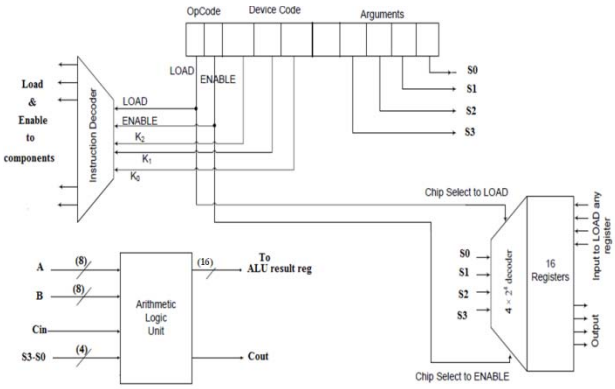

Figure 7 : Instruction Format

The important block of the control unit is the instruction decoder, which controls the eight memory components of the processor. Instruction decoder consists of two 3 to 8 decoders as shown in Figure.8. Two select signals 'load' and 'enable' are used for the decoders. The 3 to 8 decoder is designed using reversible Fredkin gates [4].

Table 2 : Device IDs of Memory Components

Device Id	Device Name
000	Accumulator Register
001	ALU Result Registers
010	Data Bus Buffer Register

011	Program Counter
100	Instruction Register
101	Status Register
110	Register File
111	Temporary Register

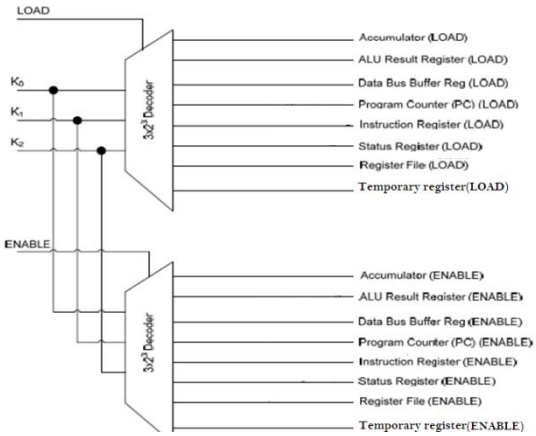

Figure 8 : Instruction Decoder

d) Memory Components

- The Accumulator is a controlled buffer that stores intermediate results or it may be used to store an operand for a binary operation performed by the ALU.
- Temporary Register is another controlled buffer register to store the second operand of any binary operation as performed by the ALU.
- Status Register is a 4-bit buffer register that represents the four flags (carry flag, overflow flag, sign flag, zero flag).
- ALU result registers are also controlled buffer register used to store the result of the ALU operation.
- The Data Bus Buffer is another controlled buffer register that takes input from memory module. It is directly connected to the data bus.

IV. Simulation Results

All the blocks are modelled using VERILOG. The functional verification of the codes is analysed using ModelSim-Altera 6.4a (Quartus II 9.0) Starter Edition and synthesised using Xilinx ISE Design Suite 13.4. The simulation results of the ALU, Instruction Decoder, Register File and Memory Components are shown in Figure.9, 10, 11, 12 respectively.

a) Arithmetic and Logical Unit

Here 'a' and 'b' indicates the 8-bit data and 'i' is a 4- bit input data that acts as the control signal. Depending on this value the required output results are obtained and stored in 'x' and 'y'.

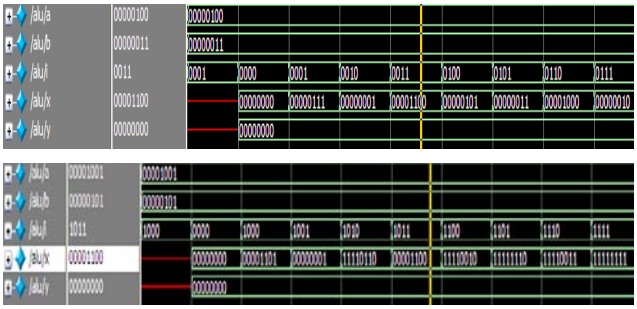

Figure 9 : Simulation Result of ALU

b) Instruction Decoder

Here two 3 to 8 reversible decoders are used. One for controlling the LOAD input 'l' of each of the 8 memory components and other to control the ENABLE input 'e' of each of the components. Here k is the 3-bit selection input to address each memory component.

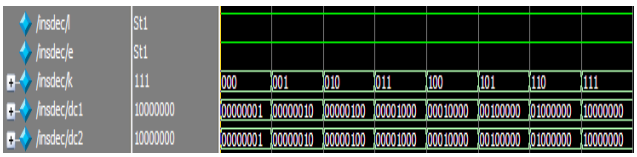

Figure 10 : Simulation Result of Instruction Decoder

c) Register File

Since 16 registers are present, 4-bit address 's' is used to select one of the registers. LOAD 'l' and ENABLE 'e' inputs act as control signals and 'din' acts as the data input to the register file.

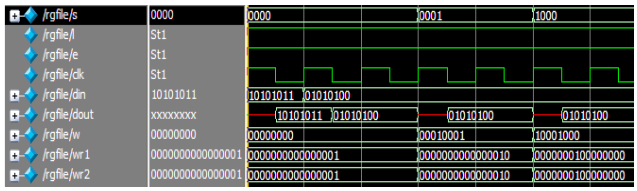

Figure 11 : Simulation Result of Register file

d) Memory Components

Accumulator, Temporary register, ALU result registers, Data Bus Buffer register are the memory components used in this design. The memory components are controlled buffer registers with two control signals LOAD 'l' and ENABLE 'e'.

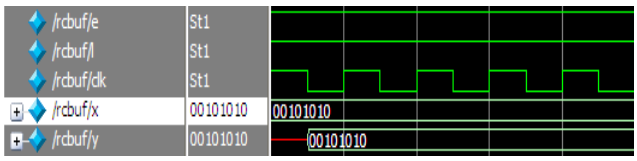

Figure 12 : Simulation Result of Controlled Buffer Register

V. Conclusion and Future Work

Reversible circuits are an emerging technology with promising applications because of the low power dissipation. In this paper a novel architecture of a

reversible 8-bit processor has been proposed. Each block of the processor was designed using the basic reversible gates.

In future, this design can be extended to any number of bits. This paper provides the circuit level implementation of the reversible processor. Further this design may be extended to transistor implementation which would help in easier analysis of power.

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