Global Journal of Researches in Engineering
Electrical and Electronics Engineering
Volume 13 Issue 3 Version 1.0 Year 2013
Type: Double Blind Peer Reviewed International Research Journal
Publisher: Global Journals Inc. (USA)
Online ISSN: 2249-4596 & Print ISSN: 0975-5861

Implementation of Closed Loop System for Diode Clamped Multilevel Inverter with Stand-Alone Photovoltaic Input

By Venus.V & K.Ramani
K.S.Rangasamy College of Technology

Abstract - Multilevel inverter is as one of the most recent and popular type of advances in power electronics. It synthesizes desired output voltage waveform from several dc sources used as input for the multilevel inverter. This paper describes a diode-clamped five-level inverter-based battery/super capacitor direct integration scheme for photovoltaic energy systems. The study is carried out for three cases. In the first case, one of the two dc-link capacitors of the inverter is replaced by a battery bank and the other by a super capacitor bank. In the second case, dc-link capacitors are replaced by two battery banks. In the third case, ordinary dc-link capacitors are replaced by two super capacitor banks. The first system is supposed to mitigate both long-term and short-term power fluctuations while the last two systems are intended for smoothening long-term and short-term power fluctuations, respectively. These topologies eliminate the need for interfacing dc–dc converters and thus considerably improve the overall system efficiency. The major issue in aforementioned systems is the unavoidable imbalance in dc-link voltages. An analysis on the effects of unbalance and a space vector modulation method, which can produce undistorted current even in the presence of such unbalances, are presented in this paper. Simulation work is done using the MATLAB software which validates the proposed method and finally THD comparison is presented for analysis.

Keywords : *diode-clamped five-level inverter, direct integration of battery energy storage systems, space vector modulation, unbalanced operation of diode-clamped five-level inverter.*

GJRE-F Classification : *FOR Code: 090699*

Strictly as per the compliance and regulations of :

Implementation of Closed Loop System for Diode Clamped Multilevel Inverter with Stand-Alone Photovoltaic Input

Venus.V[α] & K.Ramani[σ]

Abstract - Multilevel inverter is as one of the most recent and popular type of advances in power electronics. It synthesizes desired output voltage waveform from several dc sources used as input for the multilevel inverter. This paper describes a diode-clamped five-level inverter-based battery/super capacitor direct integration scheme for photovoltaic energy systems. The study is carried out for three cases. In the first case, one of the two dc-link capacitors of the inverter is replaced by a battery bank and the other by a super capacitor bank. In the second case, dc-link capacitors are replaced by two battery banks. In the third case, ordinary dc-link capacitors are replaced by two super capacitor banks. The first system is supposed to mitigate both long-term and short-term power fluctuations while the last two systems are intended for smoothening long-term and short-term power fluctuations, respectively. These topologies eliminate the need for interfacing dc–dc converters and thus considerably improve the overall system efficiency. The major issue in aforementioned systems is the unavoidable imbalance in dc-link voltages. An analysis on the effects of unbalance and a space vector modulation method, which can produce undistorted current even in the presence of such unbalances, are presented in this paper. Simulation work is done using the MATLAB software which validates the proposed method and finally THD comparison is presented for analysis.

Keywords : diode-clamped five-level inverter, direct integration of battery energy storage systems, space vector modulation, unbalanced operation of diode-clamped five-level inverter.

I. Introduction

Multilevel converters are mainly utilized to synthesis a desired single or three-phase voltage waveform. The desired multi staircase output voltage is obtained by combining several dc voltage sources. Solar cells, fuel cells, batteries and ultra capacitors are the most common independent sources used. The intermittent nature of renewable energy sources can create serious system stability issues, especially at increased levels of penetration [1], [2]. Renewable energy resources will be an Increasingly important part of power generation in the new millennium. Besides assisting in the reduction of the emission of greenhouse gases, they add the much-needed flexibility to the energy resource mix by decreasing the dependence on fossil fuels. Recently, batteries and super capacitors have emerged as leading energy storage devices [3]-[6].Furthermore, the combination of battery and super capacitor provides an excellent match that can cover a wide range of power and energy requirements [5],[15].

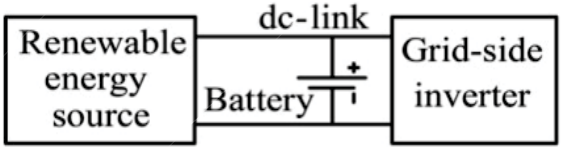

Fig. 1 (a) : Direct connection to the dc link

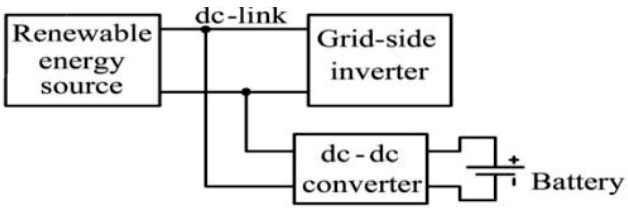

Fig. 1 (b) : Connection to the dc link through a dc–dc converter

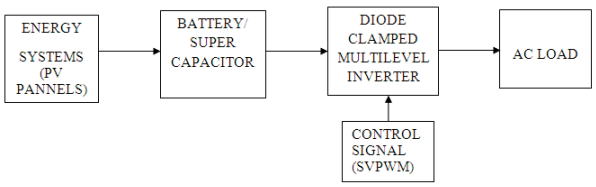

Fig. 1 (c) : Proposed battery/super capacitor five level inverter direct integration scheme

The simplest way of adding a battery (or a super capacitor) bank is the direct connection to the dc link of the grid side inverter, as shown in Fig. 1(a). But it suffers from several drawbacks such as large internal resistance, fixed current distribution governed by internal resistors, and lack of control over the power flow [8] .Effects of these issues can somewhat be reduced if an intermediate dc–dc converter is placed between the

Author : PG Scholar – Final Year, Power Electronics & Drives / EEE, K.S.Rangasamy College of Technology, Tiruchengode, Tamilnadu, India. E-mail : venuseee1989@gmail.com
Author : Associate Professor, Power Electronics & Drives/ EEE, K.S.Rangasamy College of Technology,Tiruchengode,Tamilnadu, India. E-mail : kreee82@gmail.com

battery (or the super capacitor) bank and the dc link as shown in Fig. 1(b). But the disadvantage of this topology is the increased number of components, cost, and power losses.

Therefore, the possible alternative ways of connection to avoid additional dc–dc converter while maintaining the control flexibility. The result is the simple configuration shown in Fig. 1(c). In the figure, the dc-link capacitors of a standard diode-clamped five-level inverter are replaced by a battery bank and a super capacitor bank. Latter part of this paper discusses two more cases: one with two super capacitor banks and the other with two battery banks. If a change in the source or the load happens, the power imbalance will be compensated by the battery bank and/or super capacitor bank.

The main issue with this particular topology is the imminent imbalance of the neutral point potential which is due to unequal states of charge of the battery bank and the super capacitor bank. Comprehensive analysis on capacitor voltage unbalance and balancing techniques used in diode-clamped inverters can be found in the literature [1], [8].A new Space Vector Modulation (SVM) method has been developed for diode-clamped five-level inverters with variable dc-link voltages. Furthermore, full controllability over small vector selection is available in the proposed SVM method. Relevant equations and diagrams are given in Section III with a detailed analysis. The proposed SVM technique involves more computations compared to simplified SVM techniques proposed in the literature. The THD values for the Traditional, Conventional and proposed inverters are compared and analysed.

II. Unbalanced Dc-Link Voltages Effects

For the diode-clamped Five-level inverter, shown in Fig. 1(c), line-to-ground voltages can be derived from switching states *Sa, Sb*, and *Sc*, and the results are given in Table I. If the inverter is connected to a balanced three-phase load, corresponding phase voltages can be derived from line-to-ground voltages using (1). Then, these phase voltages are transformed into the *dq* reference frame by (2).

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \quad (1)$$

Table 1 : Switching States And Line-To-Ground Voltages

Switching state s_a, s_b, s_c	IGBT Switching Sequence of the leg (Top to Bottom)	Line to ground Voltages v_{ag}, v_{bg}, v_{cg}
0	0011	0
1	0110	V_L
2	1100	$V_L + V_U$

$$\begin{bmatrix} v_{ds} \\ v_{qs} \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} \quad (2)$$

The locations of small and medium vectors vary with dc-link voltages as shown in Fig. 2. However, locations of large vectors (2 0 0, 2 2 0, 0 2 0, 0 2 2, 0 0 2, and 2 0 2) depend only on the total dc-link voltage and would remain unchanged if the total voltage is constant. When capacitor voltages are balanced, positive and negative small vectors (2 1 1, 2 2 1, 1 2 1, 1 2 2, 1 1 2, 2 1 2, 1 0 0, 1 1 0, 0 1 0, 0 1 1, 0 0 1, and 1 0 1) coincide and only one inner hexagon is formed as shown in Fig. 2(b). Furthermore, medium vectors (2 1 0, 1 2 0, 0 2 1, 0 1 2, 1 0 2, and 2 0 1) reach midpoints of the outer hexagon. If an unbalance is present, small vectors split and two separate inner hexagons appear as shown in Fig. 2(a) and (c). In addition to that, medium vectors move toward large vectors. The size of the inner hexagon formed with negative small vectors depends on the battery voltage, which is nearly constant in the proposed system. Similarly, the size of the inner hexagon formed with positive small vectors varies with the super capacitor voltage. The circles marked with dotted lines in Fig. 2 represent the path of the reference voltage vector. In the proposed method, the super capacitor voltage is allowed to vary in a way that this circle will always remain within the outer hexagon and middle inner hexagon. If the normal SPWM with two equal carriers, as shown in Fig. 3(b),

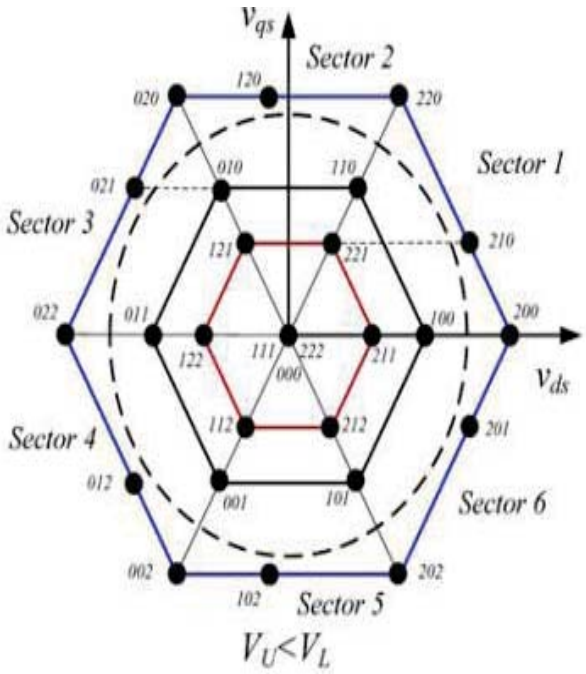

Fig. 2 (a) : Space vector diagram for VU< VL

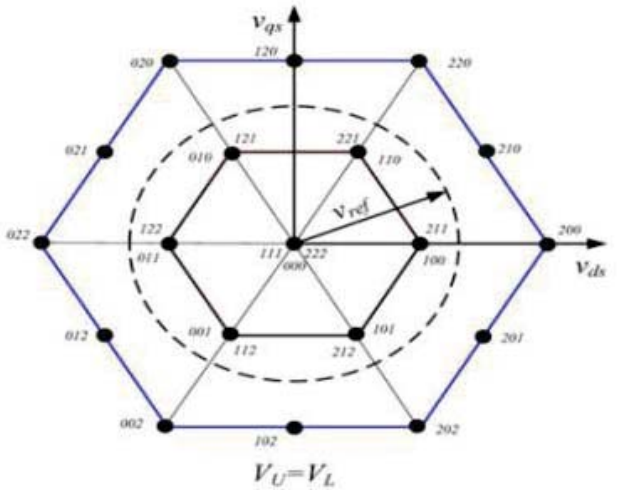

Fig. 2 (b) : Space vector diagram for $VU = VL$

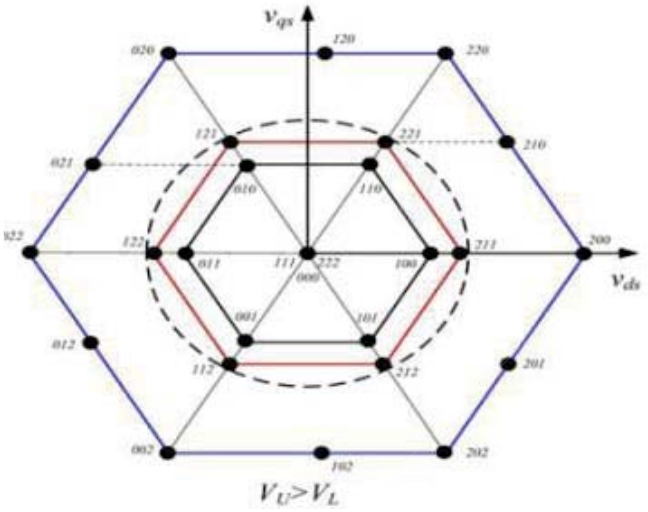

Fig. 2 (c) : Space vector diagram for $VU > VL$

is used, a dc offset will be present in the inverter output voltage. This effect is clearly visible in the fundamental component shown in Fig. 3(c).where the carriers are modified according to the voltage imbalance as shown in Fig. 3(e). Equations (3) and (4) are used to determine the amplitudes *AU* and *AL* of new carriers

$$A_U = \frac{2V_U}{V_U + V_L} \quad (3)$$

$$A_L = \frac{2V_L}{V_U + V_L} \quad (4)$$

Therefore, a novel space vector modulation method has been developed, from the scratch, to reduce voltage stresses and to produce desired fundamental components even at large imbalanced conditions. The result of the proposed SVM technique is shown in Fig. 3(h). Its fundamental component is very similar to that of the waveforms shown in Fig. 3(g), and hence, it is not shown here exclusively. A detailed description of the proposed SVM technique is given in Section III.

III. Implementation of Svm Technique

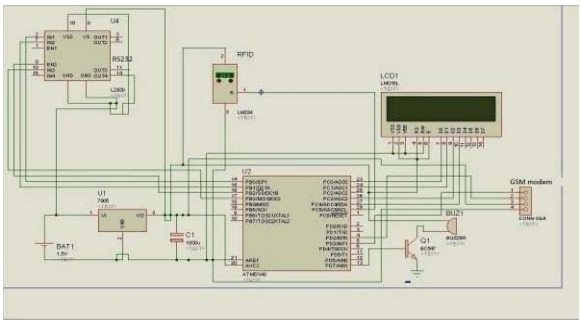

Fig. 3 : Block diagram of the proposed technique

A simplified block diagram of the proposed SVM technique is shown in Fig. 3. The amplitude *r* and the angle of the reference voltage vector are generated by the grid side inverter controller. Currently, serving sector of the space vector diagram is derived from the phase angle. However, due to the presence of two candidate triangles, four different limit angles, $\theta 1$, $\theta 2$, $\theta 3$, and $\theta 4$, need to be calculated for a given sector. First two limit angles ($\theta 1$ and $\theta 2$) are related to the triangles formed with lower small vectors as shown in Fig. 5(a) whereas the other two limit angles ($\theta 3$ and $\theta 4$) are associated with the triangles formed with positive small vectors as shown in Fig. 5(b). For the simplicity of subsequent calculations, dc-link voltages are transformed into two variables *x* and *y* using (5). These two values are directly related to the lengths of triangles as marked in Fig. 4. Limit angles are calculated using (6)–(10), where α is an intermediate variable.

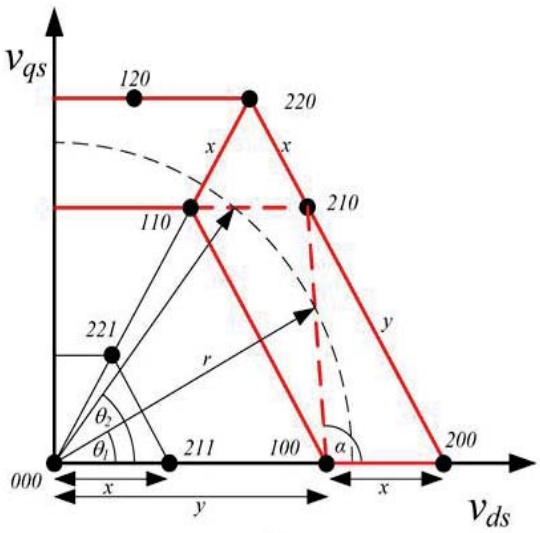

Fig.4 (a) : Limit Angles for Triangles Formed with Lower Small Vectors

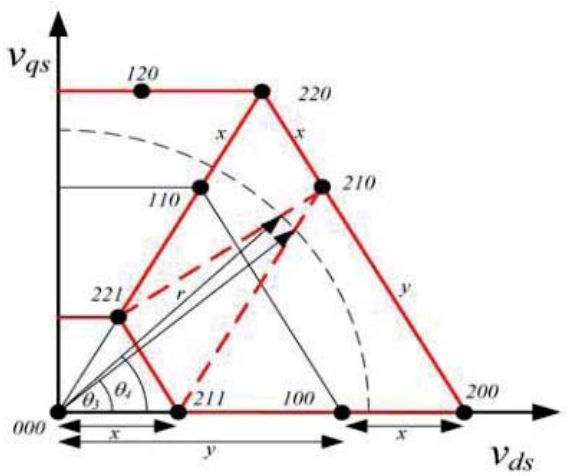

Fig. 4 (b) : Limit Angles for Triangles Formed with Upper Small Vectors

$$x = \frac{2}{3}V_U , \qquad y = \frac{2}{3}V_L \tag{5}$$

$$\alpha = \sin^{-1}\left(\frac{\sqrt{3}y}{2\sqrt{(x+y)^2-3xy}}\right) \tag{6}$$

$$\theta_1 = \alpha - \sin^{-1}\left(\frac{\sqrt{3}y^2}{2r\sqrt{(x+y)^2-3xy}}\right) \tag{7}$$

$$\theta_2 = \sin^{-1}\left(\frac{\sqrt{3}y}{2r}\right) \tag{8}$$

$$\theta_3 = \frac{\pi}{3} - \sin^{-1}\left(\frac{\sqrt{3}x}{2r}\right) \tag{9}$$

$$\theta_1 = \alpha - \frac{\pi}{3} - \sin^{-1}\left(\frac{x}{r}\sin\left(\alpha - \frac{2\pi}{3}\right)\right) \tag{10}$$

$$z = d_1V_1 + d_2V_2 + d_3V_3 \tag{11}$$

$$d_1 + d_2 + d_3 = 1 \tag{12}$$

The limit angles given in (7)–(10) are valid only for sector 1. Once the limit angles are calculated, the triangle and corresponding three vectors can easily be derived. After finding the three vectors, the next step is to determine switching times. According to the well-known volt-second balancing principle, a given reference vector can be synthesized by three adjacent vectors. Equations (11) and (12) provide the mathematical description of this process. Equations (13)–(16) are used to calculate corresponding switching times *d*1 − *d*3 that are expressed as fractions of the sampling time.

$$\Delta = (x_1y_2 - x_2y_1) + (x_2y_3 - x_3y_2) + (x_3y_1 - x_1y_3) \tag{13}$$

$$d_1 = \frac{(x_0(y_2 - y_3) + y_0(x_3 - x_2)) + (x_2y_3 - x_3y_2)}{\Delta} \tag{14}$$

$$d_2 = \frac{(x_0(y_3 - y_1) + y_0(x_1 - x_3)) + (x_3y_1 - x_1y_3)}{\Delta} \tag{15}$$

$$d_3 = \frac{(x_0(y_1 - y_2) + y_0(x_2 - x_1)) + (x_1y_2 - x_2y_1)}{\Delta} \tag{16}$$

Where (*xn, yn*)*n* = 0, . . . , 3 are the coordinates of vector points.

IV. Simulation and Results

The five level diode clamped multilevel inverter simulation results and analysis describe in this section. It has described open loop and closed loop output of DCMLI phase voltage of DCMLI,

a) Simulation Diagram for PV System

The simulation diagram for five levels DCMLI with PV is shown in the Figure 5.The PV is used as the input source. The PV simulation model diagram is given below with clearly. in this two Panels are connected.

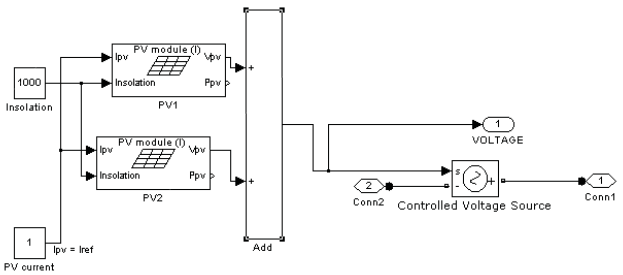

Fig 5 : Simulation Diagram for PV System

b) Simulation Diagram for Open Loop Diode Clamped Multilevel Inverter

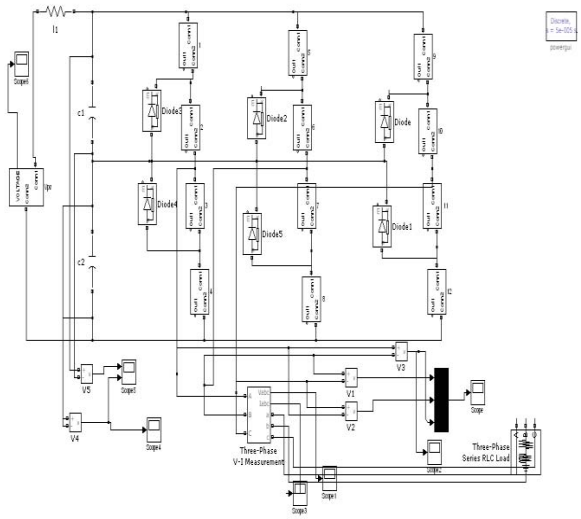

Fig 6 : Simulation Diagram for Open Loop Diode Clamped Multilevel Inverter

The simulation diagram for open loop DCMLI with PV is shown in the Figure 6.The modeling of five levels DCML inverter has been developed by using MATLAB. The simulation model parameters are given in

table 3.With the use of this proposed method harmonics are eliminated. Therefore the efficiency of inverter is increased.

c) Simulation Diagram for Space Vector Modulation

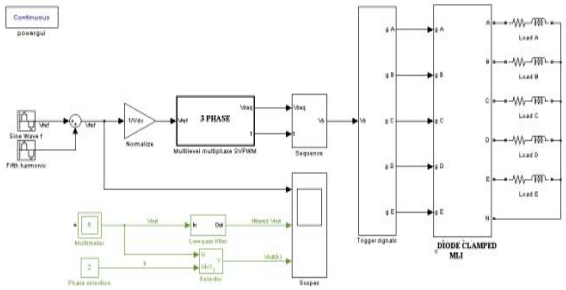

Fig. 7 : Simulation Diagram for SVPWM Techniques

The simulation diagram for space vector Modulation is shown in Figure 7.With the use of this proposed method harmonics are eliminated. Therefore the efficiency of the inverter is increased. Some soft switching method can be used for multilevel inverter to reduce the switching loss and to increase the efficiency.

d) Simulation Diagram for DCMLI with SVPWM

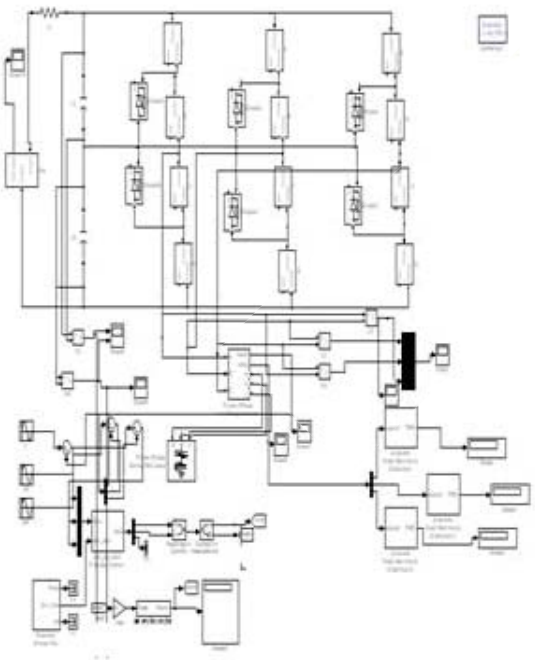

Fig. 8 : Simulation Diagram for DCMLI with SVPWM

The simulation of DCMLI with SVPWM is shown in the figure.8. This is done by using space vector PWM.A reference signal is compared with two triangular carrier signals that are phase shifted by 90 degree. The resulting PWM signals control the corresponding switches. This control strategy is used to get accurate five level stepped outputs for Diode clamped multilevel inverter.

V. Result and Analysis

a) Simulation Waveform for Photovoltaic System

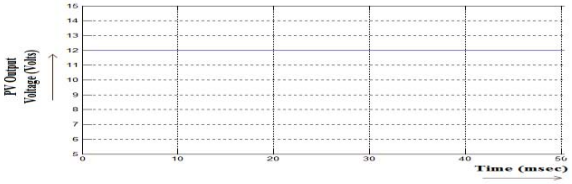

Fig. 9 : Input Voltage from Solar Panel

An input voltage of 12V is shown in the Figure 9.An accurate PV module electrical model is presented based on the Shockley diode equation. The general model was implemented on MALTAB scrip file, and accepts irradiance and temperature as variable parameters and outputs the I-V characteristic.

b) Simulation Waveform for Open Loop

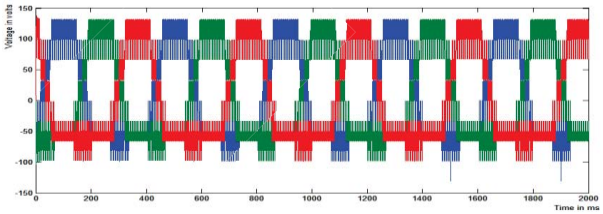

Fig. 10 : Output Voltage Waveform for Open Loop

The output of DCML Phase voltage is shown in Figure 10.It has 100V, 50 Hz frequency. The phase voltage has three levels, positive half cycle of hundred volts and negative half cycle of hundred voltages. The five level output are in stepped waveform the X-axis consists of time period in milliseconds and Y- axis consists of voltage in volts.

c) Simulation Waveform for Space Vector Modulation

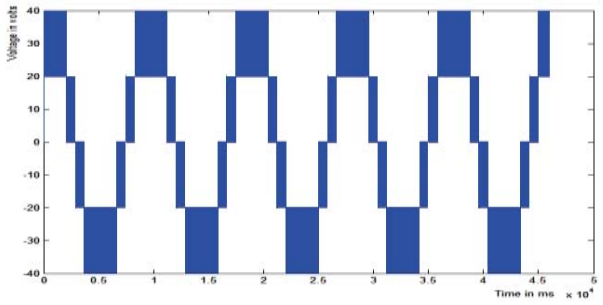

Fig. 11 : Space Vector Modulation Output Voltage

The Space Vector Modulation Output Voltage is shown in Figure 11.It has 40V, 50 Hz frequency. The phase voltage has five levels, positive half cycle of fourty volts and negative half cycle of fourty voltage. The five level output are in stepped waveform the X-axis consists of time period in milliseconds and Y- axis consists of voltage in volts.

d) Line Voltage Waveforms of the Diode Clamped Multilevel Inverter Output

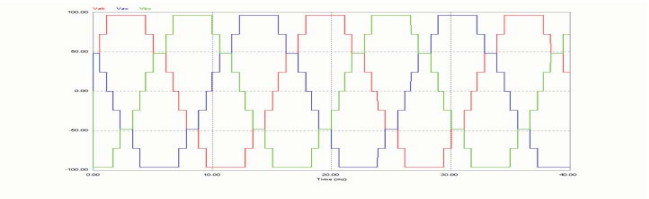

Fig. 12 : Line Voltage Waveforms of the DCMLI

The Figure 12 is the Line Voltage Waveforms of the Diode Clamped Multilevel Inverter Output.

It has 100V, 50 Hz frequency. The phase voltage has five levels, positive half cycle of hundred volts and negative half cycle of hundred voltages. The five level output are in stepped waveform the X-axis consists of time period in milliseconds and Y- axis consists of voltage in volts.

e) Simulation Waveform for DCMLI with SVPWM

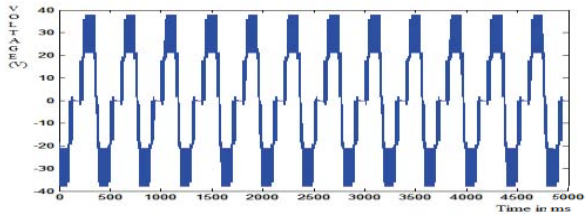

Fig. 13 : Closed Loop Inverter Output Voltage

The output of Diode clamped multilevel inverter with space vector modulation phase voltage closed loop inverter output voltage is shown in Figure 13.It has 40V, 50 Hz frequency. The phase voltage has five levels, positive half cycle of hundred volts and negative half cycle of hundred voltages. The five level output are in stepped waveform the X-axis consists of time period in milliseconds and Y- axis consists of voltage in volts.

f) Total Harmonics Distortion Analysis

The Total Harmonics Distortion for open loop system is given figure 14.

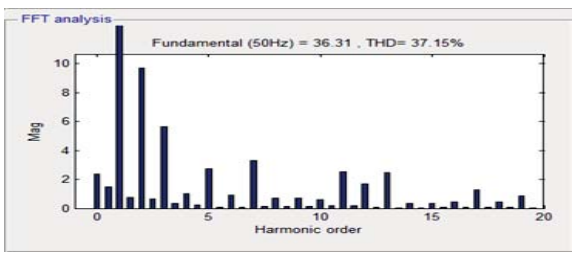

Fig. 14 : THD Analysis for Open Loop System

The figure 14 Total Harmonics Distortion for open loop system. The Total harmonic distortion of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. THD is used to characterize the linearity of audio systems and the power quality of electric power systems.

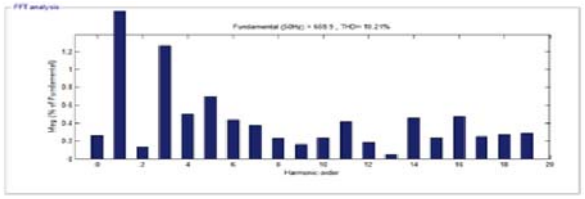

Fig. 15 : Total Harmonics' Distortions waveform for Closed Loop System with SVM

The figure 15 Total Harmonics Distortion for closed loop system. In power systems, lower THD means reduction in peak currents, heating, emissions, and core loss in motors. The output voltage THD is less than 12%. Thus by using the proposed scheme THD and switching losses are reduced.

Table 2 : THD comparison

Kind of the MLI	2 Level MLI	3 Level MLI	5 Level Proposed MLI
THD	58.84%	53.84%	10.16%

From the table 3 different inverter THD values are compared. The proposed inverter THD value is obtained as 10.16%, which is the best among all. This shows that quality of the five level inverter is improved.

V. Conclusion

This paper is the first step to develop a complete solar photovoltaic power electronic conversion system in simulation. The Proposed topologies eliminate the need for additional dc–dc converters by connecting two battery banks, two super capacitor banks or a battery bank, and a super capacitor bank directly across dc links of a diode clamped five-level inverter. Unavoidable dc-link voltage imbalance is the major issue with these topologies. This problem is handled by a novel space vector modulation technique. Further work is needed to improve the efficiency by reducing THD and the hardware will be designed for different power levels. The THD values for the Traditional, Conventional and proposed inverters are compared and analysed.

References Références Referencias

1. AlirezaNami, and FiruzZare,[2011] "A Hybrid Cascade Converter Topology with Series-Connected Symmetrical and Asymmetrical Diode-Clamped H Bridge Cells" IEEE Transactions on Power Electronics, Vol. 26, No.1,PP: 51-65.
2. Anshuman Shukla, and Arindam Ghosh, [2010] "Flying-Capacitor-Based Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multilevel Inverter" IEEE Transactions on Industrial Electronics, Vol. 57, No. 7,PP: 2249-2261.

3. Arash A. Boora and AlirezaNami,[2010] "Voltage-Sharing Converter to Supply Single-Phase Asymmetrical Four-Level Diode-Clamped Inverter with High Power Factor Loads. IEEE Transactions on Power Electronics, Vol. 25, No. 10, PP: 2507-2520.
4. AshishBendre and Slobodan Krstic, [2005] "Comparative Evaluation of Modulation Algorithms for Neutral-Point-Clamped Converters" IEEE Transactions on Industry Applications, Vol. 41, No. 2, PP: 634-643.
5. BehzadVafakhah and Jeffrey Ewanchuk,[2011] "Multicarrier Interleaved PWM Strategies for a Five-Level NPC Inverter Using a Three-Phase Coupled Inductor" IEEE Transactions on Industry Applications, Vol. 47, No. 6,PP: 2549-2558.
6. Berkouk, and C. Saudemont, September [2007] "DC Link Capacitor Voltage Balancing in a Three-Phase Diode Clamped Inverter Controlled by a Direct Space Vector of Line-to-Line Voltages" IEEE Transactions on Power Electronics, Vol. 22, PP: 1636-1648.
7. GaminiJayasinghe, and D.MahindaVilathgamuwa, [2011]"Diode-Clamped Three-Level Inverter-Based Battery/Super capacitor Direct Integration Scheme for Renewable Energy Systems. IEEE Transactions on Power Electronics, Vol. 26, No. 12, PP: 3720-3729.
8. EnginOzdemir, and SuleOzdemir, [2009] "Fundamental-Frequency-Modulated Six-Level Diode-Clamped Multilevel Inverter for Three-Phase Stand-Alone Photovoltaic System" IEEE Transactions on Industrial Electronics, Vol. 56, No. 11, PP: 4407-4415
9. Hirofumi Akagi and Kazunori Hasegawa,[2011] "A New DC-voltage-Balancing Circuit Including a Single Coupled Inductor for a Five-Level Diode-Clamped PWM Inverter" IEEE Transactions on Industry Applications, Vol. 47, No. 2,PP: 841-852.
10. Huafeng Xiao, and ShaojunXie,[2012] "Transformer Less Split-Inductor Neutral Point Clamped Three-Level PV Grid-Connected Inverter" IEEE Transactions on Power Electronics, Vol. 27, No. 4,PP: 1799-1808.
11. Jeffrey Ewanchuk, and John Salmon,[2011] "A Five-/Nine-Level Twelve-Switch Neutral-Point-Clamped Inverter for High-Speed Electric Drives" IEEE Transactions on Industry Applications, vol. 47, no. 5,PP: 2145-2153.
12. Jose I. Leon and Sergio Vazquez,[2009] "Three-Dimensional Feed Forward Space Vector Modulation Applied to Multilevel Diode-Clamped Converters" IEEE Transactions on Industrial Electronics, Vol. 56, No. 1,PP: 101-109.
13. Kazunori Hasegaw and Hirofumi Akagi,[2011] "A New DC- voltage-Balancing Circuit Including and Single Coupled Inductor for a Five –Level Diode Clamped PWM Inverter" IEEE Transactions on Industry Applications, Vol. 47, No. 2,PP: 841-852.
14. Kazunori Hasegawa and Hirofumi Akagi, [2012] "Low Modulation – Index Operation of a Five Level Diode Clamped PWM Inverter with DC-voltage-Balancing circuit for a motor drive" IEEE Transactions on Power Electronics, Vol. 27, No. 8,PP: 3495-3504
15. Masaaki Takagi and Yumiko Iwafune, [2012] "Economic Value of PV Energy Storage Using Batteries of Battery-Switch Stations" IEEE Transactions on Sustainable Energy, PP: 1-10.