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Three-Point Binary Median Filter Implementation using Single-Electron Transistor

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Three-Point Binary Median Filter Implementation using Single-Electron Transistor

Anbarasu Paulthurai [α], Balamurugan Dharmaraj [σ] & S. Rajasekaran [ρ]

Abstract - Non-linear filters are large family of filters used in signal and image processing. They have found numerous applications such as in digital image restoration, speech processing and coding, digital TV applications, etc. In this paper, three-point median filter is designed using single-electron transistor. In single-electron transistor bits of information are represented by the presence or absence of electrons at conducting islands. Single Electron Transistor (SET), distinguished by a very small device size low power dissipation, high speed and high performance, is one of the most promising nano electronics devices to replace conventional CMOS. The SET technology offers the ability to control the motion of individual electrons in the designed circuits . The Non-linear filter is simulated using a Monte Carlo technique by PSPICE9.1 and their correct and stable logical operation is confirmed.

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I. Introduction

The downscaling of complementary metal-oxide semiconductor (CMOS) technology is still in rapid progress and the increase in power consumption has become a major limiting factor in constructing large-scale integrated circuits. Consequently, the single-electron transistor (SET) has attracted considerable attention in recent years because of its potential for high packing density and low power consumption.[1] A variety of useful devices and concepts utilizing the single-electron tunneling features, such as, cellular automata, the binary decision diagram device,[2] and SET logic gates,[3,4] have been proposed and tested by actual devices.

To operate a SET circuit at room temperature, Coulomb islands constituting the circuit should be made extremely small to provide large charging energy that is sufficient to overcome thermal agitation. However, since the operation of a SET is strictly controlled by the amount of charge induced at the center island, reducing capacitances by scaling of a device should be accompanied by increased voltage and current levels.

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Thus, in contrast to the MOS transistor, the power consumption of a SET increases as the possible operation temperature rises, and the possibility of the integration of above $10^{11}/cm^2$ is questionable, since on the order of 10^{-9} W will be dissipated per elementary gate at room temperature [5].

Non-linear filters include well-known filter classes, such as rank order filters (median, min, max, etc.), morphological filters (opening, closing), etc. Rank order filters exhibit excellent robustness properties and provide solutions in many cases, where linear filters are inappropriate. Linear filters have poor performance in the presence of noise that is not additive as well as in cases, where system non-linearities on non-Gaussian statistics are encountered [6].

In this paper we present the implementation of three-point median filter using single-electron transistor. The single-electron transistor circuits have been designed and simulated using a Monte Carlo method [7].

II. Single-Electron Circuits

Single-electron circuits consist of conducting islands, tunnel junctions, capacitors, and voltage source. The islands are arbitrarily connected with tunnel junctions, capacitors and voltage sources. The basic principle of single electronics is that one needs Coulomb energy E_c to charge an island with an electron. This energy is:

$$E_c = \frac{e^2}{2C_i} \quad (1)$$

Where C_i is the capacitance as 'seen' by the island and e is the elementary charge. Electrons tunnel independently from island through tunnel junctions. To assure that electron states are localized on islands all tunnel resistances must be larger than the fundamental resistance R_q:

$$R > R_q = \frac{h}{e^2} \cong 25{,}813\ \Omega \quad (2)$$

Where h is Planck's constant.

To simulate the tunneling of electrons from island to island in a single-electron circuit, one has to determine the rates of all possible tunnel events. The tunnel rate of a possible tunnel event depends on the change in the circuit's free energy caused by this particular event [8]. The free energy F of a single-electron circuit is the differences of the electronic

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energy, U stored in its capacitances and the work done by the voltage sources of the circuit W:

$$F = U - W \tag{3}$$

The electrostatic energy is given by:

$$U = \frac{1}{2}(q, v)\begin{pmatrix} V \\ Q \end{pmatrix} \tag{4}$$

Where, q and v are the unknown parts of the island charge and voltage matrices, respectively, and Q and V are the known parts of the island charge and voltage matrices, respectively. The work done by the voltage sources is given by:

$$W = \sum_n \int V_n(t) i_n(t) dt \quad (5) \tag{5}$$

Where $\mathrm{V}_n(\mathrm{t})$ is the voltage of the n^{th} voltage source and $\mathrm{i}_n(\mathrm{t})$ is the current through the n^{th} voltage source.

The tunnel rate $r$for a particular tunnel event is given by:

$$\mathrm{r} = \frac{\Delta F}{\left(e^2 R_T\left(1 - exp\left(\frac{-\Delta F}{kT}\right)\right)\right)} \tag{6}$$

Where ΔF is the change in free energy caused by this particular tunnel event, (index) $\mathrm{R_T}$ is the tunnel resistance of the tunnel junction through which the electron is transported, and kT is the thermal energy (k is the Boltzmann's constant, and T is the temperature). Once the tunnel rates for all possible tunnel events are known the actually occurring event is determined using a Monte Carlo method combined with an exponential distribution of tunnel events [8]. The time duration of a particular event is given by:

$$\Delta \mathrm{t} = -\frac{\ln(r)}{\mathrm{r}} \tag{7}$$

Where r is an evenly distributed random number in the interval [0, 1]. Among all possible tunnel events, the event with the shortest time duration takes place [9].

a) The SECS simulator

SECS is a single electron circuit simulator based on the Monte Carlo method. The circuit is designed using ORCAD Capture CIS. A single electron component library has been developed for this purpose. This library includes the components of node, ground node, capacitor, tunnel junction and source. The node component can be used either as potential node or charge node. In the second case the background charge can be set to a desired value. The tunnel junction parameters are its capacitance and resistance. The resistance of a tunnel junction includes the modeling of the density of states and the transmission probability. In the single electron component library there are five types of sources, constant, linear, pulse, sinusoidal and a combination type source, which is used when a combination of values between two or more sources is needed, as for example in the stability plot diagram. This design environment provides great convenience for designing and manipulating large circuits.

The simulation uses the description of the circuit provided by ORCAD. Initially SECS parses the description of the circuit and performs a circuit error check. Then the simulation is initiated according to the parameters of temperature and simulating time defined. During the simulation, the free-energy of the circuit at each time step is calculated. Then the difference of the circuit's free energy is calculated for every possible tunnel event DF. From the difference of the circuit's free energy a rate, G, is calculated for all possible events. The tunneling rate is used to calculate the time interval t, for every event to appear. The event that will eventually take place is the one that corresponds to the smallest time interval. The voltages and charges are updated according to the chosen tunnel event and the time advances according to$t$. Following this procedure by the time that the simulation ends the macroscopic behavior of the circuit is determined. This algorithm provides a real time simulation of the behavior of the circuit. Simulation results are obtained in a graphical form of plots of voltage, current, charge and free-energy versus time [10].

III. Power Consumption in Set Circuits

In general, there are three components that constitute the amount of power consumed in circuit operation: dynamic, short-circuit, and leakage power. The dynamic power is consumed due to the charging and discharging of the output capacitance C_L when logic switching occurs, and thus, is inevitable in circuit operation. Short-circuit power occurs when both the nSET and pSET are turned-on simultaneously, conducting short-circuit current from the supply to the ground. The power resulting from the short-circuit current is only a minor fraction of the total dissipation, as long as the output transient times are relatively large compared to the input rise and fall times. However, the short-circuit power in SET circuits is also a function of operation temperature, and, as the temperature increases, it make up a considerable portion of the total power.

The most significant component of the power consumed in the SET circuit is the leakage power. An ideal complementary circuit does not dissipate power when the input does not change. However, in a circuit composed of SETs, leakage power is dissipated by the thermal enhancement of normal tunneling and co-tunneling. The static leakage power due to the thermal enhancement of normal tunneling makes up a considerable portion of the total power as the operation temperature increases.

Because the dynamic power has a quadratic dependence on the supply-voltage, and both the current

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level and voltage level rise as the dimensions of SETs are scaled down, supplyvoltage scalability, while device parameters[11].

IV. Basic Single-Electron Logic Gates

a) The single-electron and gate

The SET AND gate is shown in Fig. 1. The circuit comprises Six Single Electron Transistor (3 nSET and 3 pSET). Instead of two paralleled sourcing (upper) transistors connected to V_{dd} and two series-connected sinking (lower) transistors connected to ground. As with the NAND gate, SET transistors U_1 and U_3 work as a complementary pair, as do transistors U_2 and U_4. Each pair is controlled by a single input signal. If either input A or input B are "high" (1), at least one of the lower transistors (U_3 or U_4) will be saturated, thus making the output "low" (0). Only in the event of both inputs being "low" (0) will both lower transistors be in cutoff mode and both upper transistors be saturated, the conditions necessary for the output to go "high" (1).The AND function built up from the basic NAND gate with the addition of an inverter stage on the output. The voltage V_{dd} is constant and its value is 25mV.

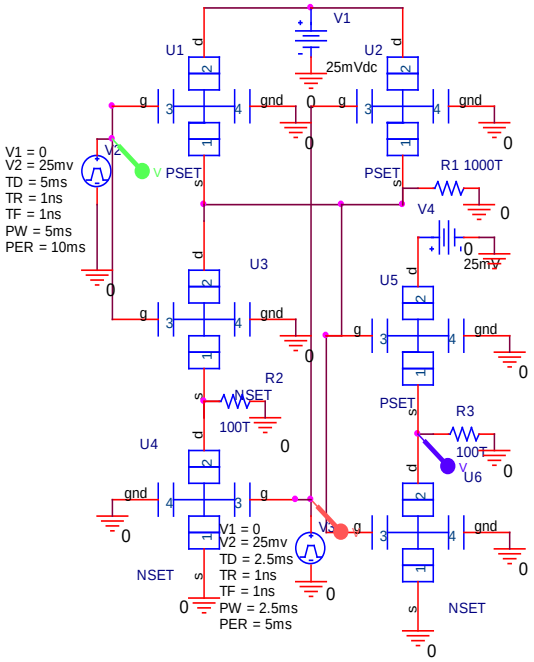

Figure 1 : Internal Circuit of AND gate

The operation of the AND gate is shown in Fig. 2. Fig. 2(a) and (b) shows the time variation of input voltages V_1 and V_2, respectively. The inputs are piece-wise constant and apply all possible combinations of logic '0' and '1' to the gate. Fig. 2(c) shows the time variation of output voltage.

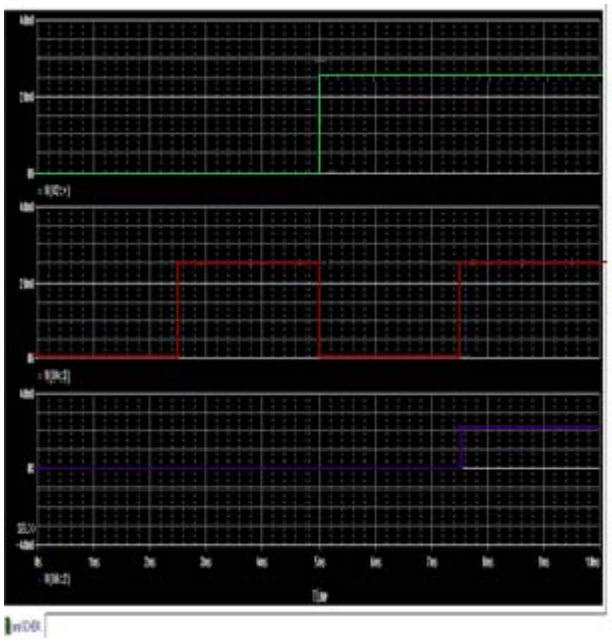

Figure 2 : Simulated input (A, B) and Simulated output (C)

b) The single-electron OR gate

The SET OR gate is shown in Fig. 3. The circuit comprises eight Single Electron Transistor (4 nSET and 4 pSET). As with the NOR gate, SET transistors U_1 and U_4 work as a complementary pair, as do transistors U_2 and U_5 likeU_3 and U_6. Each pair is controlled by a single input signal. In this circuit upper transistors U_1, U_2 and U_3areserially connected and lower transistors U_4, U_5 and U_6 connected in parallel sourcing to ground. As with the NOR gate, SET transistors U_1 and U_3 work as a complementary pair, as do transistors U_2 and U_4. Each pair is controlled by a single input signal. If both the input A and input B are "high" (1), both the lower transistors (U_3 and U_4) will be saturated, thus making the output "low" (0).

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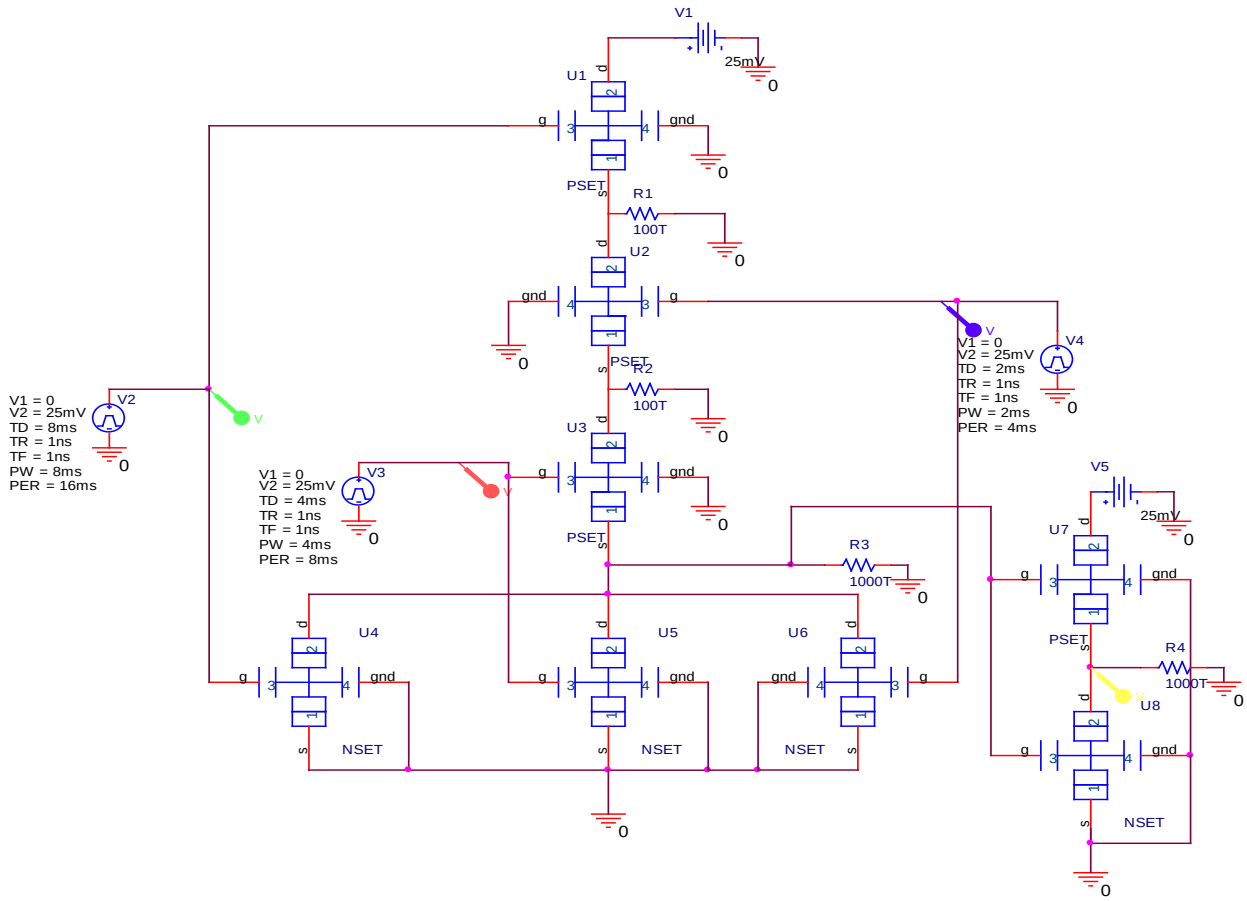

Figure 3 : Internal Circuit of OR gate

Only in the event of both inputs being "low" (0) will both lower transistors be in cutoff mode and both upper transistors be saturated, the conditions necessary for the output to go "high" (1).The OR function built up from the basic NOR gate with the addition of an inverter stage on the output. The voltage V_{dd} is constant and its value is 25mV.

The operation of the OR gate is shown in Fig. 4. Fig. 4(a), (b) and (c) shows the time variation of input voltages V_1, V_2 and V_3, respectively. The inputs are piece-wise constant and apply all possible combinations of logic '0' and '1' to the gate Fig. 4(d) shows the time variation of output voltage

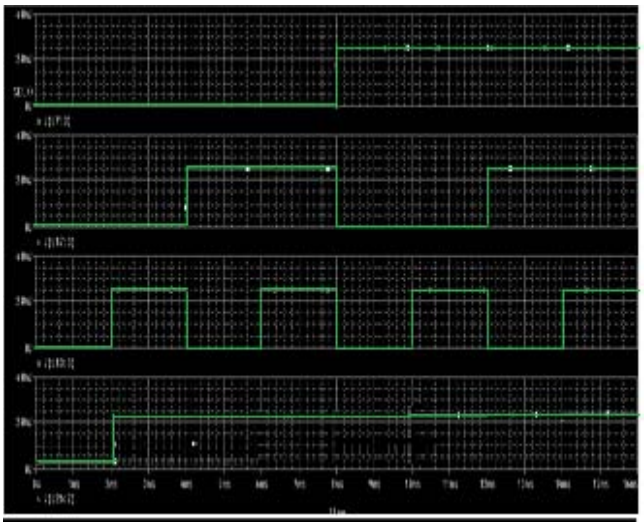

Figure 4 : Simulated input (A B C) and Simulated output (D)

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V. The Binary Median Filter

A commonly employed filter for restoring binary images is the median filter. Given a window W containing an odd number of pixels, say n, the binary median filter is defined in the following manner for each pixel z, W is translated to z and the filter outputs 1 if more than n/2 pixels in W_z are onevalued; otherwise the filter outputs 0. Medians are used to suppress impulse noise and exhibit good edge preservation if not excessive and uncorrupted image does not possess much fine detail.

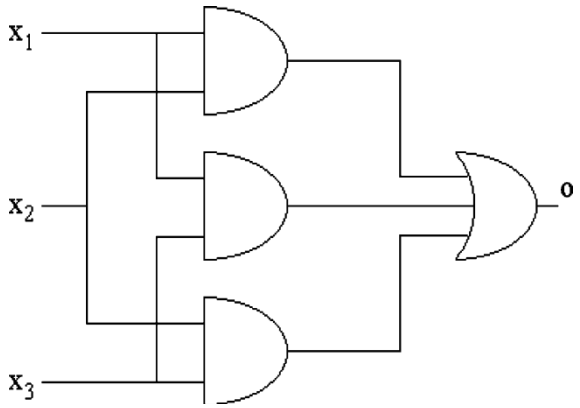

Figure 5 : Logic circuitry for three-point binary median filter implementation

A Boolean function is a binary function $h(x_1,x_2.x_n)$ defined on n binary variables [12]. Since each variable can take on two values, 0 or 1, there are 2^n possible arguments for h. In conjunction with a window W, a Boolean function defines a binary window operator J on binary images via the one to-one correspondence between the variables and pixels in the window. J(A) is defined at a pixel z by translating the window to z and applying the Boolean function h to the binary values in the translated window. As an example, consider the median function. The window consists of three pixels. For instance, it might be the pixel at which the value is being computed together with its left and upper neighbors. Or it might be a three-point filter defined on a binary digital signal, which is a subset of the set Z of integers or, equivalently, an one-dimensional string of 0 and 1 s. Logically [12],

$$h(x_1;x_2;x_3) = x_1x_2+x_1x_3+x_2x_3$$

If the input signal is

000001100100111011000111100000

Then, the filtered output is

000001100000111111000111100000

The filter is implemented by the gate structure shown in Fig. 5.

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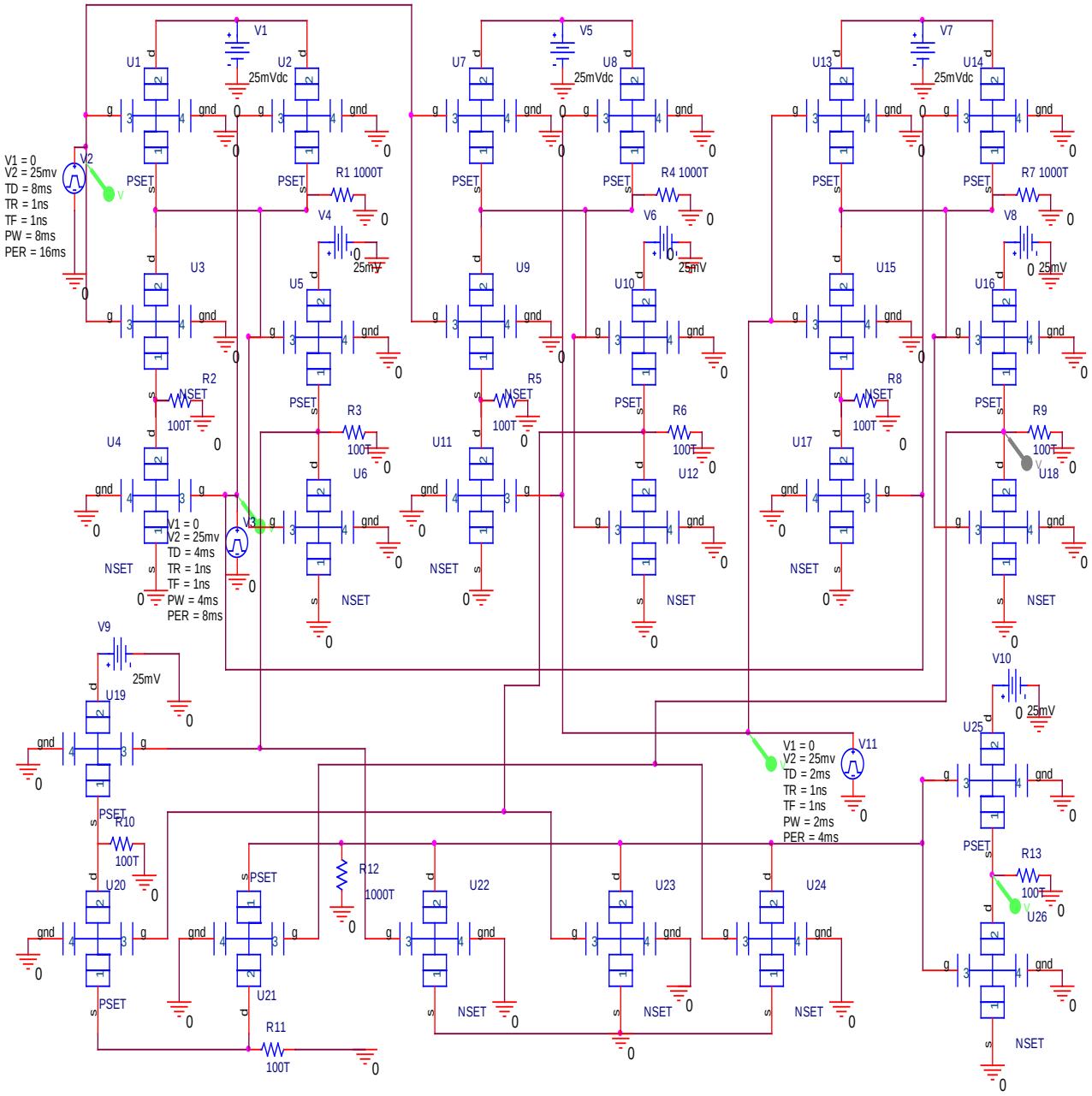

Figure 6 : The single-electron circuit for the three-point binary median filter

The single-electron circuit for the three-point binary median filter is shown in Fig. 6. The single-electron filter comprises three two-input single-electron AND gates and one three-input single-electron OR gate. The single-electron AND gate comprises three NSET and three PSET which are U_1–U_6. The OR gate comprises four NSET and four PSET which are U_{19}–U_{26}. The inputs X_1–$X_3$and the output of the logic circuit shown in Fig. 5, correspond to the input voltages V_1–V_3 and the output voltage of single-electron circuit is shown in Fig. 6. Power to the single-electron circuit is supplied by the voltage sources V_1, V_4-V_{10}. These voltage sources are all equal and are connected to drain. The ground voltages, all equal to $0V$. The input voltages are applied to the gate of the SET and, therefore, no electron transport from the voltage sources to the circuit or vice-versa is possible. The output of the three AND gates, are connected to the inputs of the OR gate.

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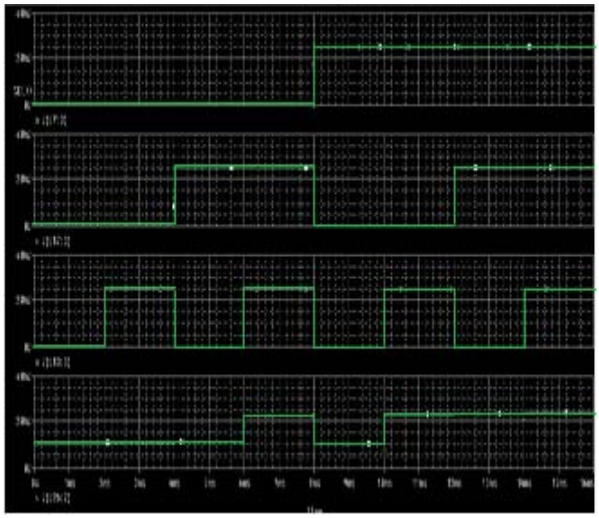

Figure 7 : The operation of the single-electron three-point binary median filter. (a)–(c) Time variations of the input voltages V1–V3, respectively. (d) Time variation of the charge at the output node N14

Fig. 7 shows the operation of the single-electron three point binary median filter. The time variations of the input voltages V1, V2 and V3 are shown in Fig. 7(a)–(c), respectively. The input voltages are piece-wise constant and apply all possible combinations of logic '0' and '1' to the filter. Fig. 7(d) shows the time variation of the voltage at the output. The voltage V_0 at the output section varies from $0$to $25mV$. The electron is well confined into the output section and the single-electron operation is stable.

VI. Conclusion

The imaging algorithms tend to be computationally intensive, especially when directly implemented on standard sequential hardware. Real-time processing for digital imaging concerns efficient deterministic implementation of algorithms. In this paper we designed a three-point median filter using nano electronic single electron circuitry. This nano electronic filter was simulated by using *PSPICE 9.1* at the voltage of$25mV$. The proposed non-linear filter is constructed by 26 transistors and 13 resistors, using single electron transistor (SET) .The proposed three-point median filter implementation using single-electron transistor has the potential advantages of less power, smaller area requirements and faster processing compared to conventional microelectronic implementation.

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