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An Adder with Novel PMOS and NMOS for Ultra Low Power Applications in Deep Submicron Technology

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Abstract- Power has become a burning issue in modern VLSI design, as the technology advances especially below 45nm technology, Leakage power become more problem apart of the dynamic power. This paper presents a full adder with novel PMOS and NMOS which consume less power compare to conventional full adder and DTMOS full adder, this paper shows different types of adders and their power consumption, area and delay. All the experiments have been carried out using cadence virtuoso design lay out editor which shows power consumption of different types of adders[1-2].

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I. Introduction

The adder is one of the most critical components of a central processing unit. The object of the adders not only adding of bits but also involves in address calculation, subtraction, division and multiplication, the adders are critical components to determine the speed, delay and power of the overall system, low power adders are always preferable. Due to the popularity of portable electronic products low power system has attracted more attention in recent years, an system on chip (SOC) design can contain more and more components that lead to a higher power density. This makes power dissipation reach the limits of what packaging, cooling or other infrastructure can support, reducing the power consumption not only can enhance battery life but also can avoid the overheating problem which would increase the difficulty of packaging or cooling. Therefore the consideration of power consumption in complex SOCs has become a big challenge to designers, moreover in modern VLSI designs [3-5].

Lowering power is one of the greatest challenges facing the IC industry Today, temperature profile and battery life requirements for tethered and un tethered systems have made power consumption a primary optimization target for IC industry[2]. IC power consumption consists of three basics components: switching power, short circuit power and leakage power[6-7].

$$\text{Dynamic power } P_D = \frac{1}{2} C_L f V_{DD}^2 \quad (1)$$

Dynamic power is square of supply voltage, therefore by reducing supply voltage we can reduce dynamic power [8].

The leakage power is mainly due to sub threshold current and it may be defined as the drain to source current of the transistor operating in the weak inversion region of MOSFET this subthreshold leakage may be defined as in eq (2) give s a simple method for estimating the leakage current in a single NMOS transistor[9-11].

$$I_s = I_0 \exp\left[\frac{(V_{gs} - v_t)}{\eta V_t}\right]\left[1 - \exp\left(\frac{V_{ds}}{v_t}\right)\right] \quad (2)$$

V_t is the thermal voltage and is given by Q/KT and n is the sub threshold slope coefficient. Generally there are varies leakage reduction techniques based on mode of operation of systems the two operation modes are active mode and stand by mode or idle mode. Most of the leakage power reduction techniques will be based on idle mode [12].

SECTION2: gives an overview of the Novel PMOS and NMOS and their simulation results, SECTION3 presents Novel 3 bit full adder and conventional full adder, SECTION 4 describes experimental results of conventional, Novel full adders and DTMOS full adders, SECTION5gives conclusions.

II. An Over View of Novel PMOS and NMOS

Ultra low power operation plays a major role in designing of CMOS circuits in subthreshold regime, for any digital or analog design the basic components are PMOS and NMOS devices, the power consumption of this basic elements determine the overall power of the system. In this section we provide Novel PMOS and NMOS, simulations have been carried out in cadence design frame work to verify the functionality of the technique, the functionality of the both the PMOS and NMOS is verified at 180nm and 45 nm technology[13].

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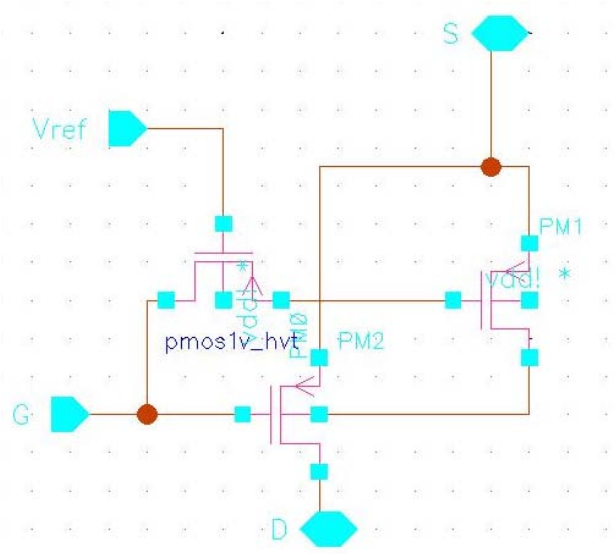

Figure 1 : Novel PMOS

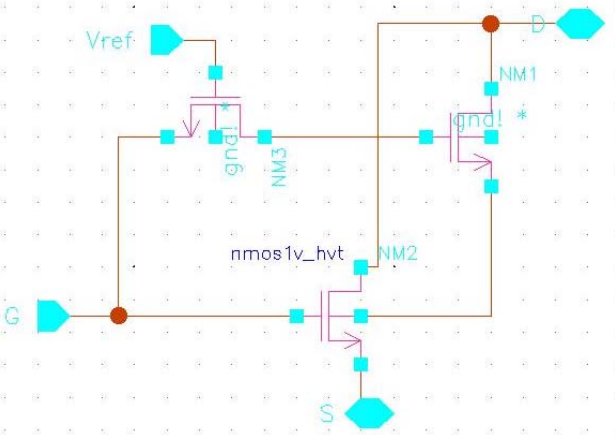

Figure 2 : Novel NMOS

III. A Conventional CMOS Adder

The 28 transistor full adder is the pioneer traditional adder circuit, the schematic of this adder is shown. This adder cell is built using equal number of NFET and PFET transistors, the MOS logic can be realized using equations [1].

$$\text{Carry: } AB+BC+AC \quad (2)$$

$$\text{SUM: } ABC+(A+B+C)C \quad (3)$$

The conventional full adder consumes more power compared to Novel full adder, both conventional and Novel full adders are simulated and their average power is calculated [14].

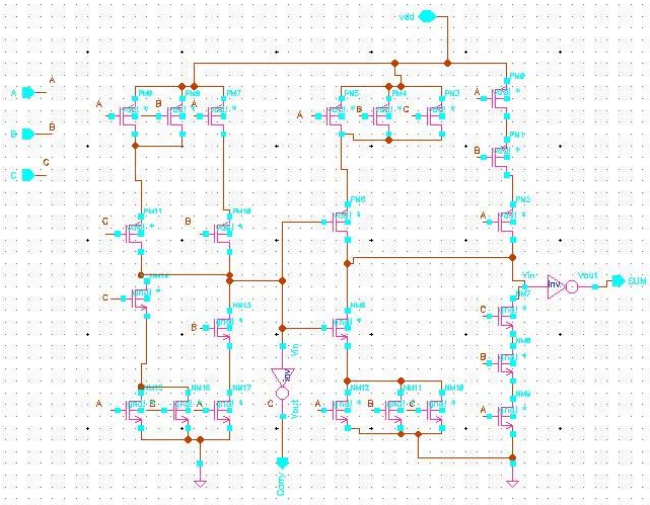

Figure 3 : Conventional full adder

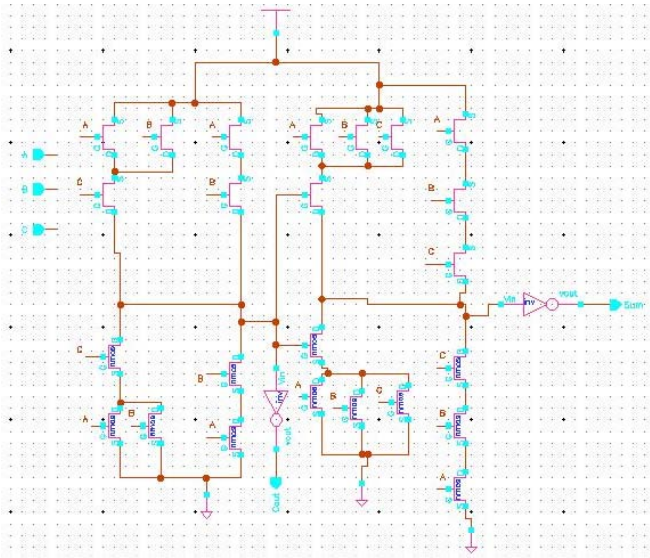

Figure 4 : Full adder with novel PMOS and NMOS

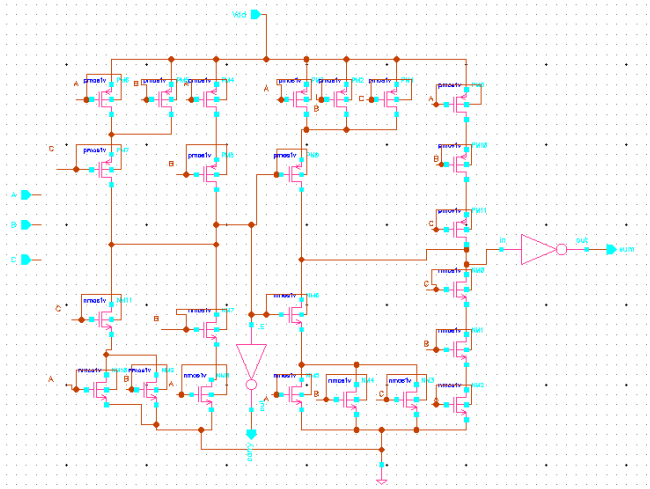

Figure 5 : DTCMOS Full adder

IV. Simulation Results and Analysis

An investigation has been carried out for calculating average power, static power of conventional full adder and the Novel full adder and compared their powers at 45nm technology using virtuoso design environment.

A novel CMOS adder may have an overhead area, but it consumes less power [15].

Table 1 : Power Comparison Table @45nm, Supply Voltage Is 0.6v

Parameter	Full Adder With Novel PMOS & NMOS	Conventional CMOS full adder	DTCMOS full adder
Avg. Power	97.23nw	105.8nw	243nw
Delay	150ps	580ps	291ps
PDP	1.456×10-17	61×10-15	7.07×10-17

Table 2 : Power Delay Comparison Table of Conventional CMOS Full Adder Versus Novel Full Adder at 45nm and Supply Voltage Is 1.1v

Parameter	Full Adder With Novel PMOS & NMOS	Conventional CMOS full adder
Avg. power	0.43μw	1.88μw
Delay	72ps	43ps
PDP	3.152×10^{-17}	8.084×10^{-17}

Table 3 : Power and Delay Comparison of Novel Full Adder and Conventional Full Adder with Supply Voltage of 1.1v @180nm

Parameter	Full Adder With Novel PMOS & NMOS	Conventional CMOS full adder
Avg. power	69.49μw	32.8μw
Delay	217ps	166ps
PDP	15×10^{15}	5.45×10^{15}

Table 4 : Static Power Comparison Table of Novel Full Adder, DTCMOS Full Adder and Conventional Full Adder at 45nm with 0.6v

Parameter	Full Adder With Novel PMOS & NMOS	Conventional CMOS full adder	DTCMOS full adder
Static power when all inputs are at 0.6v	9.159pw	8.688pw	109.4nw
Static power when all inputs are at 0v	14pw	8.756pw	78nw

Table 5 : Static Power Comparison Table of Novel Full Adder and Conventional Full Adder at 45nm With1.1v

Parameter	Full Adder With Novel PMOS & NMOS	Conventional CMOS full adder
Static power when all inputs are at 0.6v	44.6pw	30.97pw
Static power when all inputs are at 0v	52.18pw	28.76pw

Table 6 : Static Power Comparison Table of Novel Full Adder, And Conventional Full Adder At 180nm With1.8v

Parameter	Full Adder With Novel PMOS & NMOS	Conventional CMOS full adder
Static power when all inputs are at 1.8v	30.97pw	69.25pw
Static power when all inputs are at 0v	590pw	97.5pw

V. Conclusions

The performance of many large circuits are strongly dependent on the performance of the full adder circuits that have been used. An attempt has been made to design 84T novel full adder with low power consumption. In this paper we have simulated conventional full adder and Novel full adder and calculated average power. As mentioned earlier as the technology advances apart of dynamic power, there will be a equal part of leakage power, therefore a Novel full adder will suitable for low power design.

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