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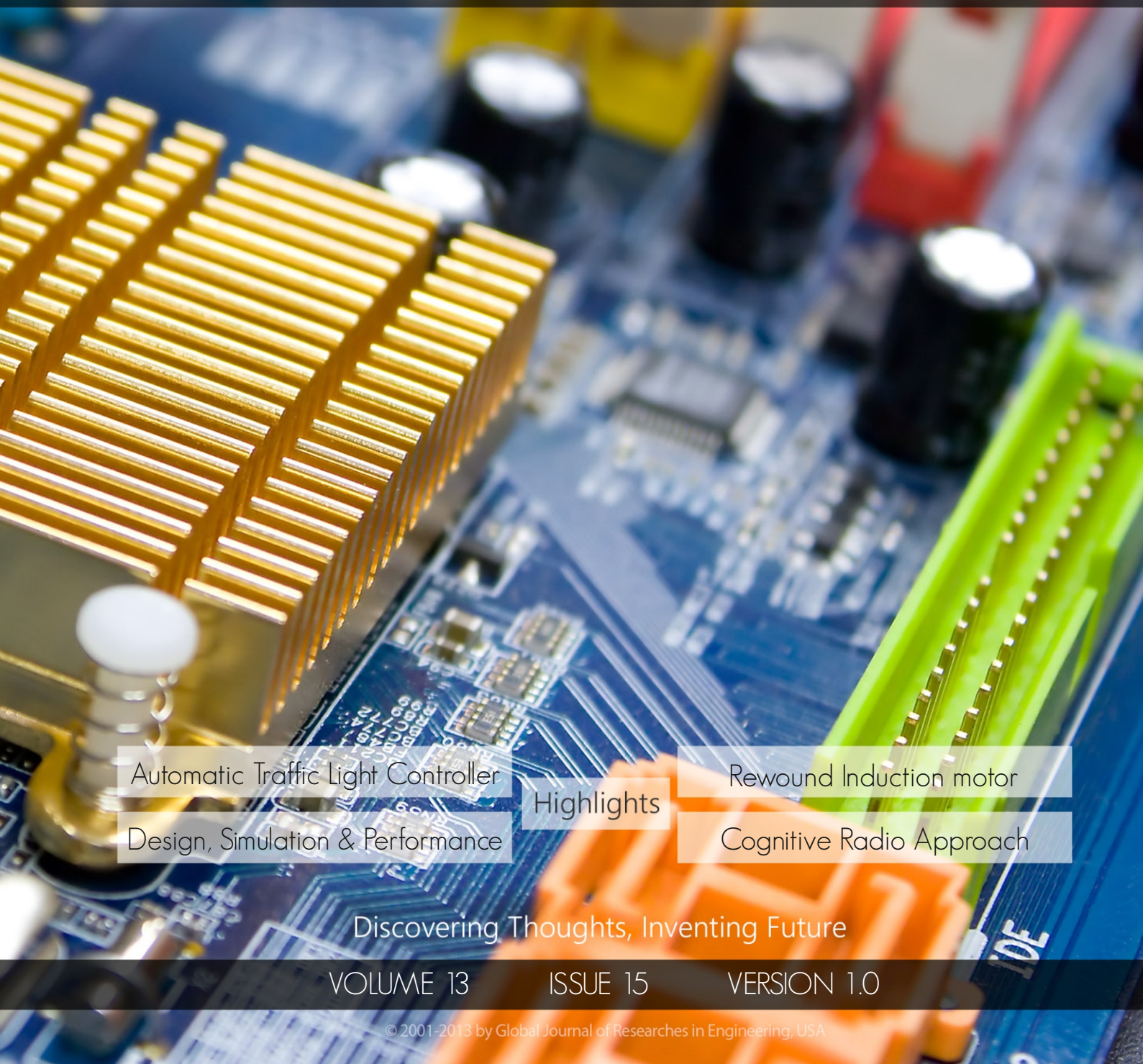

Automatic Traffic Light Controller
Design, Simulation & Performance

Highlights

Rewound Induction motor
Cognitive Radio Approach

Discovering Thoughts, Inventing Future

VOLUME 13 ISSUE 15 VERSION 1.0

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Designing of Automatic Traffic Light Controller in Roads and Railways Transport System for Controlling Purpose

By Mr. Prashant Kumar, "FARSE"
Amity University, India

Abstract- With the Traffic Light only the chances of roadside accident and human error based Railway Accidents are reduced to minimal amount these days. With the increasing number of roads and trains, the requirement for accuracy based controlling the traffic lights is increasing day by day in future generation. This paper is an attempt to introduce the reader into the world of Digital Electronics and Hardware Description Language based device. Traffic Light Controller plays a very important role in the Roads and Railways based Automatic Controlling System. The designing of Automatic Traffic Light Controller System for Roads and Railways Purpose through control the traffic of city, maintain the tracks andpublic places. The Automatic Traffic Light Controller in Railway System placed at Four Line Central Based Server which control the Railway Traffic through the Automatic Designing based System. This Traffic Light Controller plays the operation in Roads Service through controlling the Roads in the concept of Digital Electronics. This project is based on the construction and working of this Automatic Traffic Light Controller Chip Based System. This paper gives the Virtual Operation as Simulation and Integrated Circuit Performance which has to be designed in Hardware Description Language by using the concept of Digital Electronics.

Keywords: introduction, controlling system in roads, controlling system in railways, concept of digital electronics, using software in this controlling system, designing-programming and simulation, result and conclusion.

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The Automatic Traffic Light Controller in Railway System placed at Four Line Central Based Server which control the Railway Traffic through the Automatic Designing based System. This Traffic Light Controller plays the operation in Roads Service through controlling the Roads in the concept of Digital Electronics. This project is based on the construction and working of this Automatic Traffic Light Controller Chip Based System. This paper gives the Virtual Operation as Simulation and Integrated Circuit Performance which has to be designed in Hardware Description Language by using the concept of Digital Electronics.

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I. Introduction

Traffic Light plays the most important role in our life while dealing with huge traffic and increasing population. It also plays to develop the Automatic Controller System which enable for Error Free Controlling System. This traffic light controller enables for designing as Digital Designing Concepts by programming in VHDL and Verilog HDL as Hardware Description Language. This paper gives me the new way for developing the Automatic System Based Traffic Light Controller and marketing as launching this product in India. This Controller System enable for Roads and Railways Project with the Automatic Controller System. The Traffic Light Controller based on this designing language is enabling for producing the valuable information as location and other things in Railways System. This Controller can be used at Parking System, Vehicle Controlling Purpose, Educational Projects and other Public Places.

Controlling System in Roads- This controlling system is to design the Traffic Light Controller with the concepts of Four Directions Roads System. It controls the main city points as North, South, East and West Direction. This is the Automatic System Based Traffic Light Controller System.

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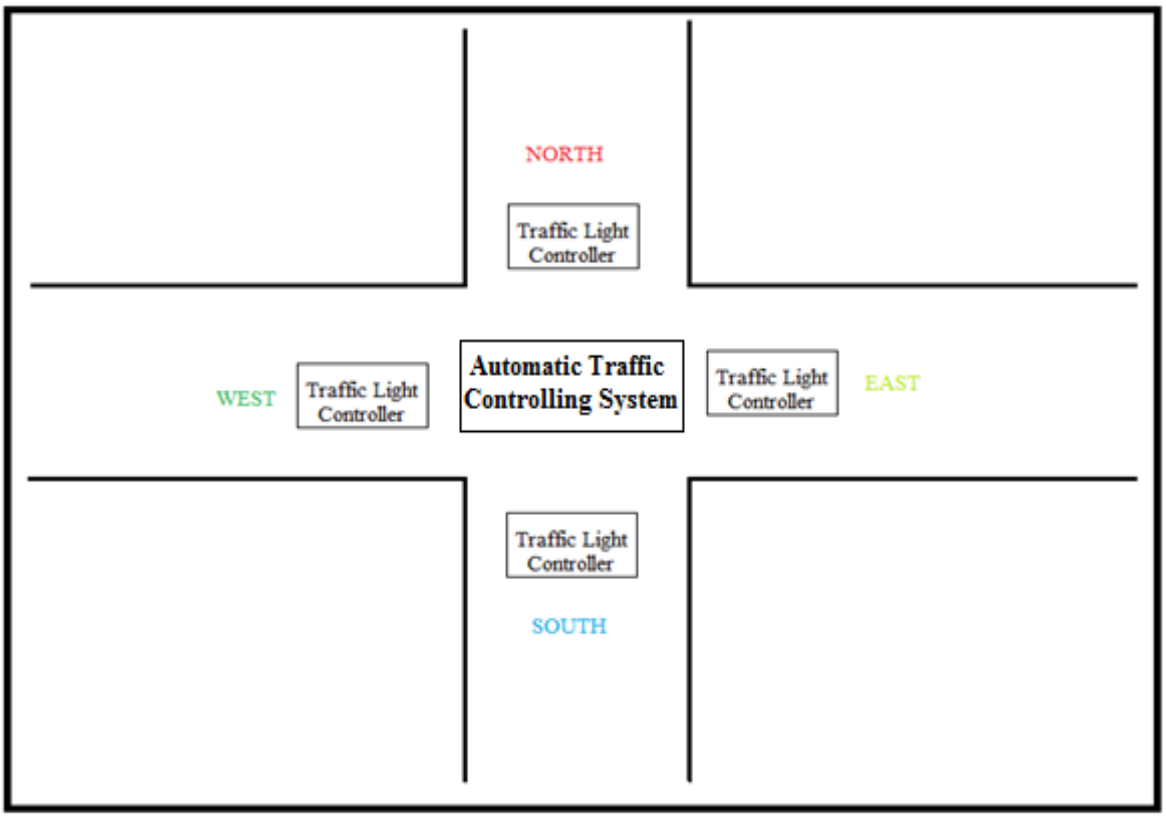
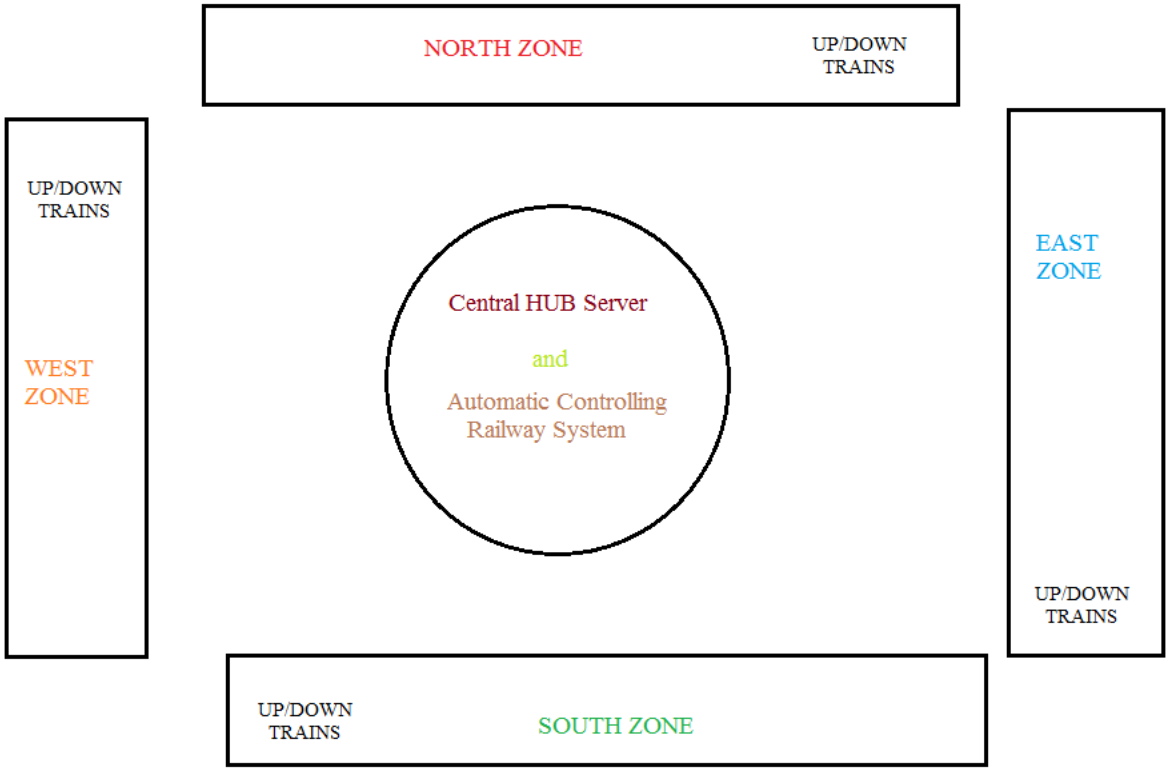


Traffic Light Controller in Roads System

This is the Digital System Based Traffic Light Controller which comes about an idea from the Digital electronics. The implementation of idea is based on VHDL and Verilog HDL as Hardware Description Language in XLINIX 9.2, DSCH 3.1, Microwind 3.1 and Altera Quartus II Software.

Controlling System in Railways-The maintaining of Traffic Light Controller System in Railways is based on the Central HUB Server which controls the four zonal direction of Railways. There are certain problems and for solving the problem of hazard and human accidental case in railways, I have to design the Restart and Clock Control System which comes from the concept of Sequential Circuit. This Restart and Clock System creates the following action when hazard and human accidental problem has started and then this system will manually restart that zone direction of Traffic Light Controller System.

The Indian Railways System is the busy and hazards creating system. This hazard shows the accidents and human errors which automatically fail the concept of Moore Machine as present state in Automatic Traffic Light Controller System. The main purpose for designing this Automatic Traffic Light Controller System is too developed in this innovative way to handle this situation at the time of Hazard Problems. The Four Direction Zone Railway System is based on the UP and DOWN Trains and Railway Lines as per Railway System in India and other countries. The Clock System is based on the Running Train Location and Operating this Automatic Traffic Light Controller System.



Traffic Light Controller in Railway System

Concepts of Digital Electronics-This AutomaticTraffic Light Controller System is based on the concept of Digital Electronics which shows the Roads Traffic Light System as Combinational Circuit. This system has arisen the concept of Four Direction Roads and the controlling of Roads in a Sequence Manner. This system is based on the designing of this four direction based Traffic Light Controller.

It also shows the Railway Traffic Light Controller System as Sequential Circuit which can be restart as Hazard and Accidental Problems. The main purpose for designing this circuit is that the system has arisen on four direction zone which shows if any hazard problem created on any direction as based on the designing of Traffic Light Controller. This System can restart that zone due to Hazard Problems as maintaining the Railway System in Automatic Controlling Based Traffic Light Controller System.

- *Abbreviations used in Truth Table*

A, B, C: CLOCK SWITCHES USED TO GENERATE INPUT PULSES.
NG: NORTH GREEN. SS
NY: NORTH YELLOW.
NR: NORTH RED.
WG: WEST GREEN.
WY: WEST YELLOW.
WR: WEST RED.
SG: SOUTH GREEN.
SY: SOUTH YELLOW.
SR: SOUTH RED.
EG: EAST GREEN.
EY: EAST YELLOW.
ER: EAST RED.

A	B	C	NG	NY	NR	WG	WY	WR	SG	SY	SR	EG	EY	ER
O	O	O	I	O	O	O	O	I	O	O	I	O	O	I
O	O	I	O	I	O	O	I	O	O	O	I	O	O	I
O	I	O	O	O	I	I	O	O	O	O	I	O	O	I
O	I	I	O	O	I	O	I	O	O	I	O	O	O	I
I	O	O	O	O	I	O	O	I	I	O	O	O	O	I
I	O	I	O	O	I	O	O	I	O	I	O	O	I	O
I	I	O	O	O	I	O	O	I	O	O	I	I	O	O
I	I	I	O	I	O	O	O	I	O	O	I	O	I	O

Automatic Traffic Light Controlling in Roads System

A	B	C	NG	NY	NR	WG	WY	WR	SG	SY	SR	EG	EY	ER
O	O	O	O	I	O	O	I	O	O	I	O	O	I	O
O	O	I	I	O	O	I	O	O	I	O	O	I	O	O
O	I	O	O	I	O	O	I	O	O	I	O	O	I	O
O	I	I	O	O	I	O	O	I	O	O	I	O	O	I
I	O	O	O	I	O	O	I	O	O	I	O	O	I	O
I	O	I	I	O	O	I	O	O	I	O	O	I	O	O
I	I	O	O	I	O	O	I	O	O	I	O	O	I	O
I	I	I	O	O	I	O	O	I	O	O	I	O	O	I

Automatic Traffic Light Controlling in Railways System

When Rst = '1' in West Zone Direction

A	B	C	NG	NY	NR	WG	WY	WR	SG	SY	SR	EG	EY	ER
O	O	O	O	I	O	O	O	I	O	I	O	O	I	O
O	O	I	I	O	O	O	O	I	I	O	O	I	O	O
O	I	O	O	I	O	O	O	I	O	I	O	O	I	O
O	I	I	O	O	I	O	O	I	O	O	I	O	O	I
I	O	O	O	I	O	O	O	I	O	I	O	O	I	O
I	O	I	I	O	O	O	O	I	I	O	O	I	O	O
I	I	O	O	I	O	O	O	I	O	I	O	O	I	O
I	I	I	O	O	I	O	O	I	O	O	I	O	O	I

Controlling the Hazard Conditions as West Zone in Railways System

Similarly as per Measuring Scale using this concepts in Hazards and Human Accident Condition.
When Rst= '1' in All Zone Direction

A	B	C	NG	NY	NR	WG	WY	WR	SG	SY	SR	EG	EY	ER
O	O	O	O	O	I	O	O	I	O	O	I	O	O	I
O	O	I	O	O	I	O	O	I	O	O	I	O	O	I
O	I	O	O	O	I	O	O	I	O	O	I	O	O	I
O	I	I	O	O	I	O	O	I	O	O	I	O	O	I
I	O	O	O	O	I	O	O	I	O	O	I	O	O	I
I	O	I	O	O	I	O	O	I	O	O	I	O	O	I
I	I	O	O	O	I	O	O	I	O	O	I	O	O	I
I	I	I	O	O	I	O	O	I	O	O	I	O	O	I

Controlling the Hazard Conditions as All Zones in Railways System

Using Software in this Controlling System- The software using in this designing of Controlling System are DSCH 3.1, XLINIX 9.2, Microwind 3.1 and Altera Quartus II Software which plays the important role as

DSCH 3.1 and XLINIX 9.2 for this designing of Automatic Traffic Light Controlling System enables:

XILLINX ISE-Xlinix ISE is a complete ECAD (Electronic computer-aided design) application. It has the added and provided value of being produced by the world's largest supplier of programmable logic devices and being free. This application also enable the helps you design, test and debugging integrated circuits.

If you ever tried to design and implement any kind of electronic circuits, digital concepts, connecting cables, LED's and chips, as soon as we know that pretty soon all you end up with a big and confusing pile of small colour cables. There are some applications which available that we shall help to keep things in perspective and respective manner for transposing the logic and circuit to your screen. This will benefit in a lot of ways as soon that we can forget about implementing the bread boards malfunctions or looking for hours through burned (forgotten) chip. Xilinx ISE simply takes this idea to the next level (several levels above in VLSI Design). We will have access to hundreds of industrial standard chips, from the standard AND or NOT gates that it can get all the way to the more complex ones (including multiplexers, counters etc.). If we do not find that what you need you will be able to design it and use it just as another chip from the library.

After the Design and Logic Circuit Phase, we can test our design by changing inputs and checking the results in this software. This will take few time in each circuit has to be completely compiled and completed before the test can be done. As we might have already concluded, this is not program for the beginner. The user interface has although clean and full of nice buttons but cannot hide the complexity of the underlying process. We shall most probably need the user manual of this software. This is very advanced program in HDL Language to be used by engineers at production and industrial level in VLSI Design by designing the chips in IC Fabrication.

One word of advice that however, we save our work frequently. Xilinx will crash repeatedly when compiling our work in HDL Language. It will not recognize our save files and it will not be able to read our data. If we try to save everything in a simple folder in the root of our disk, no characters besides letters, no special words and no spaces as soon as possible. I have always managed to get my work back but I surely would not like to have to work with this application on a daily basis.

- Advantages

1. Free
2. Very complete libraries of components
3. Multiple testing, designing and debug possibilities.
4. Lots of aid tools.

- Disadvantages

1. Very unstable

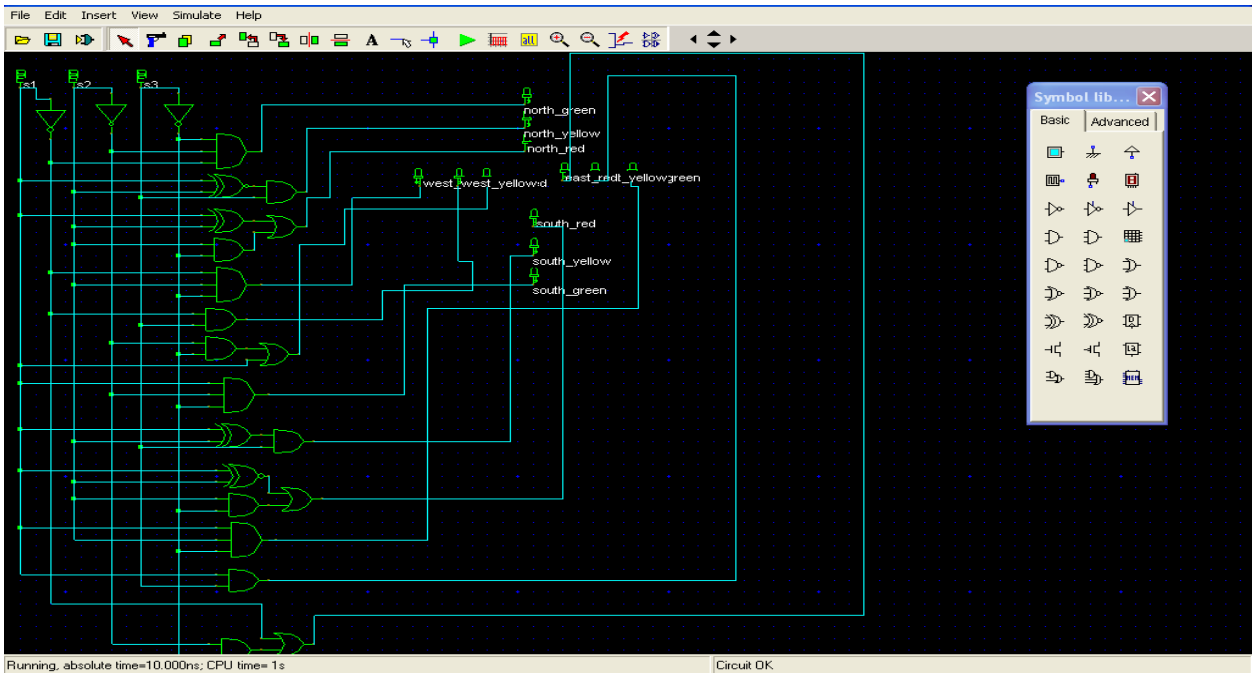
DSCH 3.1 C-The DSCH program is a logic editor, digital circuit design and simulator. DSCH is always used to validate the architecture of the logic circuit and digital design before the microelectronics design is started. DSCH also provides a user-friendly environment for hierarchical logic and digital design, fast simulation with delay and logic analysis, which allows the design and compilation of complex logic structures. DSCH also features the symbols of logic gates, models and assembly support for 8051 and other Micro Controllers. Designers can create the logic circuits for interfacing with these controllers and verify software programs using DSCH.

- Highlights

1. User-friendly environment for rapid design of logic circuits.
2. Supports hierarchical logic design.
3. Handles both conventional pattern-based logic simulation and intuitive on screen mouse-driven simulation
4. Built-in extractor which generates a SPICE netlist from the schematic diagram (Compatible with PSPICE™ and WinSpice™).
5. Current and power consumption analysis.
6. Generates a VERILOG description of the schematic for layout conversion.
7. Immediate access to symbol properties (Delay, Fan Out).
8. Model and assembly support for 8051 and PIC 16F84 microcontrollers.
9. Sub-micron, deep-submicron, nanoscale technology support.

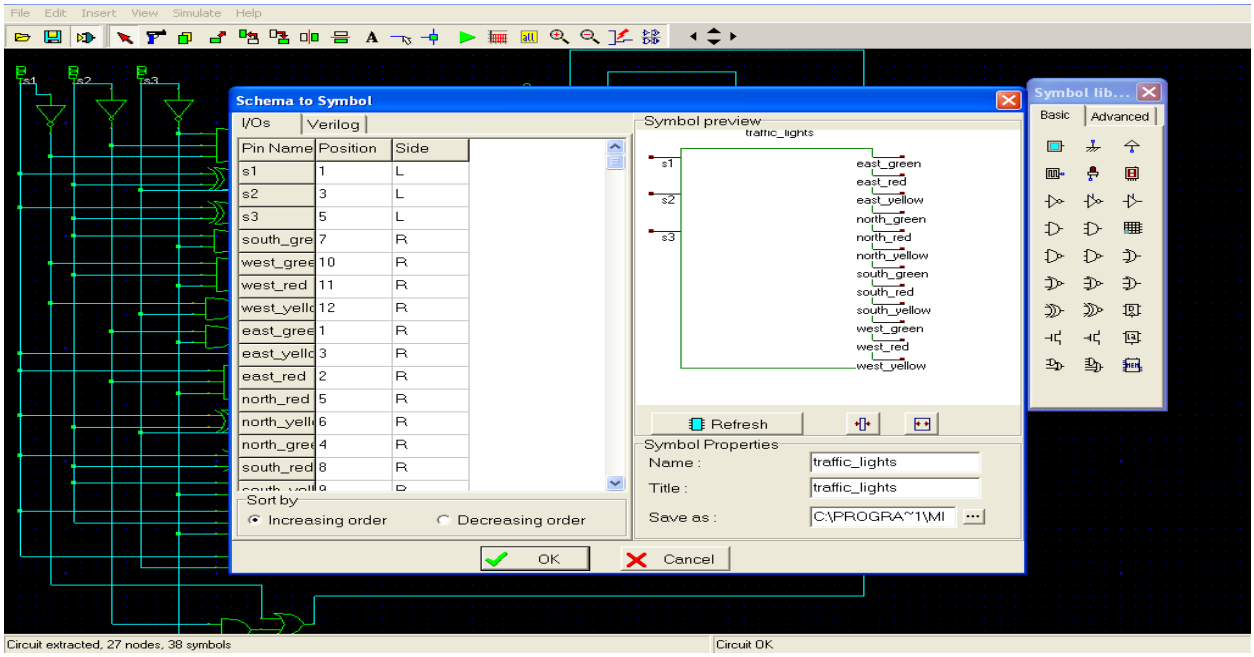
Programming-Designing and Simulation-The various steps done in the software while designing the traffic light controller chip is shown step by step using snapshots of the entire process with outputs at every level as working in DSCH 3.1 Software:

1. Creation of the schematic circuit using the truth table for traffic lights operation.
2. Creating chip from the schematic circuit of the traffic light controller.

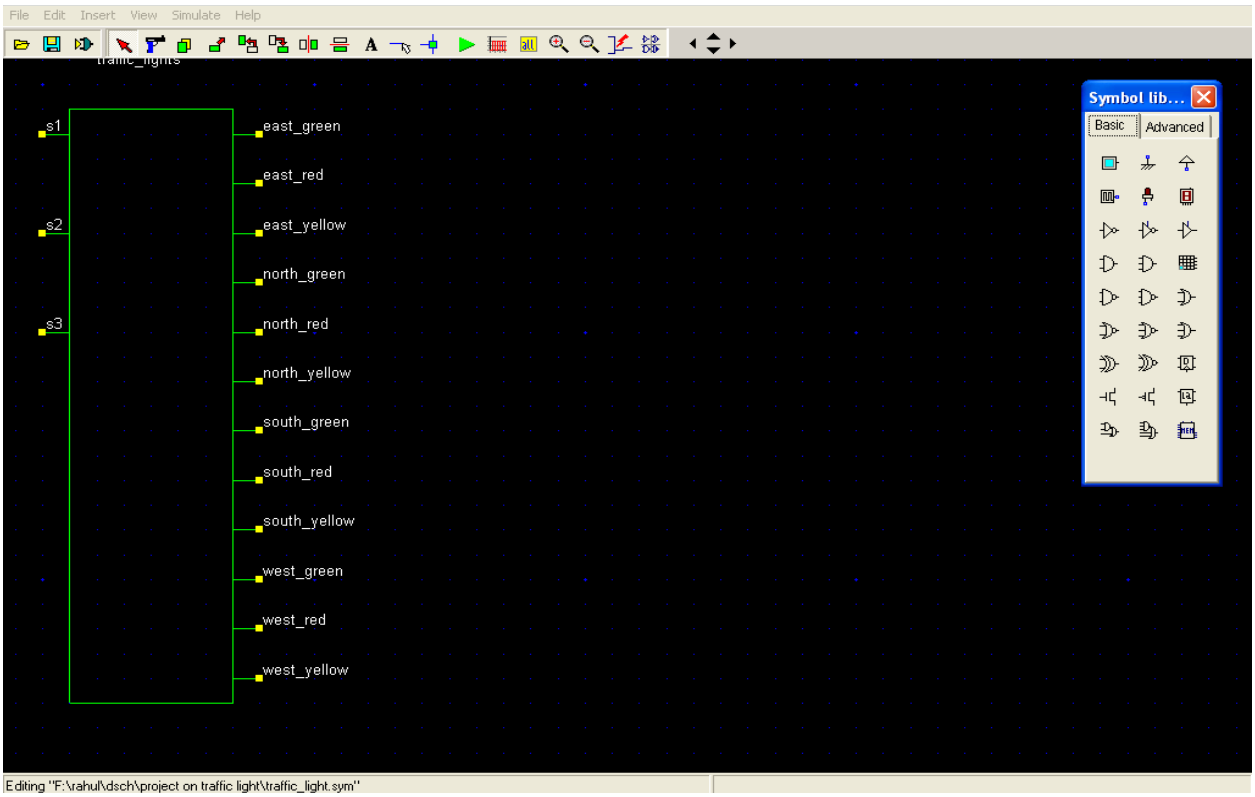


Observation of output after connecting the chip with the output LEDs and input clocks

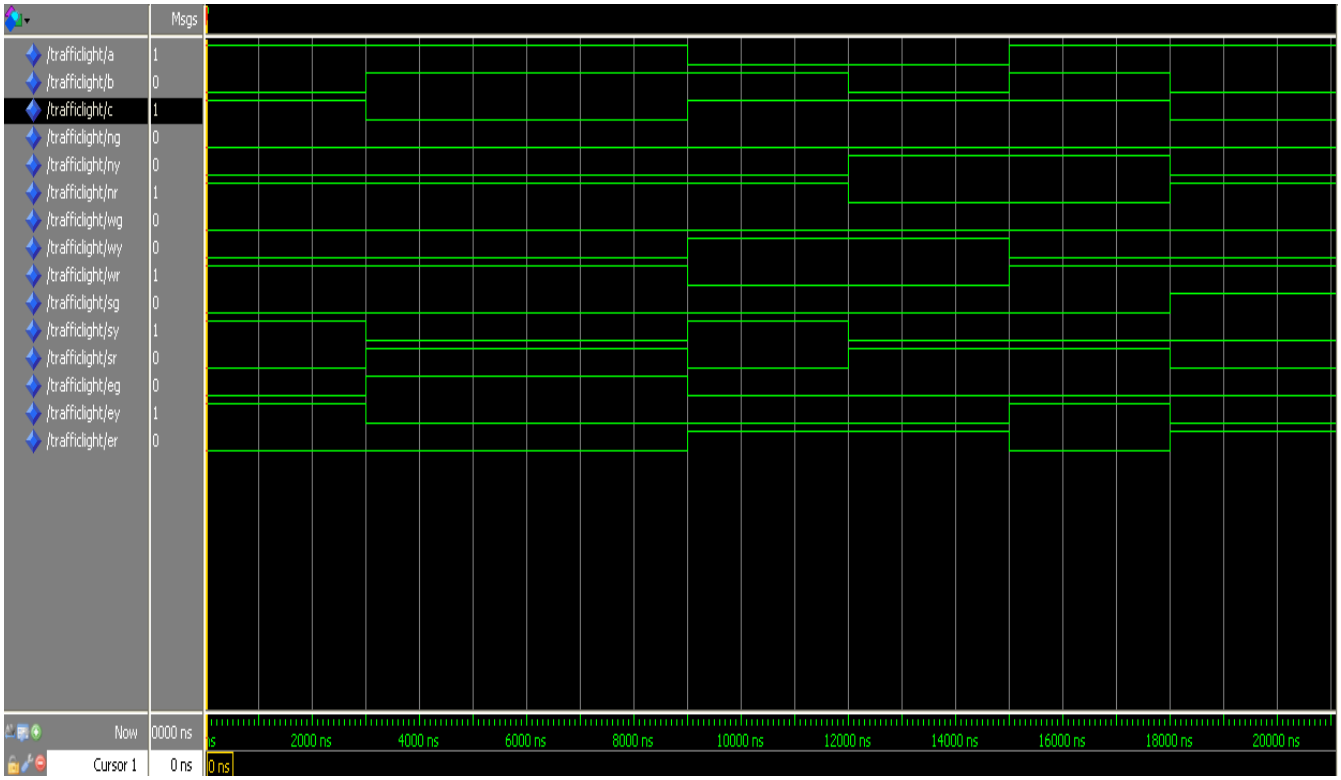
Circuit Designing Using DSCH 3.1 Software



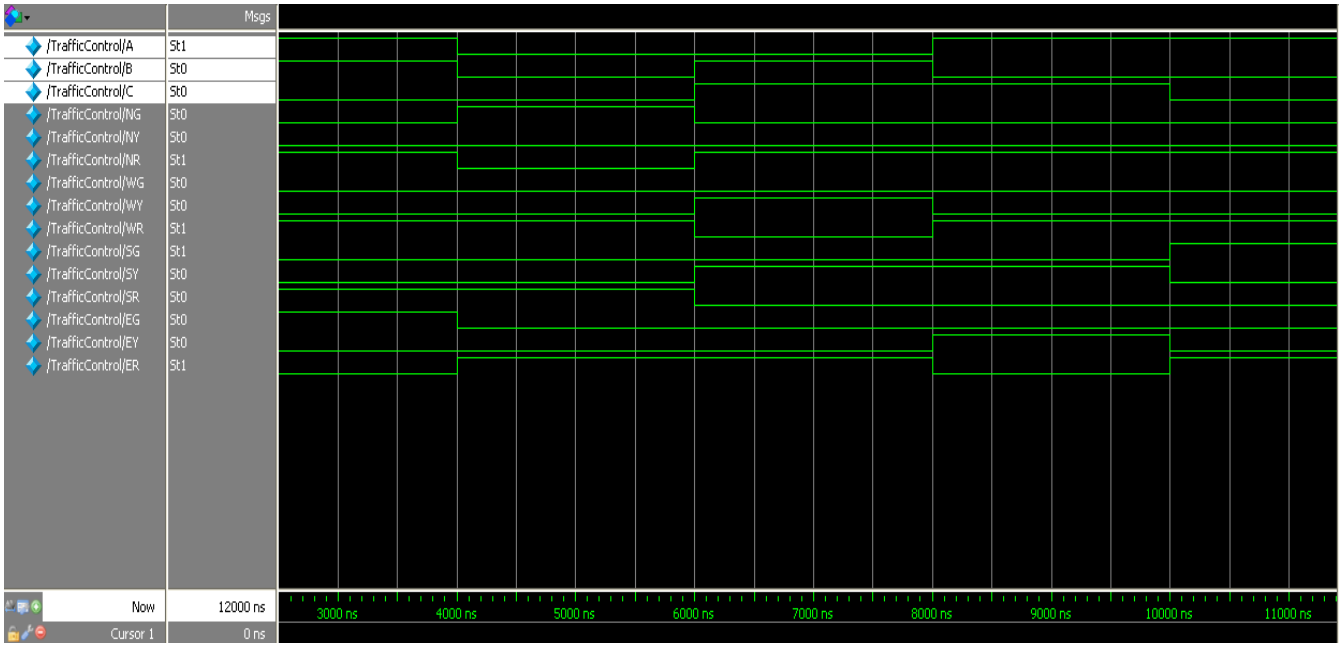
Simulation in DSCH 3.1 Software



Formation of Automatic Traffic Light Controller



VHDL Design Simulation



VERILOG HDL Design Simulation

II. Results and Conclusion

From here, I have now discussed the all points related to this Automatic Traffic Light Controller. This research and implementation of idea is based on the new device which provides flexibility and high economy for traffic solutions in our daily life. This Automatic Traffic Light Controller implements the true output state by applying the present Clock State. This controller can achieve the following aspects through automatic controlling purpose which become railway tracks and roads traffic faster and to minimize the hazard problems in our daily life.

This Automatic Traffic Light Controller is based on the State Designing and concept of Moore Machine which depends on the output and present state of machine. The design and waveform expression shows the proved explanation of Automatic Traffic Light Controller. This controller can be used in various applications like Air Traffic Control, Metro Railways System, Special Trains System, Railway Tracks and Roads System. This Automatic Traffic Light Controller is based on the Red, Yellow and Green Light as the concept of Moore Machine for creation of Controlling Device. This Traffic Light Controlling System becomes life more easily for controlling the things as automatic system with 100% accuracy purpose for designing and development of Automatic Enabling Controlling Device.

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Reducing the Vulnerability of Digital Protective Relays to Intentional Remote Destructive Impacts

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Abstract- A new way for protecting digital protective relays from cyber attacks and intentional destructive electromagnetic impacts is describe in the article.

Keywords: *digital protective relays, intentional destructive electromagnetic impacts, cyber security.*

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I. Introduction

The modern trend of the replacement of electromechanical protective relays by digital protective relays (DPR) has exposed a serious problem, which was not known before in the field of relay protection. This problem is the possibility of an intentional remote destructive impact (IRDI) on the relay protection in order to disable it or force it to perform functions that are not related to the current mode of operation of the electric equipment being protected. DPR is the most critical link in the structure of modern power supply systems [1] because, on the one hand it is the most susceptible to IRDI, while on the other hand it is directly related to power circuit breakers, which influence the configuration of the power system. This is why IRDI in the form of cyber attacks and intentional destructive electromagnetic impacts (IDEI) [3] are targeted at DPR [2]. Special research conducted by B5 CIGRE and presented in its report confirmed the relevance of the problem and reached the conclusion that the expansion of the application of the most advanced standard IEC 61850 with its GOOSE-messages as well as modern Ethernet technologies in relay protection result in increasing of its susceptibility to IRDI [4]. The Smart Grid [5] technologies are equally dangerous in this regard.

II. The New Way for Highly Efficient Compound Protection of DPR

The recent appreciation of the problem of DPR's cyber safety has resulted in intensification of multiple investigations related mainly to sophistication of computer communication protocols designed for relay protection and improvement of their cryptographic security. Until recently, different specialists have concentrated all their efforts into just this area. As for IDEI, unfortunately this problem has not been seriously addressed yet. At the same time, 17 years ago when the DPR's problems were just emerging, the author offered a general idea of highly efficient compound protection of DPR from cyber attacks and IDEI by means of hardware facilities instead of software tools. The suggested protection device implements a principle of by-passing the sensitive DPR's terminals by means of responsive electromechanical reed-switches [6]. The idea of implementation of responsive electromechanical reed-switches was further developed in more details [7, 8].

As mentioned before, the task of increasing the reliability of relay protection cannot be fulfilled by combining DPR's functions with those that have nothing to do with relay protection, such as monitoring of the functionality of electric equipment, remote control of circuit breakers, etc. The DPR should be used solely to solve problems of relay protection. Moreover, there are many specific devices in the market that can be used to solve other problems, such as the monitoring of electric equipment. These devices may vary from the simplest relays that control the continuity of the circuit breaker trip coils to sophisticated complex units that ensure online control of gas composition dissolved in the transformer's oil or the level of partial discharges in the insulating material. As for remote control of circuit breakers by means of DPR, this type of application will make it difficult to distinguish between authorized and unauthorized access, this is why use of this type of DPR should be eliminated. Moreover, with separation of the functions, the hardware facilities ensure easier protection from IRDI also of remote control of circuit breakers [9].

III. Device for DPR Protection from IRDI

The general idea behind the suggested hardware-facilitated method of protection of DPR from IRDI is to use an electromechanical reed-switch starting unit (SU) in combination with DPR and connected functionally in series with it as well as an electromechanical action element (RR1 – RR7), which ensures the blocking of the sensitive inputs of DPR and

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disconnection of its output circuit, Fig. 1. The reset of the actuated SU is performed upon the circuit breaker's actuation and backed-up by RESET command at the end of a preliminary set-up time period.

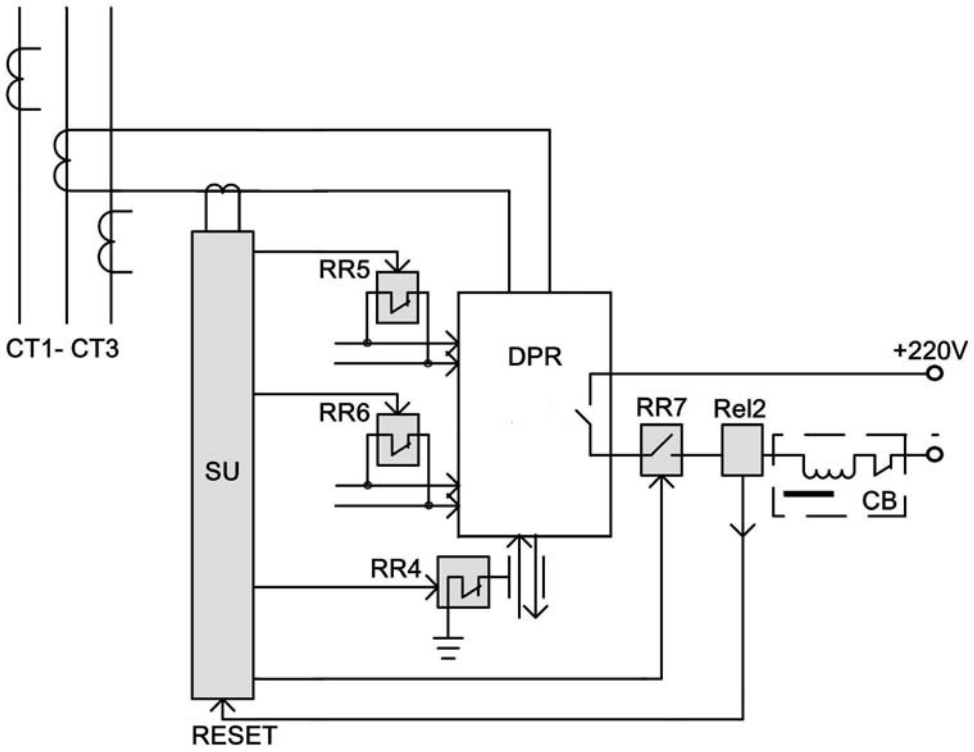

Figure 1 : A structural diagram of DPR protection from IRDI

Without current and/or voltage actuation of this SU, DPR will not be able to influence the operation mode of the power system, even under IRDI. If the SU is actuated and DPR enabled, nothing will interfere with using specific features and wide functional capabilities of DPR. At the same time, unnecessary actuation of the SU itself does not influence the operation of the relay protection and thus there are no specific requirements as to the accuracy of the SU actuation. The only thing that is important is that it should always be actuated before DPR, i.e., its settings should be a little bit lower than required for the controlled parameter. If the SU actuation was unnecessary and DPR was not actuated, the device would automatically reset. The main technical requirements for this device are its high reliability, insensitivity to short electromagnetic impulse (micro- and nanosecond range) and high-frequency interferences, resistance to substantial over-voltages, high level of galvanic insulation from external circuits and high speed of response to actuation (several milliseconds).

This article provides a description of an improved device designed to protect DPR from IRDI, which satisfies the above conditions, Fig. 2.

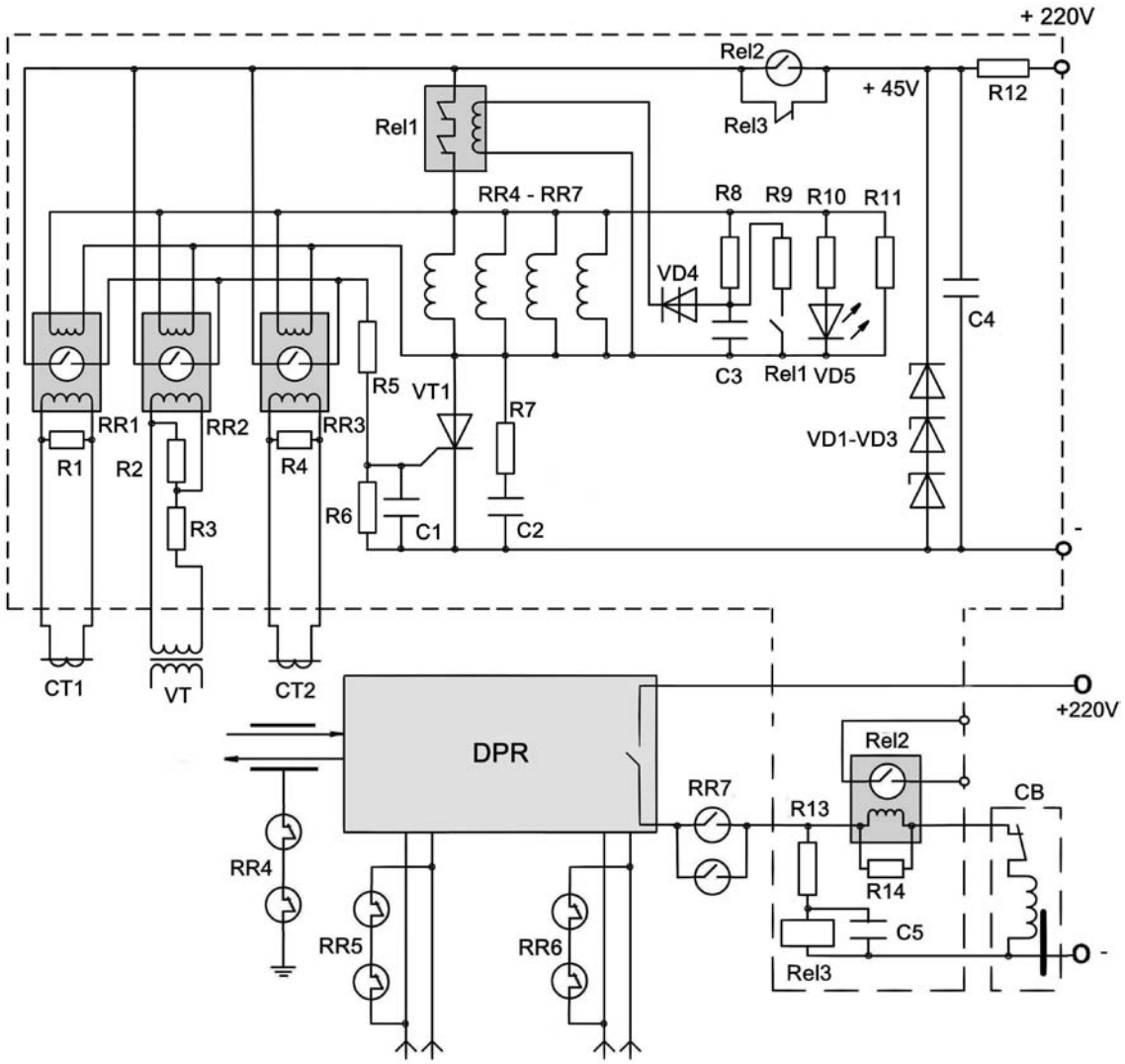

Figure 2 : A diagram of improved device protecting DPR from IRDI

The principle of operation of this device is as follows. In its initial state under the normal operation mode of the protected object, all the input reed-switches (current and voltage sensors, etc.) RR1- RR3, are in the released state. The thyristor VT1 is in the off state; the control coils of the reed-switches RR4-RR7 are not energized. The normally closed contacts RR5 and RR6 short circuit the logical inputs of DPR, the RR4 terminals short circuit the communication channel, while the RR7 terminals open the output circuit of DPR. Under these conditions the DPR is fully blocked both in inputs and in outputs and no IRDI can result in its unnecessary actuation and unauthorized actuation of the CB trip coil. Bypassing both the logical inputs of DPR and the communication channel also increases its operational vitality under the impact of a powerful electromagnetic impulse.

In case of the emergency mode in the protected object at least one of the controlled parameters (current, voltage or power) will drastically change. This change leads to actuation of at least one of the reed-switches RR1- RR3 within one millisecond or less. When actuated, a reed-switch of a corresponding input starts vibrating at a doubled frequency. During the first event of the switching of the reed-switch's terminals, the thyristor VT1 will switch on within several micro-seconds and the control coils of the reed-switches RR4-RR7 will be powered. Actuation (opening) of RR4-RR6 reed switches takes place during 2 – 4 milliseconds, while the switching on of the power terminals of the RR7 reed-switch (Bestact R15U reed-switch type) does not take longer than 5 milliseconds. Thus, the total response time of the unit to an emergency mode does not exceed 6 milliseconds, which is quite acceptable considering the DPR's own actuation time of 30-40 milliseconds. Under this mode of operation of DPR protection device, the DPR will be fully unblocked and returned into its normal mode of operation, retaining all its settings and features.

As can be seen in the diagram (Fig. 1) each of input relays (sensors) is equipped with a second

winding on the reed-switch, which receives power from the constant voltage source upon thyristor's VT1 switching on. Due to the additional magnetic field created by this winding, the reed-switch of the actuated relay stops vibrating and enters a steady on state.

After the DPR performs the time delay set-up by its feature, its internal output relay will energize trip coil of the CB. Current flowing in the circuit of the CB trip coil results in actuation of the reed-switch relay Rel2 with a powerful Bestact R15U reed-switch and switching on of its terminals connected in parallel to the normally closed terminals of Rel3. Rel3 is actuated with a small time delay (about 10-20 milliseconds). This time delay is necessary in order for Rel2 terminal to switch on before Rel3 terminal switch off.

At the end of actuation cycle of the CB circuit breaker, its interlock will switch off and the circuit of the trip coil will be interrupted. At the same time Rel2 is released and its contact interrupts the anode circuit of the thyristor VT1, which is then immediately switched off, cutting off current from the control coils of RR4-RR7 relays and addition DC coils of RR1-RR3 relays. The device is totally returned to its initial state and is ready for a new cycle of operation.

If actuation of the device was unnecessary and DPR did not generate a command to disconnect the circuit breaker, the supply circuit of the thyristor VT1 will be interrupted for a short time by a normally closed contact of Rel1 relay upon the charging of C3 capacitor through resistor R8 and switch on of VD4 dynistor diode. The capacity of this capacitor and resistance of the resistor ensure a time delay of several seconds, which exceeds the maximum possible time necessary to fulfill the full cycle of DPR operation in order not to interfere with its operation should it be required. Actuation of Rel1 relay is temporary, since immediately upon its actuation and the opening of the normally closed contacts in the thyristor's circuit, its normally open terminal will switch on and discharge the C3 capacitor through a low-Ohm R9 resistor, ensuring its full discharge and return into initial state. At the same time the VD4 dynistor diode will close and current on the Rel1 relay's coil will be cut off. This is how a forced reset of the device to its initial state happens, if its actuation is unnecessary.

The R11 resistor is needed to increase the current rate flowing through the power thyristor VT1 and its reliable maintenance in a conducting state. The LED VD4 serves as an indicator of the device's condition.

In order to increase the reliability of the device and its resistance to IDEI, only a few solid-state elements are used. They were selected with very big reserves for the device's maximal values in marginal current and voltage rates that are not used in usual industrial applications. For example, the VT1 thyristor with its actual operational voltage of 45 V was selected for maximum voltage rate of 1200 V; with its actual operational current rate of fractions of Ampere, it can work under current of tens of Ampere and conduct short-term impulses of hundreds of Ampere. The Zener diodes VD1-VD3, as well as the VD4 dynistor diode, are also selected with very large power reserves. The auxiliary relays Rel1 and Rel3 are selected as sealed with high power contacts. The general recommendations for selection of hardware components of protection device and even some specific types of recommended components are listed in [8].

IV. Resume

The described solution is designed to prove the technical possibility for implementing digital relays protection from intentional remote destructive impact by means of hardware components rather than software tools. It can serve as a starting point for detailed developments of a device suitable for industrial production. Further efforts should be aimed at developing structural designs of input reed-switch relays (current and voltage sensors) with adjustable threshold of actuation. The experience of development of such devices is mentioned in [10].

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Renewable Energy: An Ideal Solution of Energy Crisis and Economic Development in Bangladesh

By Abu Md. Abdul Wadud, Md. Tousif Zaman, Fazlay Rabbee & Md. Rajibur Rahman

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Abstract- Present world is moving fast towards development of civilization. Industries, factories, power plants, various government institutions, scientific institutions, private organizations are growing up on the basis of available natural energy sources. However, these sources are limited and expensive. CO2, CFC and other harmful gases are being produced through the utilization of these sources. Air is being polluted through these gases. So renewable energy will be the best solution. Developed countries are searching for newly alternative energy sources to minimize the pressure on natural sources like gas, oil, coal etc. Developing countries like Bangladesh are also trying to utilize different renewable energy sources to fulfill their growing demand. Bangladesh is a small country with a vast population. People have been suffering from insufficient electricity for many years. To meet the energy crisis Bangladesh has been experienced to renewable sources like biogas, bio-fuel, solar energy, wind energy, tidal energy, geothermal power, hydro power etc. In this paper we have tried to analyze about renewable sources of the country. Here we have identified the utilization of renewable sources and their benefits. This paper also belongs to subject that how far renewable energy can be treated as an ideal solution of economic development.

Keywords: bangladesh, energy crisis, electricity, economic development, renewable energy, biomass, solar energy.

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Abu Md. Abdul Wadud [α], Md. Tousif Zaman [σ], Fazlay Rabbee [ρ] & Md. Rajibur Rahman [ω]

Abstract- Present world is moving fast towards development of civilization. Industries, factories, power plants, various government institutions, scientific institutions, private organizations are growing up on the basis of available natural energy sources. However, these sources are limited and expensive. CO_2, CFC and other harmful gases are being produced through the utilization of these sources. Air is being polluted through these gases. So renewable energy will be the best solution. Developed countries are searching for newly alternative energy sources to minimize the pressure on natural sources like gas, oil, coal etc. Developing countries like Bangladesh are also trying to utilize different renewable energy sources to fulfill their growing demand. Bangladesh is a small country with a vast population. People have been suffering from insufficient electricity for many years. To meet the energy crisis Bangladesh has been experienced to renewable sources like biogas, bio-fuel, solar energy, wind energy, tidal energy, geothermal power, hydro power etc. In this paper we have tried to analyze about renewable sources of the country. Here we have identified the utilization of renewable sources and their benefits. This paper also belongs to subject that how far renewable energy can be treated as an ideal solution of economic development.

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I. Introduction

Bangladesh is situated between 20^0 34' and $26^0$38' North Latitude and $88^0$01' and $92^0$41' East Longitude with a total landmass of 1,47,570 square kilometers (56,977 Sq. miles). India on the West, North and Northeast, Myanmar on the Southeast and the Bay of Bengal on the South surround Bangladesh. Bangladesh has a tropical monsoon climate with heavy summer rain and high summer temperatures. Main seasons prevail in Bangladesh are summer (March-May), Rainy Season (June-September) and winter (December-February). 95% of the total rainfall, which averages about 1733 millimeters, occurs during these periods [1]. The temperatures range from an average of about 68^0F(18^0C) in January to about 86^0F (30^0C) in April [1]. Bangladesh is an agro-based country. Her economy depends on agriculture. Production needs sufficient electricity. But failure of power creates a bad impression on production. About 70% people of the rural area are deprived from electricity [2]. They depend on conventional energy sources-near 70% energy comes from these sources [3]. Electricity generation rate is less than the huge demand. To meet the demand Government of Bangladesh is using natural sources like gas, oil, coal etc. Bangladesh has huge reserve of gas, limited reserve of oil and coal. According to the Gas Initially in Place (GIIP) data, Bangladesh has 21.3 tcf of proven gas (P1; proved or with probably of 90 percent of greater or equal volume). Out of which 15.4 tcf is recoverable and 7.7 tcf of gas has already been produced [4]. The total coal reserve is estimated to be 2.9 billion metric tons [4]. Bangladesh imports 1.2 million tons of crude and 2.5 million tons of refined oil each year. The source of gas (24%) may be depleted nearby 2020 [5]. Huge amount of imported oil costs a lot of foreign money. To take coal through digging from soil is very much expensive and this process may be harmful for climate. Therefore, energy crisis becomes a major concern now. About 53% of total electricity comes from public sector and 47% of the rest electricity comes from private sector [6]. Due to the graphica location Bangladesh has potentiality of renewable energy. Several government organizations such as Bangladesh Power Development Board (BPDB), Dhaka Electric Supply Authority (DESA), Rural Electrification Board (REB), Local Government Engineering Department (LGED), non government organizations and private companies such as Grameen Shakti (GS), Bangladesh Center for Advanced Studies (BRAC), Centre for Mass Education in Science (CMES) etc are involved in the renewable sector of the country. Renewable energy can be a good solution of energy crisis, which has less impact on climate. Different forms of renewable energy source can provide sufficient power to urban and remote areas. It can also reduce the pressure on natural sources and can help to save foreign currency. Previous works have done to recognize the

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renewable energy sources of Bangladesh and some difficulties to establish project in rural areas. This paper reviews present condition of energy crisis and possible application of renewable sources in Bangladesh. This paper also indicates the beneficial aspects of renewable energy for the people of Bangladesh.

II. Present Power Scenerio in Bangladesh

Demand of power is increasing day by day. Due to high demand maximum generation of 4130 MW in 2007, 4036.7 MW in 2008, 4296 MW in 2009, 4698.5 MW in 2010, 5174 MW in 2011, 6350 MW in 2012, 6675 MW in 2013 could not remove the power crisis [6]. Vast rural areas are being affected by load shedding. Due to power failure irrigation, production of products, water supply and daily activities are being disturbed. To solve the crisis government has planned to install power plants with capacity of 14720 MW by the year 2016 [6]. But there is a huge gap between generation and demand. Huge amount of power loss is occurred through transmission. Most of the power plants are old. Generation rate of these power plants is lower than newer plants. Most of the power plants are gas and oil based. Rental power plants are set up to meet short-term and emergency requirements of the country, which seems to be costly. Here figure-1 [4]. shows energy sector of Bangladesh and in table-1 [4] shows electricity generation through various sources. The given table-2 [7] presents power generation capacity. According to the Master Plan 2010, the forecasted demand would be 19,000 MW in 2021 and 34,000 MW in 2030 [7]. This plan insisted to use domestic coal 30%, imported coal 20 %, natural gas (including LNG) 25%, liquid fuel 5%, nuclear, renewable energy and power import 20% [7].

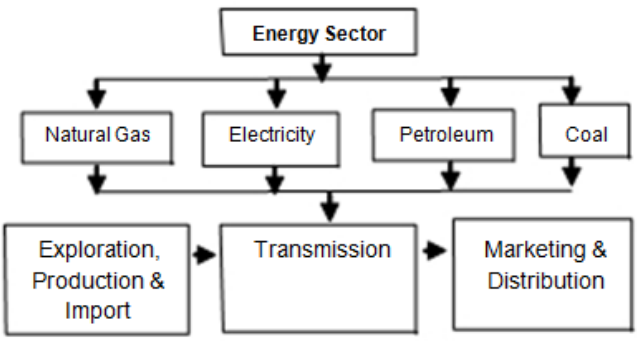

Figure 1 : Energy sector of Bangladesh

Table 1 : Source of energy of electricity generation

Source of Energy	Installed Capacity (MW)	% of Total Installed capacity	Present Capacity	% of Present Capacity	Shutdown Capacity (MW)	Running Capacity (MW)	% of Total Running Capacity
Gas	4847	74.38	4412	74.21	792	3620	74.23
Coal	250	3.84	220	3.70	100	120	2.46
HFO	275	4.22	271	4.56	0	271	5.56
HSD	594.5	9.12	567	9.54	16	551	11.30
FO	170	2.61	95	1.60	60	35	0.72
GT	150	2.30	150	2.52	0	150	3.08
Hydro	230	3.53	230	3.87	100	130	2.67

Table 2 : Present Generation Capacity (Oct, 2011)

Public Sector		
SL.		Generation Capacity (MW)
1	BPDB	2868
2	APSCL	659
3	EGCB	255
	Subtotal	3782 (53%)
Private Sector		
1	IPPs	1231
2	SIPPs (BPDB)	99
3	SIPPs	226
4	15 YR. Rental	168
5	3/5 YR. Rental	1613
	Subtotal	3337 (47%)
	Total	7119

III. Biomass & Biogas

Bangladesh has strong potential for biomass gasification based electricity. More common biomass resources available in the country are rice husk, crop, residue, wood, jute stick, animal waste, municipal waste etc. Exploration of these resources for electricity generation is still at preliminary stage. Biogas is composed of CH_4, CO_2 and other gases, which can be produced by cattle dung, poultry droppings, human excreta and agricultural residues. The digested slurry obtained as a byproduct which acts as a nutrient- rich fertilizer [8]. Bangladesh is in a suitable position for availability of raw materials and the climate conditions for biogas production. About 29.7 billion m^3 of biogas and 10 billion m^3 can be produced from cow dung and human excreta [8]. Different institutions and organizations such as Institute of Fuel Research and Development (IFRD) of Bangladesh Council of Scientific and Industrial Research (BCSIR), universities (BUET, DU, RUET, KUET, JU, BAU etc), LGED, GS etc are working on biogas projects. In 1972, Bangladesh entered the area of biogas technology through Bangladesh Agricultural University (BAU). In 1976, BCSIR first constructed a family-size biogas plant following the design of Khadi and Village Industries Commission, India. In 1986, LGED constructed its first biogas plant at kurigram. In 1992, a biogas plant of 85

cubic meter digester volume was built at dholpur, Dhaka to produce 200 cft biogas from garbage [9]. About 17194 biogas plants were established under a project of IFRD in 2004 [10]. In 2004, Sustainable Rural Energy (SRE) project under LGED has installed 10KW power generation unit, which was based on poultry litter. Excess gas from this unit is being used for cooking purpose at Faridpur Muslim Mission. SRE has also installed two biogas units, one at Kutubdia and the other at Kishoregonj which were based on human excreta. This type of inventions created better health and sanitation facilities as well as energy requirement for cooking and lighting. Demonstration of 3.5KW cow dung based power generation unit at Netrokona district created enthusiasm among the small-scale farmers. Beginning from June 2006, over 10000 biogas plants were constructed under National Domestic Biogas and Manure program (NDBMP) [9]. According to the renewable energy policy, govt. has planned to develop biogas plants to produce at least 500MW power by 2015. Fig-2 shows installation of biogas plants.

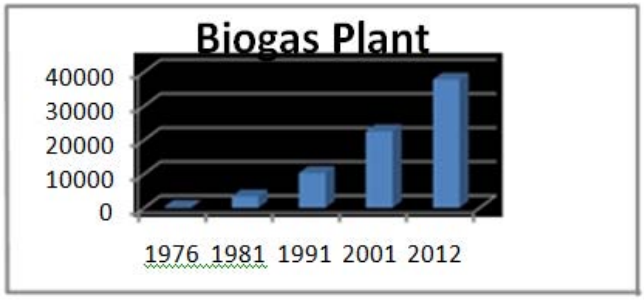

Figure 2 : Biogas plant chart from 1976 to 2012

a) Utilization of Biogas

Significant amount of power can be produced from biomass energy. It can be used in some applications as well as in small household works, cooking, harvesting, lighting, irrigation etc. A fig-2 [11] shows the utilization of biogas in a house.

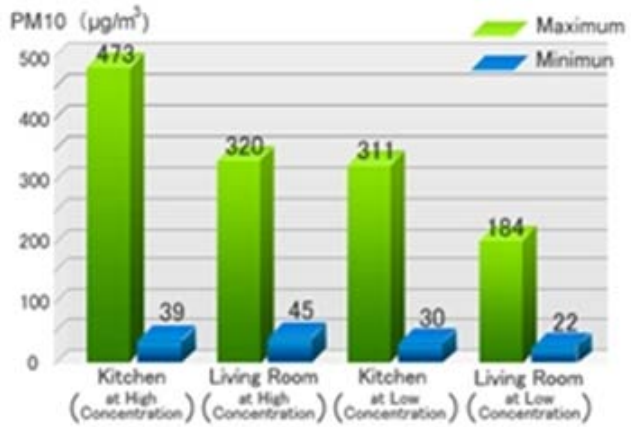

Figure 3 : Utilization of biogas in Bangladesh Houses (24Hr mean)

b) Benefits of biogas energy

People can be benefitted through biomass energy. These benefits are given below:

i. *Financial Benefits*

- revenues from the sales of electricity and heat
- independence from network providers
- use of exhaust heat as thermal and process heat
- sale of high quality fertilizer

ii. *Emission issues*

- methane reduction through elimination of digestible organic mass
- odor nuisance reduction through digesting substrates

iii. *Energy Economic Benefits*

- continuous power generation with basic and peak load capability
- biogas can compensate for fluctuations in wind and solar energy
- reduction of dependence on fossil fuels

iii. *Environmental Aspects*

- production of clean energy from waste
- easier way to spread the fermented residues through improved flow ability
- reduced CO2 emissions of biogas in contrast to fossil fuels
- recycling of previously unused energy resources
- active environmental protection through energy-related recycling
- waste recycling
- production of high-quality, natural fertilizer

iv. *Market Aspects*

- use of overproduction of energy crops relieves food markets
- biogas production opens new production and sales markets

IV. Wind Energy

Recently Bangladesh gets experiences on wind energy. Several locations have already been assessed to evaluate the wind energy potential of the coastal region of the country. Strong wind potential flows during the months of April to September, and a very weak potential during rest of the year. Table-1 shows wind speed [12] in Kuakata. Wind Resource Assessment Station (WRAS) established by BPDB at Moghnama Ghat, Cox Bazar district in December 2003. For the first time in Bangladesh, BPDB implemented a pilot project of 0.90 MW capacity of the

Table 3 : Wind speed in Kuakata

Month	Wind Speed (m/s)
January	5.80
February	5.50
March	7.70
April	8.30
May	7.90
June	6.90
July	7.70
August	7.50
September	6.90
October	6.30
November	5.50
December	4.80

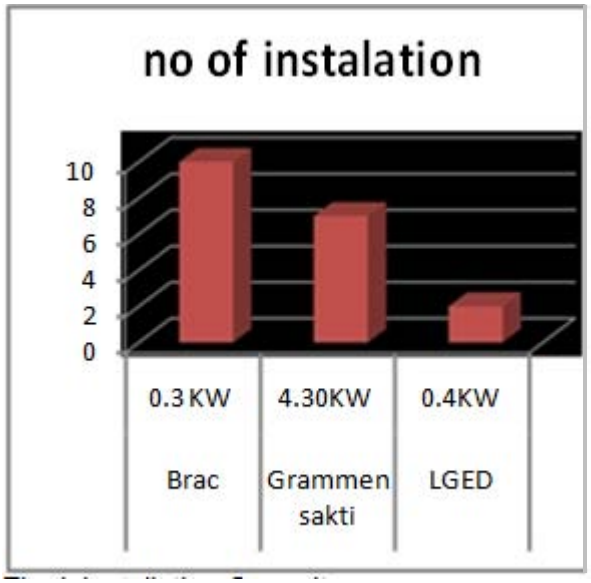

Figure 4 : Installation Capacity

Grid Connected Wind Energy (GCWE) in the Muhuri Dam areas, which is suitable for 100MW wind electricity [13]. BPDB has planned to implement 50-200 MW Wind Power Project at Parky Beach area, Anawara, Chittagong. BPDB has also planned to install 1MW off Grid Solar- Diesel based Hybrid Power Plant in Kutubdia Island. 10KWp capacity based Wind-Solar Hybrid System installed by LGED in Saint Martin Island at Bay of Bengal. GS has installed seven numbers of wind-diesel systems of 4.32KW capacity at coastal areas. BRAC has also installed .3KW capacity based wind turbine. Here fig-4 shows installation of wind hybrid systems. A pilot project has taken to set up 250KW capacity based diesel power stations at Kutubdia and Kuakata. The estimated annual energy outputs for Kutubdia and Kuakata are about 200MWh and 230MWh respectively from a 250KW station at these places [14].

a) Utilization of wind energy

Wind speed is not sufficient in Bangladesh to produce wind electricity. But this electricity can be utilized in different ways such as wind water pumping and power generation through Wind-Diesel-hybrid systems, small battery charging, shrimp production, fish/poultry firming, salt/ice production, fish-mill industries, hatcheries, domestic applications and vegetable irrigation.

b) Benefits of wind energy

Wind energy has not utilized properly in Bangladesh due to the lack of wind speed and huge cost. However, it has some benefits. Those are given below:

- The wind is free and with modern technology, it can be captured efficiently.
- Once the wind turbine is established, the produces energy does not cause green house gases or other pollutants.
- Although wind turbines may rich in height, each have only a small piece of land. This means that the unused land can be utilized for other purposes, especially for agricultural or farming purposes.
- Remote areas where electricity has not supplied yet can use wind turbines to produce their own supply.
- Wind turbines have a role to play in both the developed and third world.
- Wind turbines are available in a range of sizes, which means a vast range of people, and businesses can use them.
- Single households to small towns and villages can make good use of range of wind turbines available today.
- Wind energy is a clean renewable energy source cheaper to maintain, saves fuel and can give decentralized energy [14].

V. Solar Energy

Solar power is the conversion of sunlight into electricity, either directly using photovoltaic (PV), or indirectly using concentrated solar power (CSP). Concentrated solar power systems use lenses or mirrors and tracking systems to focus a large area of sunlight into a small beam. Photovoltaic converts light into electric current using the photoelectric effect. Average daily solar radiation is 4-6.5 kWh/m in Bangladesh. The first significant program of solar system was Norshingdi project. Under this project, solar home systems (SHS) with a total capacity of 32.586KWp were installed [15]. Under Renewable Energy Technologies (RET) 40.5KWp capacity based solar systems have installed through LGED from 1998 to 2006. BPDB has installed several types of solar systems such as Solar Home System (SHS), Solar Vaccination, Solar water pump, Solar Street light, Centralized Solar PV Power Plant of 123.55kWp (233.095KW or 0.233MW) [16]. From 1993 to 2007 REB established SHS of 233.095KW (0.233MW)

capacity. Private organizations such as BRAC and GS also installed valuable solar systems in the rural areas. Recently BPDB has taken a project to implement 1000 Solar Home Systems of 120Wp each in Chittagong hill tracts. Government of Bangladesh (GOB) has taken a solar program under which about 400 no's of solar panels has been installed in Juraichhri area of Rangamati district. Fig-5 shows installation through various organizations. A fig [6] of solar panel is shown below [17]. Cost of solar power has decreased about 60% from 1991 to 2003 and decrease about 47% from 2006 to 2010 [18]. Now 30% household works can be done through SHS system [19].

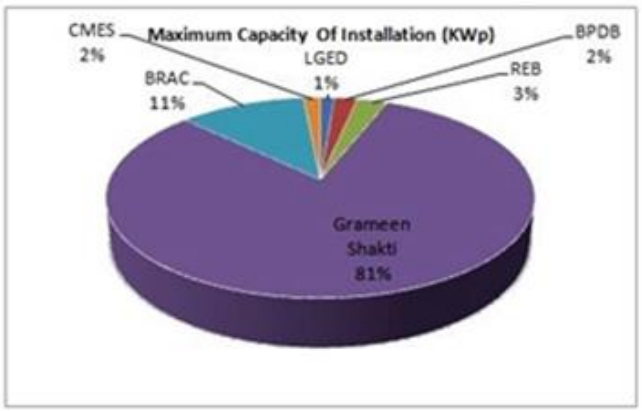

Figure 5 : Installation capacity of Solar panels

a) Utilization of Solar energy

Due to graphical location, Bangladesh has huge opportunities to use solar energy. Instead of having some bad impact on climate as well as CO_2 impact however the blessing of solar energy is untold [32]. So far this energy can be utilized in many activities of daily life as solar lighting, pumping, irrigation, solar park, poultry-firms, small dc applications etc.

b) Benefits of Solar energy

Most of the rural areas where people are suffering from energy crisis, solar energy can bring them solution through its some benefits as:

- Solar energy is free although there is a cost in the building of "collectors" and other equipment required to convert solar energy into electricity or hot water.
- Solar energy does not cause pollution. However, solar collectors and other associated equipment/ machines are manufactured in factories that in turn cause some pollution.
- Solar energy can be used in remote areas where it is too expensive to extend the electricity power grid.
- Low cost and easy installation.
- Could be an effective alternative source of energy.
- Energy can be stored in the battery.

Figure 6 : Solar panels at Rangamati

VI. Geothermal Energy

Geothermal energy is very much cost effective and environmentally friendly thermal energy generated and stored inside the earth surface. To generate electricity, the steam and hot water produced inside the earth surface is used in this technology. Geothermal energy is a reliable source of power that can reduce the need for imported fuels for power generation and emits almost no greenhouse gases. As renewable, it based on a practically limitless resource of natural heat within the earth. Geothermal energy is generated about 4,000 miles below the surface, in the earth's core. The process takes place due to the slow decay of radioactive particles, the high temperature produced inside the earth and it happens in all rocks. About 10,715 megawatts (MW) of geothermal energy is generated in 25 countries worldwide [21]. The first geothermal power plant for electricity generation in Bangladesh is under construction, which will thus become the twenty-sixth country in the world to use this source of renewable energy [22]. The northern districts of Bangladesh show the prospect to explore the geothermal resources. Also there is a hot salt water spring known as Labanakhya at Sitakunda (40 kilometer from Chittagong) which has the possibility to

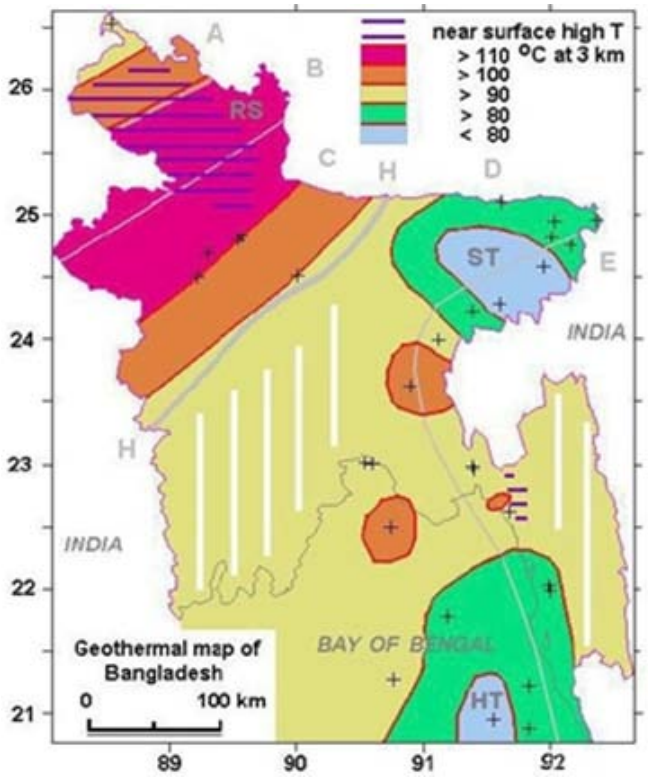

Figure 7 : Geothermal map of Bangladesh

be an excellent location for the extraction of geothermal energy, and so further investigation is required to fully evaluate its potential. Recently, the Ministry of Power, Energy and Mineral Resources has approved the establishment of the first ever-geothermal power plant in the country [23]. The demand of electricity in urban as well as in the rural areas are increasing, but our production of electricity is not increasing. The rural demand for electricity can be covered by the production of electricity through geothermal energy. A private company named Anglo MGH Energy has planned to setup Bangladesh's first geothermal power plant with a capacity to produce 200 MW. Plants for 200 MW are in the pipeline at Salandar village in the northern district of Thakurgain [22]. The company has done primary feasibility studies on the plan and will conduct a final one shortly on a span of 3500 hectares of land to select the spot for the plant. The Company has secured favorable opinions from the Geological Survey of Bangladesh, the Ministry of Water Resources and the Ministry of Environment and Forest [22]. According to the plan, 28 deep tube wells will be dug to lift hot steam to run a turbine connect to the generator to generate electricity, whose temperature will be at least 12 degree Celsius. These geothermal resources can therefore play a significant role as regards energy supply for populated areas, where there is a severe shortage of energy in general and specifically of electricity. Fig-7 shows geothermal energy prospects of Bangladesh (Guha et al., 2010) [24]. The establishment cost of geothermal power plant is high due to the high cost of drilling wells, it can be reduced by using the abandoned on shore dry wells which have sufficient high temperature gradient (like over 30K/km) [23]. Geothermal energy can provide a suitable energy solution for Bangladesh as it is green, indigenous, abundant, continuously available and independent of climate changes [23]. With the population of over 156 million inhabitants, it must be noted that 200MW are not sufficient to consider the solution of energy crisis where the total installed power capacity is currently about 6000 MW [22].

VII. Hydro Power

Flowing water creates energy that can be captured and turned into electricity. This is called hydroelectric power or hydropower. It is an eco- friendly clean power generation method. As a riverine country, Bangladesh is a great delta formed by the alluvial deposits of the three mighty Himalayan Rivers: the Ganges, the Brahmaputra and the Meghna [25]. Also there are lots of canals, tributaries of main river Karnafuli, Shangu, Matamuhuri as well as tiny waterfalls having good potentials for setting up mini/ micro hydropower unit in Chittagong Hill Tracts (CHT) region [26]. At present only 230 MW of conventional hydro power is utilized in the Karnafuli Hydro Station, which the only conventional hydro-electric power plant in the country operated by Bangladesh Power Development Board (BPDB). BPDB is considering extension of Karnafuli hydro Station to augment another 100 MW capacity, which will add energy marginally, but will be effective to operate it as a peaking power plant. The additional energy will be generated during the rainy season when most of the water is spilled [8]. Classifications of hydro power based on generated power are as follows:

Pico-Hydro<5KW

micro-hydro>5<300KW

Mini-hydro>300KW <3MW

Small hydro > 3MW < 10MW

Bangladesh Water Development Board (BWDB) and Power Development Board (BPDB) carried out a joint study on Micro-Hydro power potential in the country. In Table-4, it is given in detail [23].

Table 4 : Potential Small Hydro Sites identified by BPDB and BWDB

District	Name River/Chara /Stream	Potential of Electrical energy in KW
Chittagong	1. Foy"s lake	4
Chittagong	2. Choto Kumira	15
Chittagong	3. Hinguli Chara	12
Chittagong Hill Tracts	4. Sealock	81

Chittagong	5. Lungichara	10
Chittagong	6. Budiachara	10
Sylhet	7. Nikhari Chara	26
Sylhet	8. Ranga Pani Gung	616
Jamalpur	9. Bhugai-Kongsa at 2 miles U/S. Of Nalitabari P.S	69KW for 10 months 48 KW for 2 months
Jamalpur	10. Marisi at Dukabad near Jhinaigati Thana Head Quarter	35KW for 10 months 20 KW for 2 months
Dinajpur	11. Dahuk at Burabari	24
	12. Chawai at U/S. of Chawai L.L.P	32
	13. Talam at U/S. of Talam L.L.P	24
	14. Pathraj at Fulbari	32
	15. Tangon at D/S of Nargun L.L.P	48
	16. Punarbhaba at Singraban	11
Rangpur	17. Buri Khora Chikli at Nizbari	32
	18. Fulkumar at Raiganj Bazar	48

SRE under LGED has successfully demonstrated first micro-hydro power unit at Bamerchara Lake, Banshkhali, and Chittagong district in Bangladesh. Its installed capacity was 10kW but due to inadequate water head about 4kW power was generated. Estimated capacity of the system was 10kW. Salient feature of the unit has been illustrated below [26]:

- Turbine type : Corssflow
- Penstock : 52m
- Design flow : 150 litter/sec.
- Net head available : 6m-10m
- Preferred gove : Flowcontrol (Manual)
- Electrical Output : 4-6 KW, 50Hz, 3 phase voltage, 220 V / 440 V

SRE has carried out a study on prospective micro-hydro sites in the Chittagong Hill Tract region and eight potential sites were identified with an estimated capacity of 135kW. It also provided technical support to promote indigenous technology (wooden water wheel which is driving locally procured generator) of micro-hydro power generation unit which was developed by member of local indigenous community named Mr. Aung Thui Khoyan [27]. A recent study on Sustainable Rural Energy shows that micro hydro power plants are able to provide necessary power supply for rural areas. According to socio- economic development strategy, the study was conducted on the micro hydro power plants of generation capacity starting from 3KW up to 30KW [27] [28].Table-5 shows socio- economic development & Fig-8 represents power generation capacity of these plants:

Table 5 : Micro hydro plants of Bangladesh

Site	Expected Power Generation (KW)	Socio- economic Infrastructure within 1 km		
		House hold	School/ Mosque / Bazar/ Clinic	Small Industry
Nunchari Tholipara, Khagrachari	3	100	3	1
Chang-oo-Para, Bandarban	30	200	5	2
Bangchari, Bandarban	25	600	12	5
Liragaon, Bandarban	20	500	8	3
Kamalchar, Rangamati	20	150	8	9
Thang Khrue, Rangamati	30	300	6	3
Monjaipara, Bandarban	7.5	50	9	-

a) Ongoing Projects of Hydro Power in Bangladesh

- BPDB has taken steps to install 50-70 kW Mohamaya Irrigation-cum-Hydro Power Project at Mirersorai, Chittagong [28].
- Rehabilitation of 50 kW Micro-Hydro Power Plant at Barkal Upazila of Rangamati district [28].

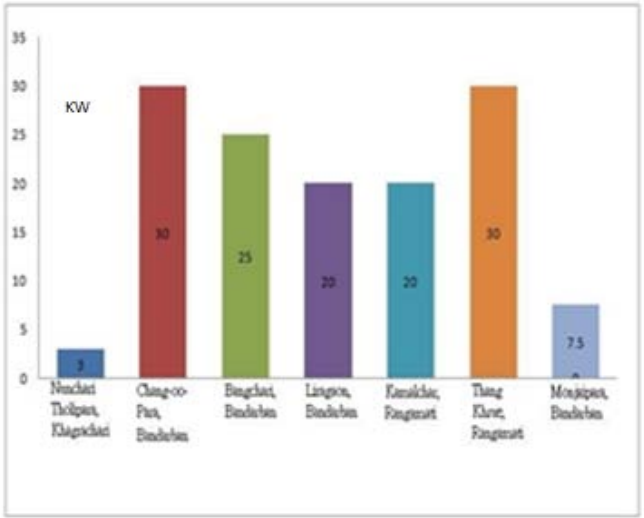

Figure 8 : Power generation capacity of Micro- Hydro plants

There are many rivers with high flow rate in monsoon but low in winter. It would be a good idea to create a diversion structure across the river channel, diversion channel along the bridge and the powerhouse at a suitable location that offers a suitable head. The Teesta Barrage, the largest irrigation project of the country has several sites with sufficient head. BPDB has submitted a proposal to the government to install a 25kW power plant at the Teesta barrage. Further investigation can open the door to more success in this regard. To improve development outcomes, Bangladesh has good potential of hydro power through micro/ mini hydro power and its proper utilization can bring effective changes to energy sector in upcoming days.

VIII. Economic Development

Now Bangladesh has started to have advantages of renewable energy. Day by day, it becomes cheaper. Rather than high power equipments, long transmission and distribution line and other installations, it becomes easier to set up. Due to fall in price, people become interested in biomass and solar energy. This motivation saves money and makes our life easier. This also influences our social and economical activities. Renewable energy reduces dependency of natural fuel. Employment opportunities are increasing for rural people. Especially green jobs where people can produce harmless chemical pesticides and fertilizer, Compact Fluorescent Light (CFL) to reduce 80% of electricity cost [30]. Here fig-9 illustrates employment estimation through renewable energy.

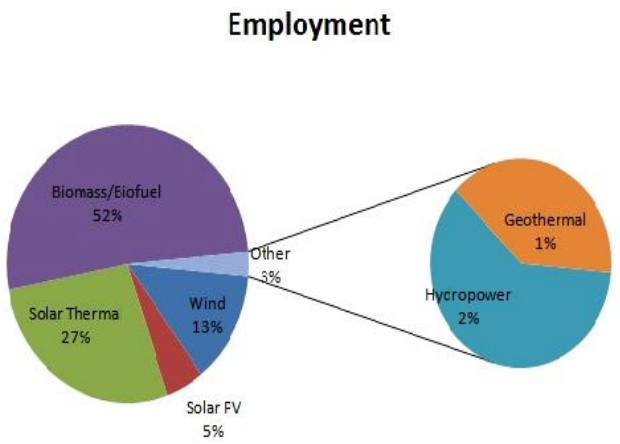

Figure 9 : Employment estimation around the world

IX. Conclusion

Bangladesh, the land of natural resources, rich in gas, limited amount of coal, oil as diesel and kerosene. These natural resources are stored in deep soil and sea blocks. As if, carry out these resources through open access digging from soil is very much expensive and harmful for environment. For this Proper utilization and installation of biogas plants, solar panels and wind turbines could be cost effective for our economy. Bangladesh is mainly dependent on natural gas and imported oil. Excessive use of natural energies may cause bad impact on GDP (Gross Domestic Product). A prediction estimates that maximum reserve of natural energy sources will deplete within few decades. So dependency on natural sources should be reduced. If we create diversity to renewable energy then it will be our achievable energy sources in near future. However, Economic development through renewable energy can play a vital role to reduce unemployment and poverty, which is helpful for Bangladesh to continue her journey with global world.

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Design, Simulation & Performance Evaluation of OFDM System to Reduce PAPR using SLM & LCM with FPGA

By Rajesh S. Bansode, Dr. B.K Mishra & Aqsa Temrikar
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Abstract- High peak-to-average power ratio (PAPR) of the transmitted signal is a major drawback of orthogonal frequency division multiplexing (OFDM). Selected mapping (SLM) technique is one of the promising PAPR reduction techniques for OFDM. In the SLM technique, statistically independent data blocks are generated from an OFDM data block using a set of phase sequences and one with the lowest PAPR is chosen and transmitted. In this paper, we propose an SLM technique which gives sizable reduction of nearly 2dB. The paper elaborates the hardware implementation of the generated block using FPGA. The test benches and the RTL schematic are generated.

Index Terms: *field programmable gate array, matlab simulink, orthogonal frequency division multiplexing, selective level mapping, peak-to-average power ratio and xilinx.*

GJRE-F Classification : *FOR Code: 290903p*

Strictly as per the compliance and regulations of :

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Rajesh S. Bansode [α], Dr. B.K Mishra [σ] & Aqsa Temrikar [ρ]

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I. Introduction

The root of Orthogonal Frequency Division Multiplexing (OFDM) scheme is traced back to 1960's when it was first proposed by Chang in 1968 . Since then, there has been a vigorous research effort in developing OFDM-based wireless communication systems. Over the years, OFDM has become to be the most popular transmission scheme for broadband communication systems that require high-speed 4G communication with 100 mbps data rate. Its increasing popularity is due to its spectral efficiency and inherent ro-bustness to channel impairments. In addition, the OFDM waveforms offer substantial improvements in performance over traditional single carrier approaches.[2]

Various applications of OFDM are Digital Audio Broadcast-ing (DAB) and Digital Video Broadcasting (DVB) in Europe, and for Asymmetric Digital Subscriber Line (ADSL) high data rate wired links. OFDM has also been standardized as the physical layer for the wireless networking standard 'HIPERLAN2' in Europe and as the IEEE 802.11a, g standard in the US, promising raw data rates of between 6 and 54Mbp[14]. Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier-based technique for mitigating ISI to improve capacity in the wireless system with spectral efficiency.[1]

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The paper aims at successful implementation of the transceiver on a FPGA which would pave a way towards developing an OFDM system which resolves the issue of high PAPR. Simulation results using System Generator and Matlab/Simulink and XILINX tools have been given in the paper."Low Crest Method" which is the selected technique of PAPR reduction is given in thi spaper. Finally it aims at development of a complete system which then results in robust, maximum throughput, highly scalable wireless LAN network.[2]

II. OFDM and PAPR

a) General OFDM Block Diagram Description

i. OFDM Transmitter

The model considered for the implementation of the OFDM transmitter is the shown above and basically consist of the following blocks:[13]

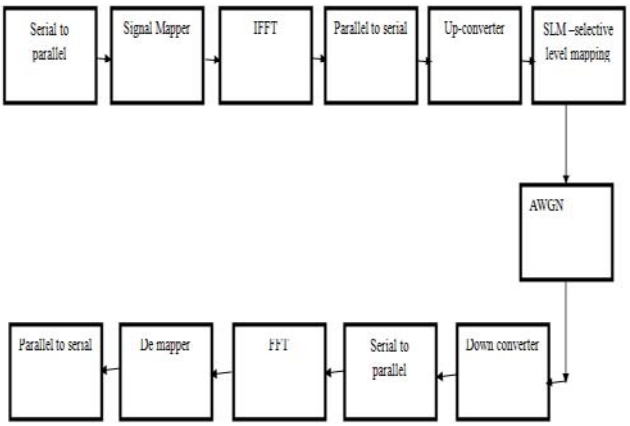

Figure 2.1 : Block diagram of an OFDM system

Serial to parallel converter, Constellation modulator, IFFT block, Parallel to serial converter, Digital to Analog converter, Selective Level Mapping.

ii. OFDM Receiver

The blocks of the OFDM Receiver are detailed below:

Analog to digital converter, Serial to parallel converter, Cyclic prefix removal, FFT block, M-QAM decoder, Parallel to serial converter.

b) Peak to average Power ratio

The major disadvantage of using several subcarriers in parallel using IFFT is the highly non-constant envelope of the transmit signal, making OFDM

very sensitive to nonlinear components in the transmission path. A key component is the high power amplifier (HPA). Due to cost, design and most importantly power efficiency considerations, the HPA cannot resolve the dynamics of the transmit signal and inevitably cuts off the signal at some point causing additional in-band distortions and adjacent channel interference. The power efficiency penalty is certainly the major obstacle to implement OFDM in low-cost applications. Moreover, in power-limited regimes determined by regulatory bodies, the average power is reduced compared to single-carrier systems reducing in turn the range of transmission. The power control problem motivates further research since it touches on many of the advantages that originally made OFDM transmission popular, i.e. spectral efficiency and implementation issues.

In OFDM systems, a fixed number of successive input data samples are modulated and then jointly correlated together by use of IFFT at the transmitter side. IFFT processes signals to produce orthogonal data sub-carriers. Mathematically, IFFT combines all the input signals to produce each one of the output symbols.

The signal processing by IFFT in the OFDM transmitter changes the statistical distribution of signals from uniform-to-Gaussian. Therefore, the dynamic range of the OFDM output envelope is most often higher than that of the single-carrier systems. However, PAPR is widely used to evaluate the dynamic range of the output envelope. The PAPR (in dB) is defined by the following equation [14].

$$\text{PAPR}=10log_{10}\left\{\frac{P_{peak}}{P_{avg}}\right\}=10log_{10}\frac{max[|x(n)|^2]}{E[|x_n|^2]} \quad (1)$$

where Ppeak represents peak output power, Paverage means average output power. E[•] denote the expected value, xn represents the transmitted OFDM signals which are obtained by taking IFFT operation on modulated input symbols Xk . xn is also expressed as[12]

$$x_n = \frac{1}{\sqrt{N}}\sum_{K=0}^{N-1} X_k W_N^{nk} \quad (2)$$

c) Selective Level Mapping

Selective level Mapping (SLM) was first proposed in 1996 to reduce PAPR in OFDM systems. The system block diagram of SLM is shown below.

At first, the input information is divided into OFDM data block X, which consists of N symbols, by the serial-toparallel (S/P) conversion and then data block X is multiplied carrier-wise with each one of the U different phase sequences B(u), resulting in a set of U different OFDM data.

In the SLM algorithm the data source denoted as X, is multiplied by the U different sets of phase factors/masks, element-wise to produce U different copies of X,

$$Xu = BuX \quad u= 1, 2, ...,U \quad (3)$$

where U is the design parameter in SLM. In general, more reduction in PAPR is likely to achieved when U in-creases.[12]

In addition, Bu is defined as:

$$Bu=[Bu,1\ Bu,2\ Bu,3...\ Bu,(N-1)] \quad (4)$$

Then all U alternative data blocks (one of the alternative sub-carrier sequences can be the unchanged original one) are transformed into time domain to get transmit OFDM symbol where N represents the number of subcarriers in IFFT and Bu,k is given by:

$$Bu,k = e^{j\phi u,k} \quad k = 0, 1, 2, ...,N - 1 \quad (5)$$

After multiplying X with the phase factors, each Xu is processed by IFFTs and its PAPR is then computed and compared with the others. The resulting signal that yields the lowest PAPR is subsequently chosen for transmission. In addition, the Bopt which implies the optimal Bu that produces the lowest PAPR has to be transmitted to receiver as a side information[14]. The receiver will then use Bopt to recover the data source, X[6].

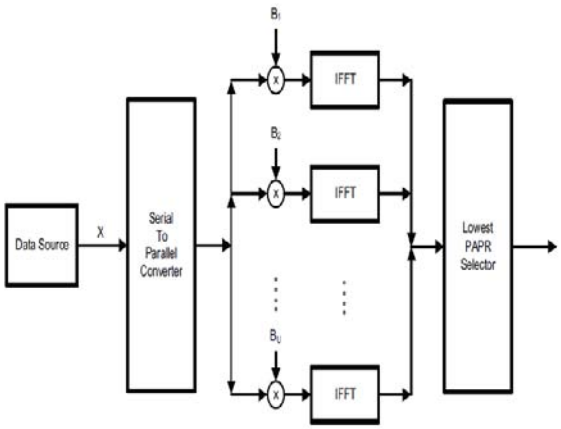

Figure 2.2 : Block diagram of SLM

III. Designed OFDM Model

The top level design contains simulink blocks for input, signal display and output. Input to the design is given from a sine wave generator or from a sound input stored in the workspace. The inputs are passed through a gateway in block to convert from floating point numbers to fixed point numbers compatible to Xilinx blockset. The data is then serialized using a parallel to serial converter and given to the OFDM transmitter. The transmitter is explained in detail in the later section. The

output of the transmitter, which is PAPR reduced serial data stream is given to the receiver to decode it. Also a certain amount of noise is added to the data stream. The receiver then decodes the stream. The final output is given from the receiver. This data is displayed and compared on the scope and also output on the workspace for comparison. Also the BER is calculated by comparing the data before and after decoding.

a) Transmitter Design

In the design presented, block length of 8 points and 4 different phase sequences are used. Transmitter subsystem design contains 4 independent OFDM modulators. In the modulator, the input data is multiplied by a look-up table from ROM before giving it to actual OFDM modulation process. This lookup table holds the phase sequences for each block. The output of each block is given to a PAPR calculator and selector. It transmits the data block with lowest PAPR and also transmits the selected block number.

b) Receiver Design

The receiver is a normal OFDM receiver with a phase sequence selector block. The data stream is first given to FFT block for decoding. Then the data stream is passed to a lookup table multiplier which multiplies data with a phase sequence as indicated by the the selected block number from transmitter.

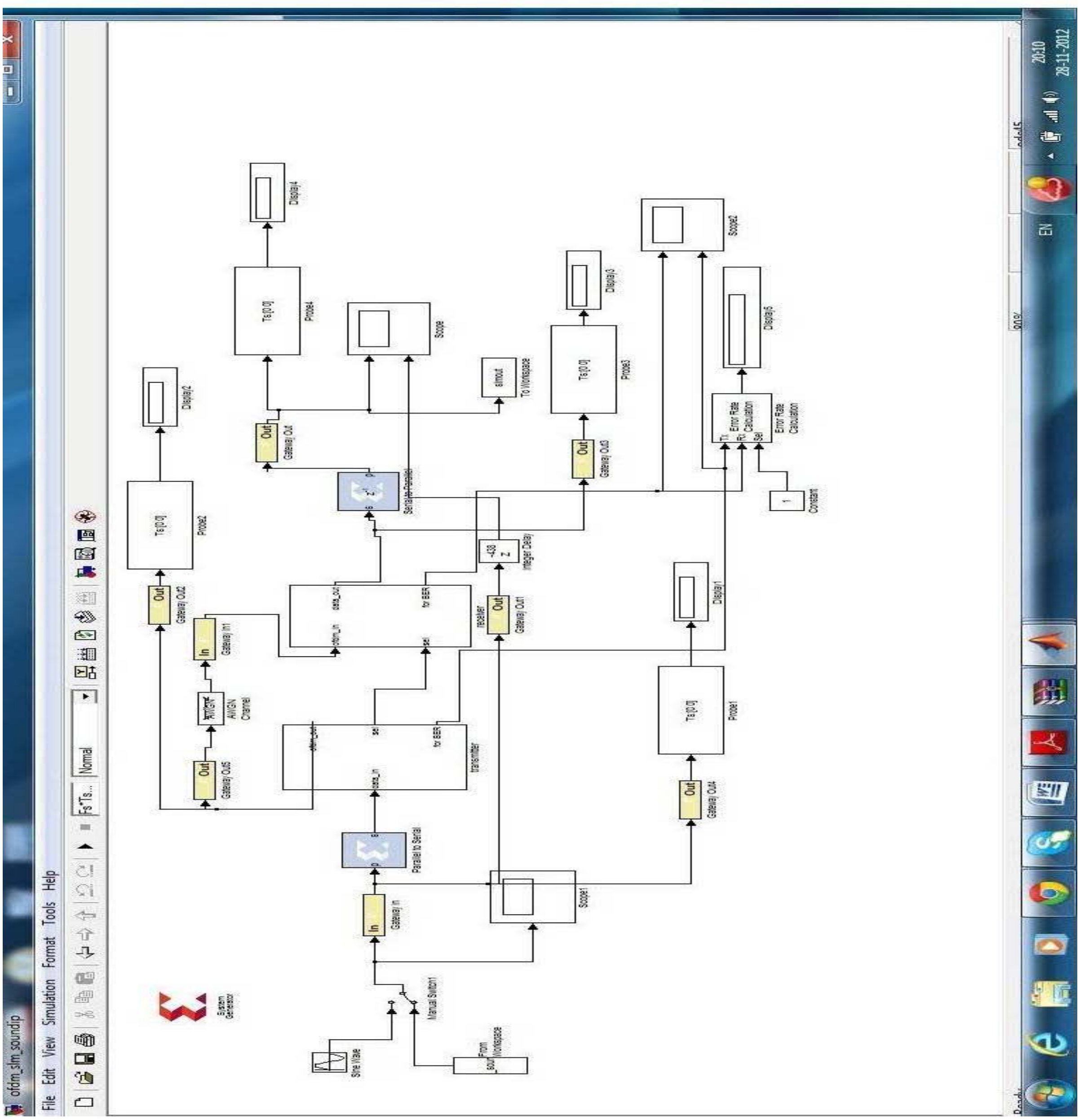

Figure 3.1 : Block diagram of the designed system

c) Transmitter Subsystem

- *Encoder*

The Figure 3.2 indictes the encoder module where there are two shift registers and two X-OR gates. Initially the shift registers have a zero bit stored in it. For the first X-OR gate there are three inputs. The first input is as it is the output of parallel to serial block. The second input is output of parallel to serial block with one delay while the third is the output of parallel to serial block with two delays. The output of the first X-OR is given out as data_out 1.

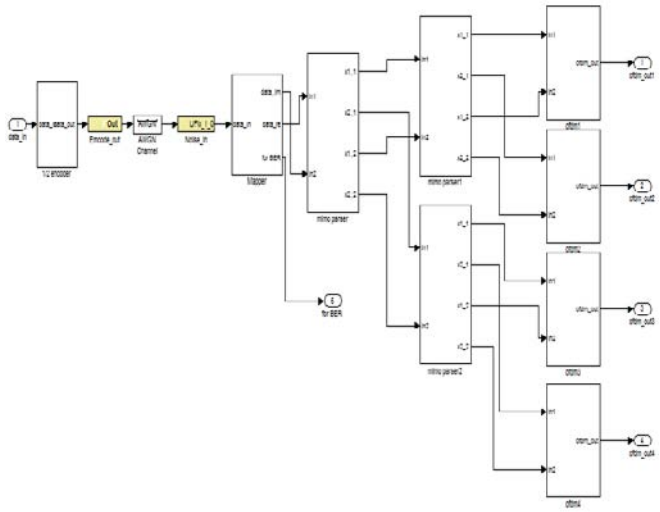

Figure 3.2 : Transmitter Module

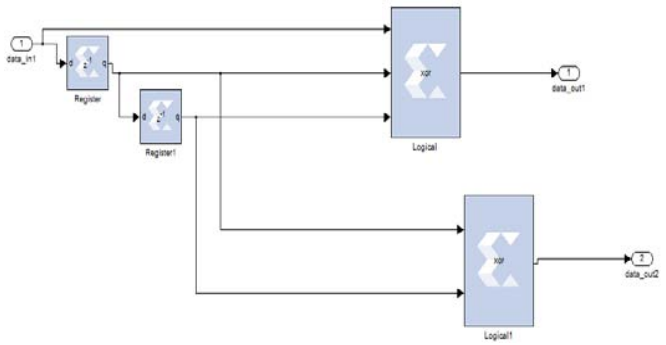

Figure 3.3 : Encoder Model

The outputs of parallel to serial blocks with one and two delays respectively are given to the second X-OR gate . The output of the second X-OR is given out as data_out 2.

- *Mapper*

The output of encoder/interleaver module is applied as input to the Mapper. The combination of ROM_Imag, ROM_Real altogether forms QAM mapper. The ROM_Imag provides the value on imaginary axis while ROM_Real provides the value on real axis. This is giving up the points on different quadrants.

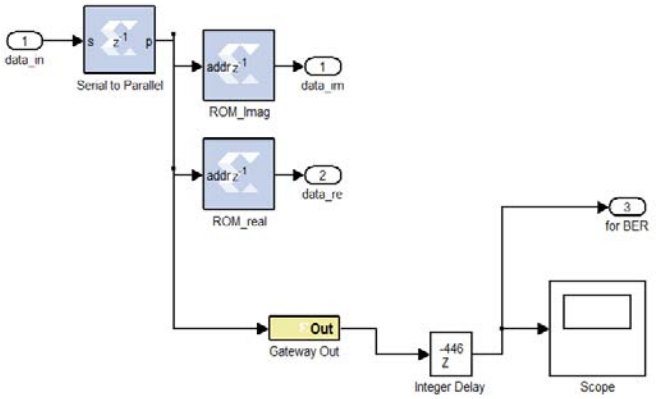

Figure 3.4 : Mapper

d) Receiver Subsystem

- *Demodulator*

The Figure 3.5 represents the demodulator i.e. demapper block. The ROM_REAL and ROM_IMAG signals are fed as input as xr and xi to the demodulator respectively. A Matlab code is used for QAM demodulator and is given out at dout.

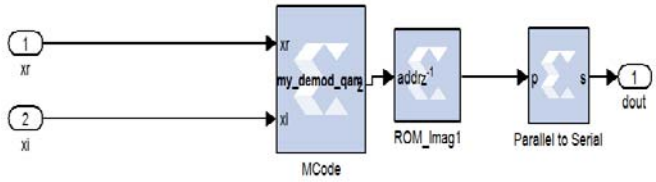

Figure 3.5 : Demodulator module

- *Decoder*

The Figure 3.6 represents the decoder which consists of serial to parallel block and a decoder block. A Matlab code is written for the purpose of decoding the actual data.

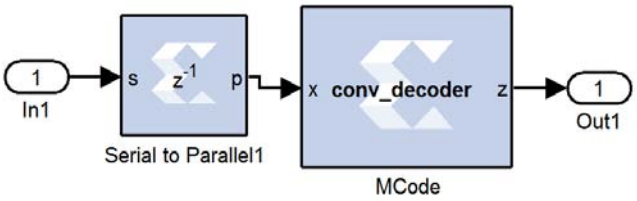

Figure 3.6 : Decoder module

IV. Implemented SLM Block

The SLM algorithm applied in this model uses 4 OFDM se-quences of 8 point each and applies 4 different mask on each sequence [6]. Blocks B1-4 are OFDM blocks which each multiply the input sequence with a predetermined mask. IFFT is then calculated on the masked stream. The PAPR calculator evaluates the PAPR for the stream independently. The stream with the lowest PAPR is then selected for transmission. Along with the stream, the stream number is also transmitted

for the receiver to know which mask to apply to decode the sequence.

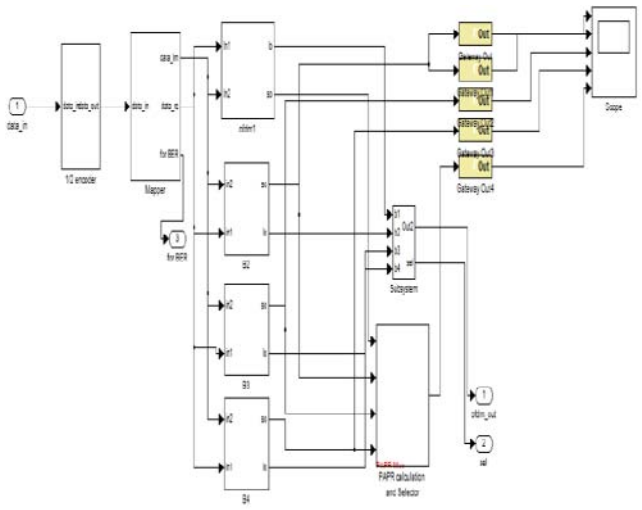

Figure 3.7 : Showing PAPR calculation block

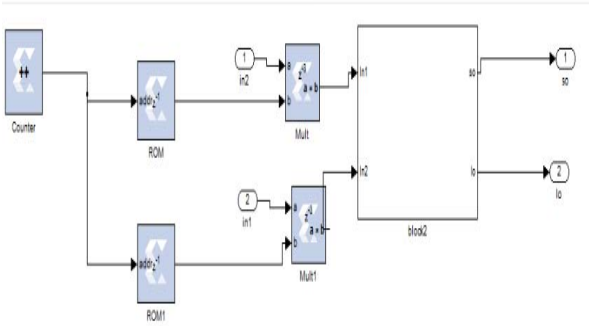

Figure 3.8 : Inner details of one of the 4 OFDM blocks

V. Hardware Implementation

Using XILINX and modelsim the developed simulink model is converted into its JTAG equivalent.[2] Internal simulator of XILINX, i-sim can also be used in place of modelsim.[20]

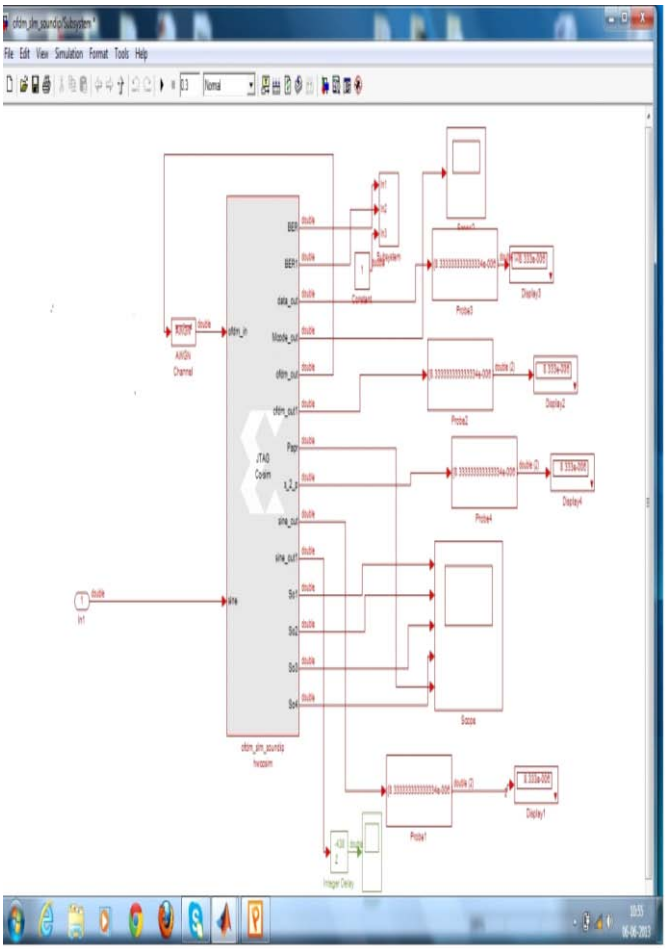

Figure 3.9 : JTAG-Hardware Co-sim block

The hardware implementation of the simulink model is done using JTAG. The process of developing such a hardware is called Hardware-In-Loop.

VI. Methodology

The algorithm of each block using Matlab Simulink is imple-mented by use of constructing block diagrams in Simulink. VHDL code is imported into Simulink using the Xilinx Sys-tem Generator block set, which gives flexibility to design flow. Simulink and Xilinx System Generator create bit-true. The Xilinx Integrated Software environment (ISE) is used as the synthesizer in the design flow diagram. ModelSim is used to verify the hardware simulation of the blocks by using test vectors generated by System Generator or HDL test benches. Finally synthesis and performance results of the blocks are reported using ISE, and bit streams are generated to program the FPGA board. [24][25].

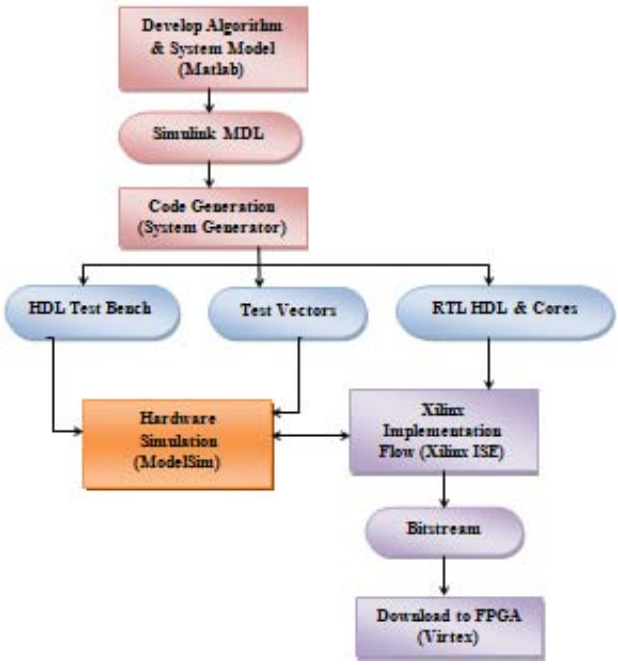

Figure 4.1 : Methodology and flow diagram [24][25]

VII. Result and Discussion

a) FPGA kit analysis

The DONE LED glows indicating that the FPGA is now ready to be programmed.

The output of the scope can be seen in the Figure 5.2 where the first waveform is the signal which has been achieved at the output of model which is the received signal and the second waveform is the actual signal which was been fed as input to the model.

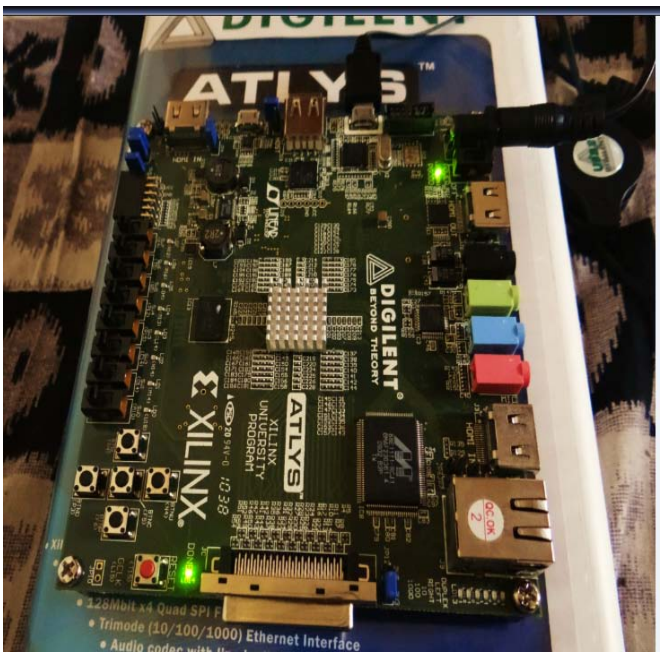

Figure 5.1 : FPGA ready for programming[25]

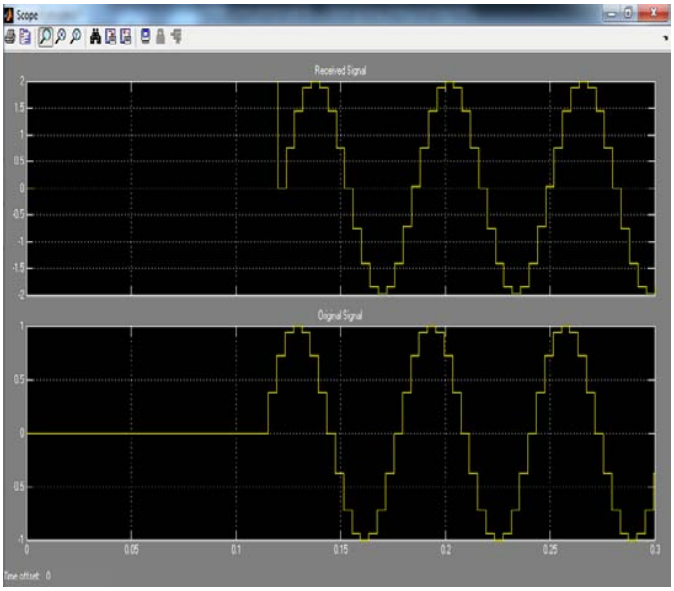

Figure 5.2 : Received and Original Signal (Test sinewave)

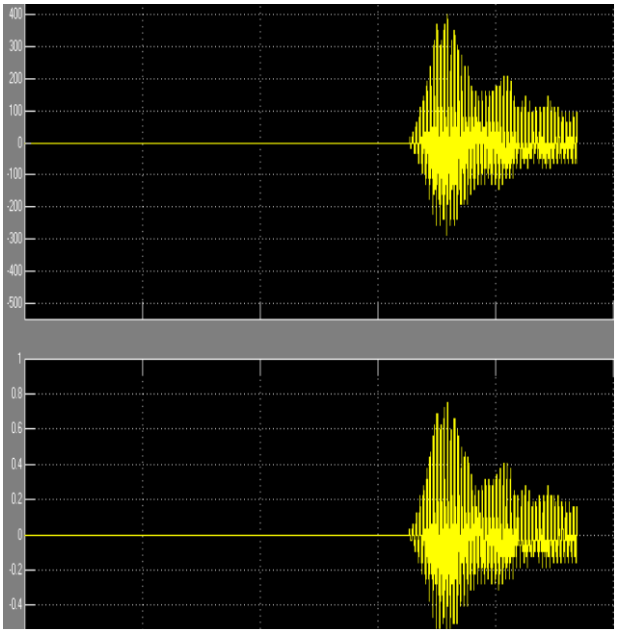

Figure 5.3 : Received and Original Signal (Realtime audio sinewave)

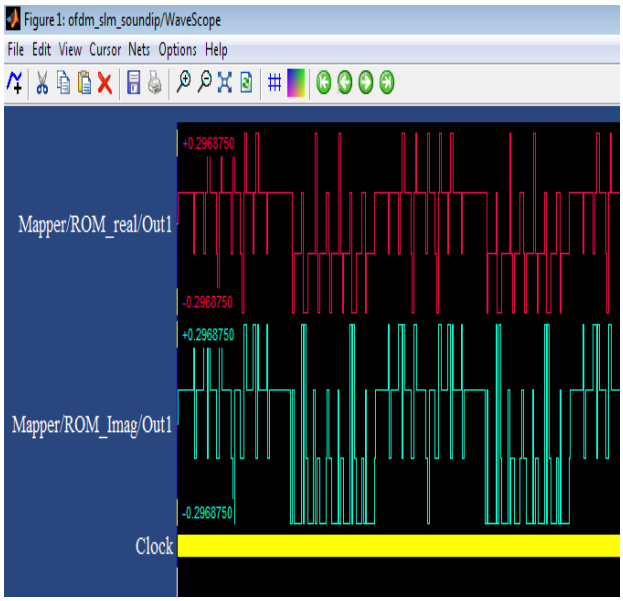

Figure 5.4 : Output of Wavescope (after running it for 30 secs)

b) Output of the wavescope- QAM Explaination

Wavescope block shows following two signals. First one is Rom_real and Rom_imaginary as shown below. These two signals represent the real and imaginary part of the input signal resulting in 16 – QAM.

After running the model for almost 30 seconds and the wavescope block is opened. The following output is observed.

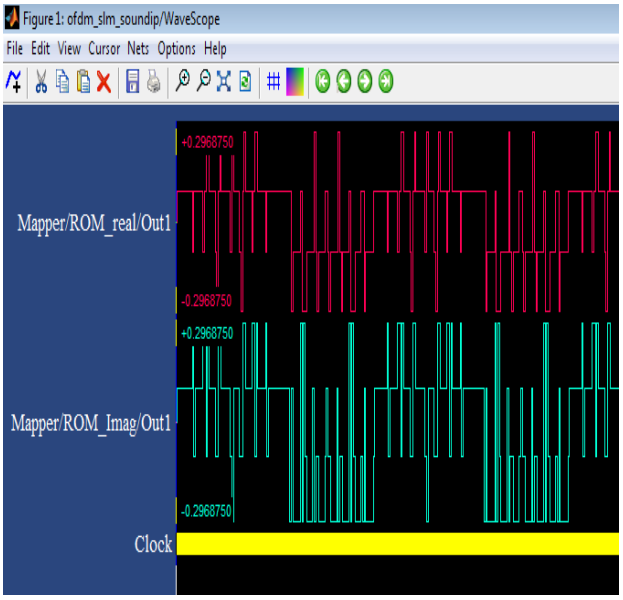

Figure 5.5 : QAM Output

Observing the output carefully, it is seen that the signal is repeating after certain intervals (16 Frames) as shown by square.

From the waveform it is clearly observed that the maximum and minimum value for the real and imaginary signal is same and it is (+0.29) as shown below.

Table 5.1 : Showing 16-Qam Constellation Points

QAM Input Symbol	QAM constellation	Array Index	Array Value (Real + j*Imaginary Part)
0	-3-3j	0000	-0.29 – 0.29 j
1	-3-1j	0001	-0.29 – 0.10j
2	-3+3j	0010	-0.29 + 0.29j
3	-3+j	0011	-0.29 + 0.10 j
4	-1-3j	0100	-0.10 – 0.29 j
5	-1-1j	0101	-0.10 – 0.10 j
6	-1+3j	0110	-0.10 + 0.29j
7	-1+j	0111	-0.10 + 0.10 j
8	+3-3j	1000	+0.29 – 0.29j
9	+3-1j	1001	+0.29 -0.10j
10	+3+3j	1010	+0.29 + 0.29j
11	+3+j	1011	+0.29 + 0.10j
12	+1-3j	1100	+0.10 – 0.29j
13	+1-1j	1101	+0.10 – 0.10j
14	+1+3j	1110	+0.10 + 0.29j
15	+1+j	1111	+0.10 + 0.10j

Thus the signal lies between +0.29 to -0.29 on both real and imaginary axis.

From the repeated sequence of 16-QAM in the model from Rom_real and Rom_imaginary signals, it is concluded that the signal represents the non uniform 16– QAM.

From the above symbols , the 16 – QAM Constellation Map-ping is obtained.

VIII. Hardware Co-Simulation

ofdm_slm_soundip_cw Project Status			
Project File:	ofdm_slm_soundip_cw.xise	Parser Errors:	No Errors
Module Name:	synth_reg_w_init	Implementation State:	Synthesized
Target Device:	xc6slx45-3csg324	•Errors:	
Product Version:	ISE 12.3	•Warnings:	
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

Figure 5.6 : project status report

a) Project Status Report

The following diagram shows the project status report which includes details like:

Project file name, target device, product version etc.[20]

b) RTL Schematic

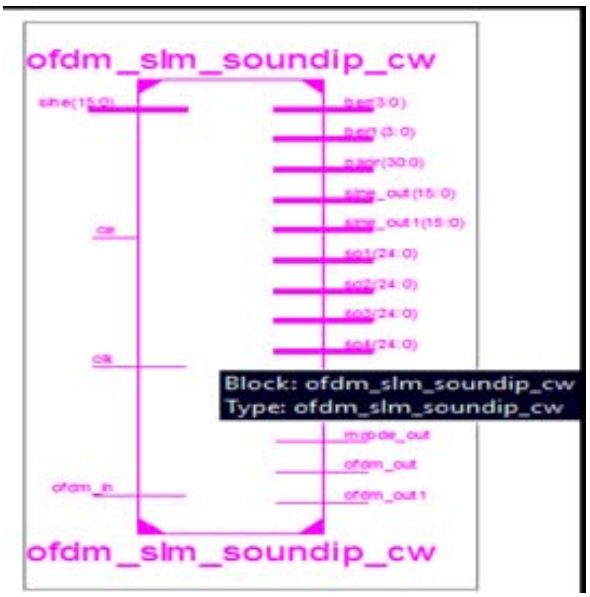

Figure 5.7 : RTL Schematic

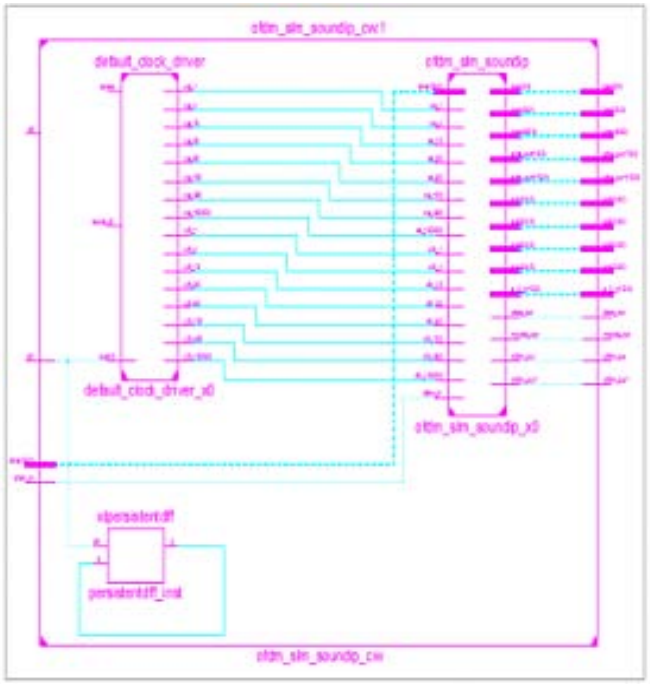

Figure 5.8 : RTL Schematic inside ofdm_soundip_cw

c) Test Benches

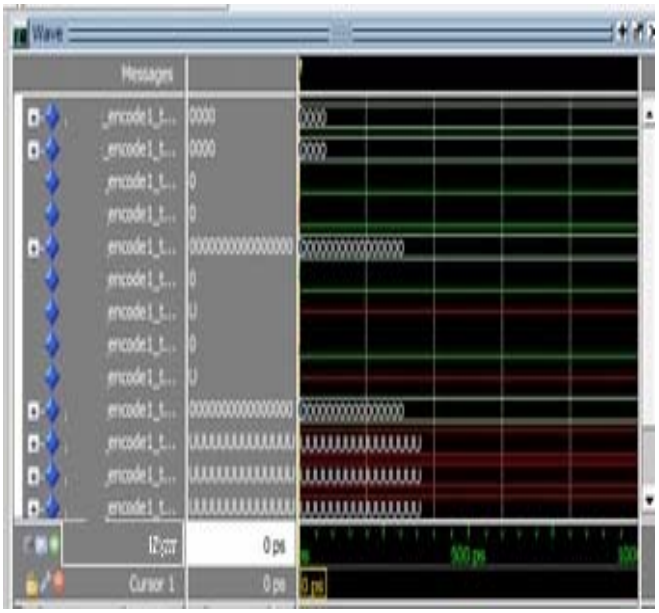

*Figure 5.9 .*Generating Test Bench

d) Graphs Plotted

Table 5.2 indicates PAPR values with SLM and without SLM. Last coloum shows Crest Factor(√ K).

It is evident from the table that PAPR reduction of about 2 dB is obtained using 64 carriers.

Varying difference in PAPR is obtained using 2,4,8 and 64 number of carrier.

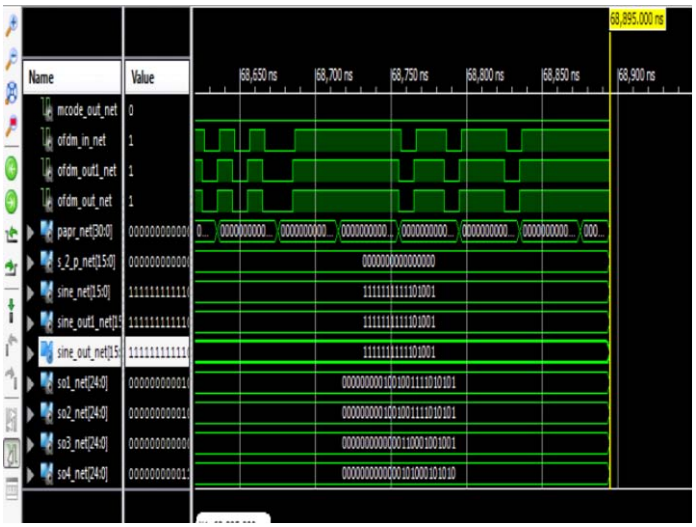

Figure 5.10 : Test Bench [20]

PAPR reduction of nearly 1.6dB is obtained using 2 carriers. Higher reduction of PAPR is obtained using 8 carriers.

Table 5.2 : Papr Values With and Without Slm, Crest Factor

Number of carriers	PAPR without SLM in dB	PAPR with SLM in dB	Difference in PAPR	Crest Factor =□√K
2	12.61	11.01	1.6	1.264
4	25.22	24.01	1.21	1.1
8	37.83	35.03	2.77	1.67
16	50.45	48.89	1.56	1.24
32	63.06	62.01	1.59	1.024
64	75.76	73.76	2	1.414

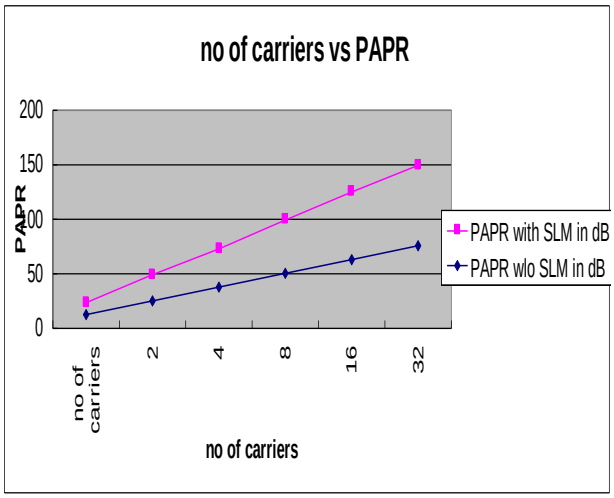

Figure 5.11 : Number of carriers v/s PAPR

As number of carriers increase the PAPR increases. Implementing the proposed technique PAPR can obtain reduction in PAPR.

Table 5.3 : Probability of Papr and Papr (Db)

PAPR in dB	Without SLM	With SLM
0	0.985	0.945
1	0.984	0.944
2	0.9832	0.944
3	0.983	0.9
4	0.982	0.85
5	0.981	0.8
6	0.98	0.712
7	0.885	0.612
8	0.8	0.511
9	0.7	0.21
10	0.6	0
11	0.512	0
12	0.001	0

The above table shows that nearly 2 dB reduction is achieved by using LCM technique.

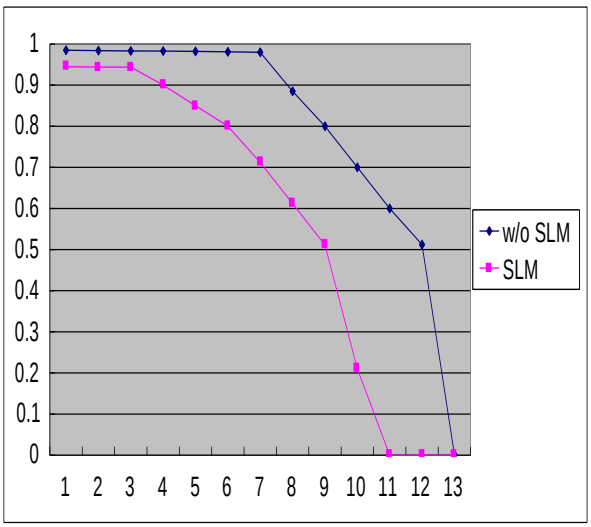

Figure 5.12 : CCDF of PAPR v/s PAPR(in dB)

The PAPR without SLM for OFDM system is 12dB and with SLM is 10dB resulting in overall reduction of 2dB.

It is observed from figure.5.17 that in case of OFDM systems without employing SLM technique the PAPR that is evaluated is constant upto 10dB and it results in a steep slope after 10dB terminating at 12dB. The OFDM system with SLM block for which the PAPR is calculated initially remains constant between 0 to 2dB and 3 to 5dB but varies between 5 to 10dB. Thereby the final PAPR with SLM is 10dB and without SLM is 12dB resulting in overall PAPR reduction of 2dB.

Difference of PAPR in **dB** calculated for OFDM system with & without SLM	PAPR calculated as factor not in **dB**	Crest Factor as **Sqrt(PAPR)** as factor not in **dB** - C^2
2dB	**1.58483**	**1.2589**

Crest Factor=√ PAPR

IX. Conclusion

OFDM is a very attractive technique for wireless communications. One of the serious drawbacks of OFDM is very high PAPR when the input sequences are highly correlated. The PAPR obtained without SLM for OFDM system is 12dB and with SLM is 10dB resulting in overall reduction of 2dB. Thus SLM technique has the potential to reduce PAPR for OFDM systems and improve its performance in terms of low PAPR high SNR and improved BER.

Xilinx System Generator combined with Matlab Simulink provides an easier and efficient way of developing the FPGA system design and simulating it. Also the hardware co-simulation feature of the software enables easier way to test and debug the design effectively on the actual hardware.

The hardware co-simulation, RTL Schematics, Test Bench and VHDL codes, are also obtained for the implemented OFDM system. First the model is created in the Matlab/Simulink environment. The Matlab Simulations were carried out and necessary modifications were done. The hardware co-simulation was done to run the model on the hardware platform. The VHDL code, RTL Schematics and Test Bench were generated for the model. Test Vectors are passed through the test bench to verify functionality of the each block of the model. At the end complete functionality of the model is verified using Matlab Simulations, Test Bench/Modelsim Simulations and Hardware co-simulations.

e) Future Scope

The paper deals with reduction of PAPR in a SISO OFDM. The concept of reduction of PAPR can be implemented in MIMO technology. If such a model is implemented it shall give the advantages of low PAPR as well as high data rate, which is an advantage of MIMO.

Different modulation techniques such as QPSK or QAM ac-commodating number of subcarriers as 1024 or up to 4096 can be experimentally tried to achieve data rates in multiple of 100 Mbps or more.

The new system model can emphasis on performance of Signal to Noise Ratio, Bit Error Rate, CDF and CCDF with respect to channel capacity.

X. Acknowledgement

Our thanks to the experts who have contributed towards development of this paper.

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Effect of Syntesis and Frequency on Electrical Properties on Dielectric Ceramics $MgCO_3$-TiO_2

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Keywords: *sintering, mechanical activation, dielectric constant, quality factor.*

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Effect of Syntesis and Frequency on Electrical Properties on Dielectric Ceramics $MgCO_3$-TiO_2

Vera V. Petrovic [α] & Hranislav Milosevic [σ]

Abstract- Magnesium titanate based dielectric materials are used for producing type-I capacitors. A common way of obtaining this material is a solid-state reaction. The process of sintering can be enhanced if mechanical activation preceedes. In this work starting powders of magnesium carbonate ($MgCO_3$) and titanium dioxide (TiO_2) with a rutile crystal modification were weighed to attain a 1:1 molar $MgCO_3$:TiO_2. Mechanical activation of the starting mixture was performed by high energy ball milling using ZrO balls and vessels with ball to powder mass ratio 40:1. The observed grinding times were 15, 30, 60 and 120 minutes. The isothermal sintering of compacted powders was conducted at 1100ºC during 30, 60 and 180 minutes. For specimens synthesized in such a manner, microwave dielectric properties were measured, quality factor Q and the dielectric constant (ε_r) in function of frequency. The measurements of electrical resistivity, capacitance and loss tangent of samples were measured in the frequency range from 500 Hz to 5 MHz frequencies with a HIOKI 3532-50 LCR HiTESTER device at a constant voltage mode (amplitude 0.5 V of sinusoidal signal applied to the specimens).

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I. Introduction

Ceramic materials with functional electric properties hold an important place among new materials. These materials are obtained by sintering through particle interaction during heating of a dispersive mixture of crystal and non-crystal materials. Qualitative and quantitative changes occur at powder particle contacts. Ceramic materials thus attain certain mechanical and electrical properties as a consequence of physical-chemical, structural and microstructural transformations of the material. Rapid development of electronics is lately linked with development and improvement of new components based on titanate, stannate and zirconate ceramics. These ceramic systems belong to the perovskite group of materials. The subject of research in this paper is the MgO-TiO_2 system, i.e. magnesium-titanate ($MgTiO_3$).

Modern technologies most often prepare powders for the synthesis of new materials applying mechanical activation – intensive transfer of mechanical energy to powder in specially constructed mechanic activators. Mechanical activation leads to controlled reduction of order and material destruction. As the reaction capability of a material is the consequence of structural properties, reduction of order and destruction in a material occurring during mechanical activation of the powder later causes acceleration of the synthesis process and sintering of a material using activated powder [1]. Besides increasing powder reaction capability mechanical activation can also achieve phase structural transformation.

The market for electronic devices requires faster development and application of new materials with defined properties. Rapid development of electronics has lately depended on development and advancement of new components based on titanate ceramics. Magnesium titanate ($MgTiO_3$) is a basic dielectric material used for the production of type-I condensers [2]. Magnesium titanate is widely applied in industry [3, 4, 5]. Due to its good electric properties magnesium titanate has lately been widely applied in microwave frequency resonators and filter and oscillator antennae for application in communication systems and GPS devices [6].

The dielectric characteristics required for microwave resonator are high dielectric constant (ε_r) to reduce the size of resonators and high quality factor (Q) for achieving prominent frequency selectivity and stability [7]. Moreover, low-sintering temperature is also required to match with low-loss and low-melting point conductors in fabrication of dielectric devices [8]. There are several methods used for reducing sintering temperature of dielectric ceramics such as addition of a low-softening glass or liquid phase sintering aid, chemical pre-treatment and processing of precursor ceramic powders and reduction of particle sizes of starting materials. $MgCO_3$-TiO_2 (hereafter referred to as MT) ceramics is well known as the material for temperature compensating capacitor and dielectric resonator. However, it required sintering temperatures as high as 1300ºC.

a) Experimental

Samples were prepared by conventional solid-state ceramic processing using $MgCO_3$ (99.9% p.a.) and TiO_2 (99.9% p.a.) as the starting materials. Appropriate amounts of the compositional constituents, those correspondents to the demanded stoichiometric ratio 1:1 were weight out. The powders were submitted to mechanochemical treatment, in a planetary ball mill

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device (Fritsch Pulverisette 5), with zirconium oxide balls (approx. 10 mm in diameter) and the ball to powder mixture mass ratio was 40:1. The time of milling was varied from 15 to 120 min and mixtures, as appropriate samples, were denoted according to the applied time of activation as MT-00, MT-15, MT-30, MT-60 and MT-120. Powders were then sieved through a 0.2 mm sieve.

The binder-free powders were compacted at 400 MPa pressure using the uniaxial double action pressing process in an 8 mm diameter tool (Hydraulic press RING, P-14, VEB THURINGER). Compacts were places in an alumna boat and heated in tube furnace (Lenton Thermal Design Typ 1600). The heating rate was 10°C/min and when the temperature of the furnace reached 1100°C, compacts were sintered isothermally in air atmosphere for 180 min. The density of specimens was calculated from precise measurements of specimen's diameter, thickness and mass.

The relative shrinkage of samples in order to investigate the reactive sintering process was followed by a sensitive dilatometer Bähr Gerätebau GmbH Type 702s. Heating was carried out in air with a constant heating rate of 20°C/min, from room temperature to 1000°C.

X-ray powder diffraction patterns of the milled powder mixtures, as well as sintered samples, were obtained using a Philips-Analitical PW-1710 diffractometer, with a CuK_α radiation and a step scan mode of 0.02°/2 s.

Scanning electron microscopy was used to record starting powders MT-00, MT-15, MT-30, MT-60 and MT-120 on a JSM-6460 LV JEOL device with INCA x-sight Oxford analysis EDS analysis.

The measurements of electrical resistivity, capacitance and loss tangent of samples were measured in the frequency range from 500 Hz to 5 MHz frequencies with a HIOKI 3532-50 LCR HiTESTER device at a constant voltage mode (amplitude 0.5 V of sinusoidal signal applied to the specimens). The "four-probe" configuration has been employed. The samples were prepared by painting silver electrodes on both sides following with thermal treatment at 120°C for 2 h performed in order to improve the paint conductivity.

II. Results and Discussion

Research and analysis of dielectric ceramics has been done for some time so new research is essentially focused on analyzing fine interactions in the synthesis-structure-properties relationship. As in this research the starting components have been greatly influenced (mechanical activation of the powder mixture has a significant influence on the structure of components reacting during the sintering process) it is of great significance to establish the influence of synthesis and structure of the electronic ceramics on functional properties of the electronic components. In this work special attention has been paid to the influence of mechanical activation of 120 minutes on the structure and properties of sintered magnesium titanate. The sintering time was varied from 0 to 180 minutes. In this work special attention has been paid to the influence of mechanical activation and sintering time concerning to electrical properties meassured via different frequencies.

According to our X-ray analysis [9], intensive milling of $MgCO_3$-TiO_2 powder mixture leads to the decrease of crystallinity, occurring as a consequence of defect formation and diminution of crystallite size. The diffractograms obtained after 15 and 30 min of activation, show that the decomposition of $MgCO_3$ takes place along with the simultaneous formation of $MgTiO_3$ phase, occurring as a consequence of a solid-state reaction between MgO and TiO_2.

We have noticed that: intensities of all starting phases are significantly lowered after 15 min of mechanical treatment, the first significant appearance of a new magnesium-titanate phase along with all the starting phases is established to be after 30 min of mechanical treatment. Microstructure parameters revealed from an approximation method [10] of ball-milled $MgCO_3$-TiO_2 powder mixture: particle size (D_{hkl}), density of dislocations (ρ_D) and lattice strain (e_{hkl}) are presented in Figure 1. After sintering, a magnesium-titanate ($MgTiO_3$) phase along with small amounts of unreacted TiO_2 [5] phase is observed, Figure 2. Also, phase identification has been done using JCPDS cards 01-079-0831 and 01-074-1940 for magnesium-titanate and titan-dioxide, respectively.

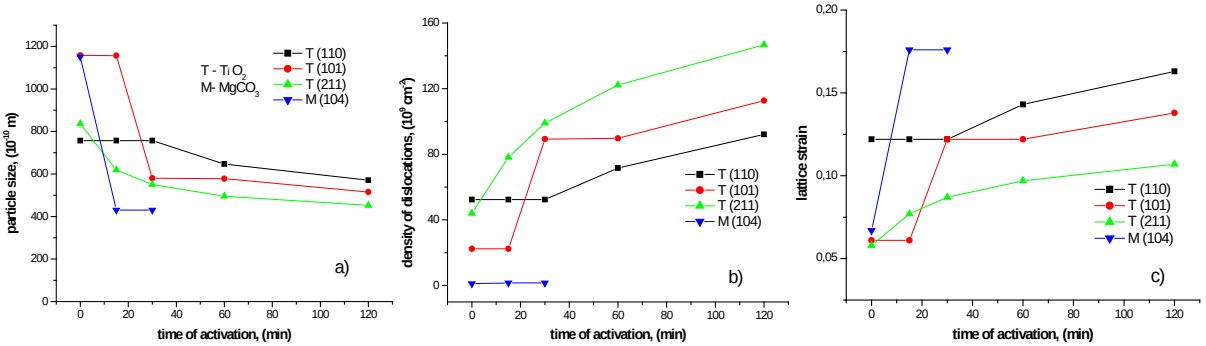

Figure 1 : Microstructure parameters: particle size, (b) density of dislocations and (c) lattice strain as a function of activation time

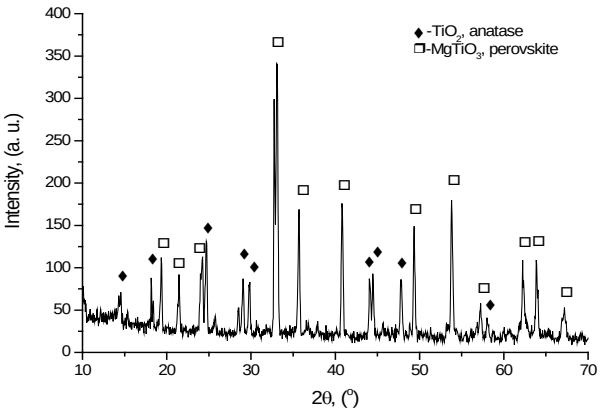

Figure 2 : XRD pattern of sample activated 120 min and sintered 3 h at 1100°C

Dilatometric analysis, given on figure 1, confirms the results obtained by X ray difractometry and thermal analysis [9]. The non-activated mixture shows dimension fluctuations at about 400°C corresponding with mass loss, confirmed with DTA analysis, that originate from carbon dioxide release. All specimens mechanically activated did not show such curve deflection, indicating that carbon dioxide release is enhanced and causes no sudden shape changes of the specimen. During sintering the slope of dilatometric measurements indicates a phase transition at 850°C from $MgTi_2O_5$ to Mg_2TiO_4 [11].

Increased milling time to 120 minutes, as confirmed by SEM micrographs, Figure 3, lead to linking of most particles into solid agglomerates characterized by closed porosity that slows down the shrinkage process so the sintering process temperature increases and also the sintering time. This analysis also indicates the time required for non-isothermal sintering. Microstructural analysis has shown that mechanical activation not only increases the sintered sample density but also leads to increased neck contacts and strengthening of boundary grain zones. As a result of this, microstructures show that sample surface fractures have occurred between and over grains. According to the performed analysis the most homogenous microstructure was obtained for the sample activated for 120 minutes.

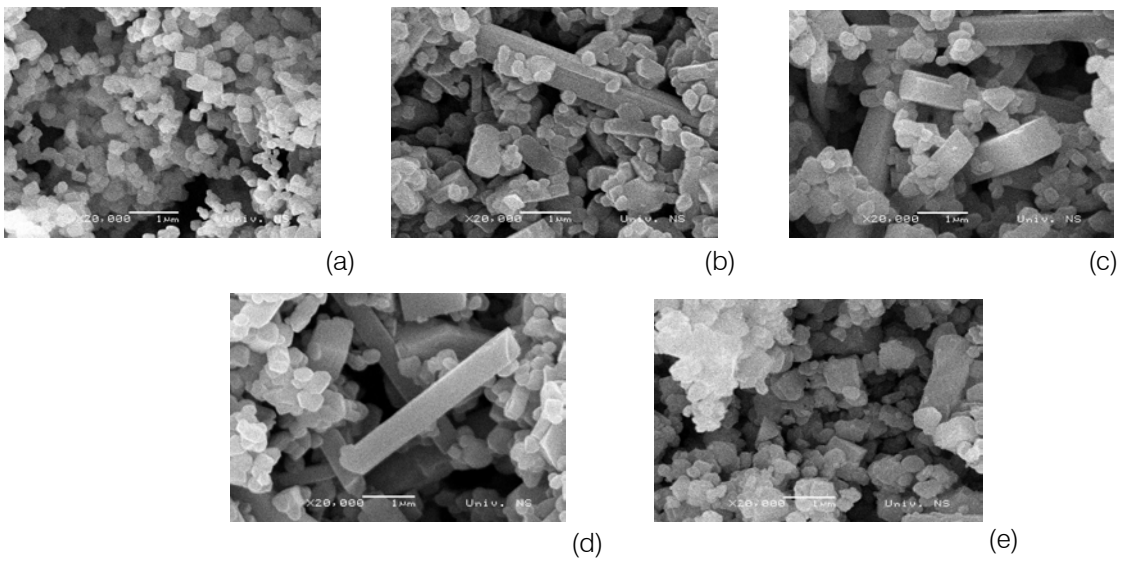

Figure 3 : SEM micrographs of samples activated (a)0,(b)15,(c)30,(d)60 and (e)120 min and sintered at 1100°C for 3 h

The most significant electric properties on which application of a dielectric material directly depends is the quality factor Q or the dielectric loss tangent angle $tg\delta$ and relative dielectric constant ε_r [11].

Variation of synthesis parameters can give a material with defined properties. Concretely, using the example of the relative dielectric constant, it is noticeable that variation of the sintering time for the same duration of mechanical activation can select a certain ε_r value.

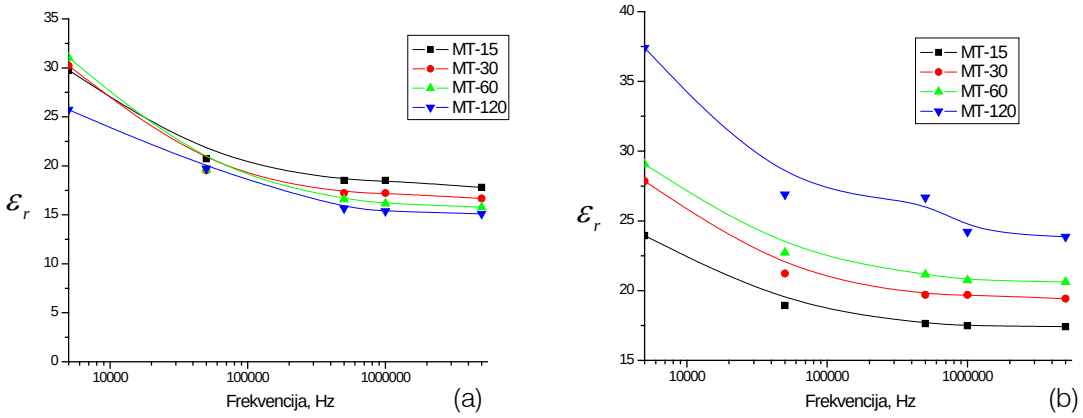

Figure 4 : ε_r as a function of frequency for samples sintered 30 minutes (a) and 60 minutes (b) at 1100°C

Measurement results show that changes in the sintering time change the polarization of constant electric dipoles in $MgTiO_3$ that has a direct influence on the value of the relative dielectric constant. The lowest ε_r value was obtained for the MT-120 sample sintered for 30 minutes, while a similar value was obtained for the MT-60 sample also sintered for 30 minutes. These results indicate if a material with a high ε_r value is desired, one should set the synthesis parameters to mechanical activation of 120 and sintering time of 60 minutes. With the increase of frequency, ε_r value decreses. Depending on requirements, variation of synthesis parameters can give predicted values for the relative dielectric constant.

The results obtained show that the quality factor increases with the increase in sintering time for activated samples. The quality factor also increases for increasing times of mechanical activation as a function of frequency. The results obtained for the quality factor show that synthesis parameters have a significant influence on electric properties of the sintered $MgTiO_3$ system. Increasing of the sintering time in combination with increasing the time of mechanical activation gives a material with a higher quality factor. With the increase of frequency, Q value increses, as well.

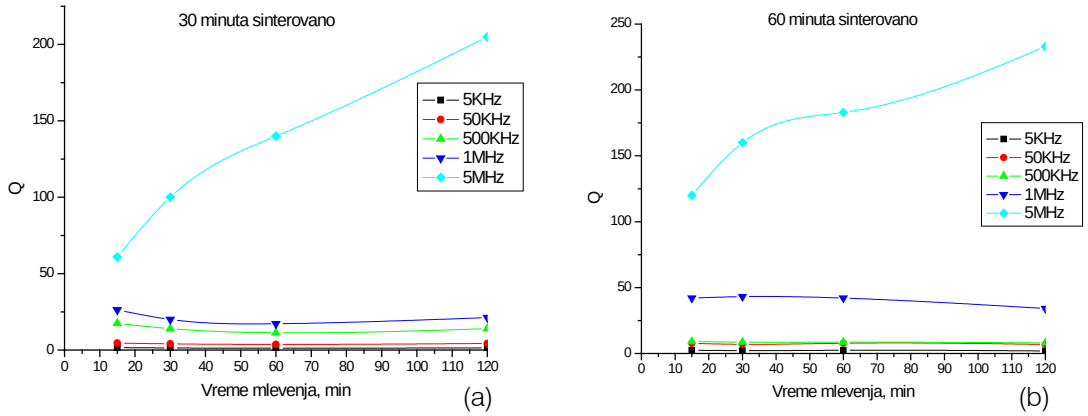

Figure 5 : Quality factor of frequency for samples sintered 30 minutes (a) and 60 minutes (b) at 1100oC

III. Conclusions

Obtaining materials with advance defined properties is the main task of new materials science. The research subject of this paper were a stady of the influence of synthesis parameters of magnesium titanate ($MgTiO_3$).

Increasing the activation time leads to lowering temperature of the reaction compared with non-

activated samples. Basic changes in the material during mechanical activation occur on physical-chemical surface parameters thus changing the materials reactivity. Reduction of the povder particle size increases its specific surface and thus its reaction capability. Grinding $MgCO_3$ and TiO_2 powders increases their reactivity and accelerates solid state reactions. All analyses show that increasing the grinding time reduces the phase formation temperature and thus shortens the sintering duration.

One of the parameters set before new materials syntheses is the time needed to obtain them and accordingly the invested energy. Optimal duration of mechanical activation leads to reduced energy consumption, and thus reduction of the sintering temperature and time. The results obtained show that the worst properties are obtained for samples that were not mechanically activated. Increasing the sintering time in combination with increasing the time of mechanical activation gives a material with an increased quality factor. Depending on requirements, variation of synthesis parameters can give desired values for the relative dielectric constant.

Based on the results obtained in this work conditions have been created for controlling the structure of magnesium titanate through synthesis parameters thus enabling obtaining of materials with advance defined electric properties that can be widely applied in the field of electronics.

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Securing Distributed FPGA System using Commutative RSA Core

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Abstract- Protecting important data is of utmost concern to the organizations or multiple transceiver based communication systems and, cryptography is one of the primary ways to do the job. RSA algorithm is extensively used in the popular implementations of Public Key Infrastructures. Many cryptographic protocols and attacks on these protocols make use of the fact that the order in which encryption is performed does not affect the result of the encryption, i.e., encryption is commutative. On the other hand, the need of a security feature encompassing data authentication among multiple MIMO or transceivers has become very critical. This paper presents the implementation of a cryptography core based on Commutative RSA public key cryptography algorithm for accomplishing data security and authentication in environment comprising multiple FPGA cores without any key exchange overheads. In spite of considering conventional two terminal communications, we have implemented a scalable architecture for multi distributed FPGA based systems and realizes commutative RSA algorithm for verifying data security among multiple transceiver terminals. In this approach, a sophisticated RSA cryptographic technique based on commutative Encryption methodology has been implemented for distributed FPGA terminals. The proposed system architecture has used the Montgomery multiplication algorithm with exponential modular multiplication and Radix-2 multiplication based multiparty cryptography.

Keywords: *authentication, cryptography, data security, FPGA, montgomery multiplication, RSA cryptosystem, Radix-2 multiplier.*

GJRE-F Classification : *FOR Code: 090699*

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R. Ambika [α], S. Ramachandran [σ] & K. R. Kashwan [ρ]

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Keywords: authentication, cryptography, data security, FPGA, montgomery multiplication, RSA cryptosystem, Radix-2 multiplier.

I. Introduction

As the telecommunication network has grown explosively and the internet has become increasingly popular, security over the network is the main concern for services like electronic commerce [1]. The fundamental security requirements include confidentiality, authentication, data integrity, and non repudiation. Cryptography plays an important role in the security of data. It enables us to store sensitive information or transmit it across insecure networks so that unauthorized persons cannot read it. The urgency for secure exchange of digital data resulted in large quantities of different encryption algorithms which can be classified into two groups: symmetric key algorithms (with private key algorithms) and asymmetric key algorithms (with public key algorithms) [2]. Many systems utilize public-key cryptography to provide such security services, and the algorithms developed by Rivest, Shamir, and Adleman (RSA) [3] is one of the most widely adopted public key algorithms at present. Since, RSA is considered as an efficient and optimized solution for public-key cryptography, we have implemented the Commutative RSA (CRSA) approach for authenticating data communication between Multiple Input Multiple Output (MIMO) or transceiver systems. In most of the existing data authentication or security systems, the authentication is accomplished by key exchange approach and thus it increases the key exchange overheads. On the other hand at every terminal, encryption and decryption process is required and thus if general RSA approach is applied in that case the data authentication and security could be violated. Therefore, in order to accomplish the goal of data security with individual encryption/decryption without affecting the data security and its integrity, a modified RSA has been developed and this mechanism is termed as Commutative RSA (CRSA).

RSA is the most widely used public-key cryptosystem. An RSA operation is an exponentiation, which requires repeated multiplications. The Montgomery multiplication algorithm [4] is the most efficient multiplication algorithm available. It replaces trial division by the modulus with a series of additions and divisions by a power of two. Thus, it is well suited to hardware implementation and forms the basis of many of the currently reported RSA hardware architectures [5–7]. To date, several techniques have been proposed in order to avoid carry propagation during the addition stages of the computation, as this is a key factor in determining performance. One approach proposed by Elbirt and Paar [6] is to break these additions into x-bit stages, where x is an optimal bit length chosen to take advantage of the fast carry chains available on modern FPGAs. However, a drawback of this approach is that the circuits developed can be very heavily technology

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and implementation dependent. For example, it is unlikely that a design created in this manner for a specific FPGA family will show the same speed advantages if migrated to a modern ASIC technology or, indeed, an alternative type of FPGA or Programmable Logic Device (PLD). An alternative approach presented by Blum and Paar [7] is based on the use of FPGA systolic array multiplier architectures with varying processing element sizes, namely, 4, 8 and 16 bits. However, these systems are again tailored specifically for the XilinxFPGA series.

As the operands such as the plain text of a message or the cipher or possibly a partially ciphered text are usually large and, in order to improve time requirements of the encryption/decryption operations, it is essential to attempt to minimize the number of multiplications performed and to reduce the time requirement of a single multiplication. There are various algorithms that implement multiplication. But considering the versatility and robustness of Montgomery multiplication approach, we have used Montgomery Multiplication algorithm. The most attractive feature of Montgomery algorithm is that it computes multiplications without trial divisions.

The RSA algorithm and Diffie-Hellman key exchange scheme need exponentiation, which binary or m-ary methods can break into a series of multiplications. It is effectively accomplished by Montgomery multiplication algorithm. Montgomery algorithm speeds up the multiplications and squaring required for exponentiation. The efficient implementation of this long-word length multiplication is crucial for the performance of public-key cryptography like our proposed CRSA. Exponentiation with a large modulus, which is usually accomplished by repeated multiplications, has been widely used in public key cryptosystems for secured data communications. To speed up the computation, the Montgomery multiplication algorithm is used to relax the process of quotient determination and, the carry-save addition (CSA) is employed to reduce the critical path delay. Basically, the exponentiation with a large modulus is usually accomplished by performing repeated multiplications, which is considerably time-consuming. As a result, the throughput rate of RSA cryptosystem will be entirely dependent on the speed of multiplication and the number of performed multiplications. One way to achieve this is to use carry save adders (CSAs) to perform the addition stages of Montgomery's algorithm. For example, Kim et al. [8] used two levels of carry save logic (CSL) and a 32-bit carry propagate adder along with a 32 x 32-bit shift register in order to perform the 1024-bit additions required. Bunimov et al. [9] improved this by replacing one level of CSL with a look-up table.

In order to accomplish the goal of data security and authentication among multiple MIMO or transceiver terminals with proposed Commutative RSA cryptographic algorithm, we have implemented an enhanced and optimized noble data authentication architecture called Commutative RSA algorithm with multiple MIMO or transceiver systems, and simulated on FPGA devices. In this approach, three FPGA cores have been considered in simulation framework and simulation for RSA encryption and decryption has been accomplished at every considered terminal. The developed architecture encompasses the Montgomery modular multiplication approach to speed up the computation and to relax the process of quotient determination and similarly the carry-save addition has been employed to reduce the critical path delay. The proposed multiplier is able to work with any precision of the input operands, limited only by memory or control constraints. In order to make the system compatible with Very Large Scale Integration and to get optimized performance, the system architecture has been developed with Montgomery multiplication with Radix-2 multiplier based architecture. We have implemented two different CRSA implementation architectures. One is Serial Montgomery implementation and another one represents Parallel Montgomery based CRSA core. The performance for both architectures for delay, frequency, efficiency, power consumption as well as throughput have been calculated and we have found that the proposed Parallel Montgomery (PM) based CRSA performs far better than serial Montgomery (SM) based CRSA core.

The remaining paper has been divided into the following sections. Section 2 discusses in brief the literature survey conducted for the research work with emphasis on RSA algorithm and implementation of Montgomery multiplication with Radix-2 architecture. Section 3 discusses the proposed Commutative RSA algorithm and presents the mathematical derivation for CRSA approach. Section 4 represents the proposed commutative RSA core based on serial Montgomery and parallel Montgomery multipliers. The hardware implementation has been presented in Section 5 followed by Section 6 that presents the results and analysis of the research work. The conclusion has been given in the last section.

II. Related Works

Gustavo D. Sutter et. al [10] optimized the Montgomery's multiplication and proposed architectures to perform the least significant bit first and the most significant bit first algorithms. The developed architecture has the following distinctive characteristics: 1) use of digit serial approach for Montgomery multiplication. 2) Conversion of the CSA representation of intermediate multiplication using carry–skip addition. This allows the critical path to be reduced, albeit with a small-area speed penalty; and 3) recomputed the quotient value in Montgomery's iteration in order to

speed up the operating frequency. In this paper, researchers presented results in Xilinx Vertex 5 and in 0.18-µm application-specified integrated circuit technologies.

Jin-Hua and Cheng-Wen [11] proposed a radix-4 modular multiplication algorithm based on Montgomery's algorithm, and a fast radix-4 modular exponentiation algorithm for RSA public-key cryptosystem. The proposed multiplier is four-times faster than a direct radix-2 implementation of Montgomery's algorithm. Extending the design for a larger modulus is straightforward. High-radix bit-level and digit-level modular multipliers have also been discussed.

C. McIvor et.al [12] presented Modified Montgomery multiplication and associated RSA modular exponentiation algorithms and circuit architectures. Practical approach presented is based on a reformulation of the solution to modular multiplication within the context of RSA exponentiation.

Alexandre F. Tenca and C¸ etin K. Koc [13] presented a scalable architecture for the computation of modular multiplication based on the Montgomery multiplication algorithm. A word-based version of is presented and used to explain the main concepts in the hardware design. The proposed multiplier is able to work with any precision of the input operands, limited only by memory or control constraints.

Marcelo E. and Naofumi Takagi [14] proposed a mixed radix-4/2 algorithm for modular multiplication/division for a large modulus suitable for VLSI implementation. The calculation of modular multiplication is based on the Montgomery multiplication algorithm and the modular division on the extended Binary GCD algorithm. The researchers exploit these similarities to modify the algorithms in order to share almost all hardware components for both operations.

Koç, C.K., et.al [15] studied the operations involved in computing the Montgomery product and describe several high-speed, space-efficient algorithms for computing MonPro (a, b), and analyzed their time and space requirements. Their focus is to collect several alternatives for Montgomery multiplication, three of which are new. However, the researchers do not compare the Montgomery techniques to other modular multiplication approaches.

Ching-Chao Yang et. al [16] proposed a new algorithm based on Montgomery's algorithm to calculate modular multiplication that is the core arithmetic operation in an RSA cryptosystem. The modified algorithm eliminates over-large residue and has very short critical path delay that yields a very high-speed processing. The researchers have implemented a 512-bit single-chip RSA processor based on the modified algorithm with Compass 0.6-μm SPDM CMOS cell library.

Along with the strong momentum of shifting from single-core to multicore systems, Zhimin Chen et. al [17] present a parallel-software implementation of the Montgomery multiplication for multicore systems. Their comprehensive analysis shows that the proposed scheme, pSHS, partitions the task in a balanced way so that each core has the same amount of job to do. In addition, we also comprehensively analyze the impact of inter-core communication overhead on the performance of pSHS. The analysis reveals that pSHS is high performance, scalable over different number of cores, and stable when the communication latency changes.

GuilhermePerin et. al [18] described a comparison of two Montgomery modular multiplication architectures: a systolic and a multiplexed. Both implementations target FPGA devices. The modular multiplication is employed in modular exponentiation processes, which are the most important operations of some public-key cryptographic algorithms, including the most popular of them, the RSA. The proposed systolic architecture presents a high-radix implementation with a one-dimensional array of Processing Elements.

The RSA algorithm proposed by P. Fournaris and O. Koufopavlou [19] has gained wide acceptability and has been well used algorithm in many security applications. Its main mathematical function is demanding in terms of speed, operation of modular exponentiation. In this article, a systolic, scalable, redundant carry-save modular multiplier and RSA encryption architecture are proposed using the Montgomery modular multiplication algorithm.

Perovic, N. S. et. al [23] presented FPGA implementation of RSA algorithm, where a key is 1024 bits long and the project synthesis results like resource occupancy, maximal operating frequency, etc. were examined for the system implementation.

III. Proposed System

Highly robust and optimized system architecture for implementation of $\boldsymbol{Commutative\ RSA}$ algorithm for data authentication among multiple MIMO terminals (here simulated on FPGA devices) has been proposed in this paper. In order to facilitate the secure data communication among multiple MIMO or transceiver systems, a noble commutative RSA approach that states that, the order in which encryption is performed does not affect the result of the encryption, has been implemented and simulated on multiple FPGA devices. In order to optimize the performance of the system with minimum space and higher speed, the robust Montgomery modular multiplication mechanism has been adopted with $\boldsymbol{Radix-2}$ multiplication architecture. We have proposed the implementation of Serial Montgomery as well as Parallel Montgomery based CRSA cryptography core, with a goal to enhance the system performance for its less memory occupancy, fast rate, higher throughput and less power consumption.

a) Commutative RSA

A secure plane is realizable provided the data communicated over the plane is protected and cannot be colluded. The use of cryptographic techniques is generally preferred, hence the *Secure Multi FPGA Communication Protocol* (*SMFCP*) proposed in this paper adopts the commutative RSA algorithm. The *SMFCP* considers two prime numbers $Param\_P_p^{CRSA}$ and $Param\_Q_q^{CRSA}$ initialized amongst all the group members. G_A Let and G_B represent the group members required to communicate over the secure plane. To compute the encryption keys and decryption key pairs of the commutative RSA algorithm, the Property $Prop\_N^{CRSA}$ and $Prop\_\phi^{CRSA}$ are computed using the following equations:

$$Prop\_N^{CRSA} = \left[\left(Prop\_P_p^{CRSA}\right) \times \left(Prop\_Q_q^{CRSA}\right)\right] \quad (1)$$

$$Porp\_\phi^{CRSA} = \left[\left(Prop\_P_p^{CRSA} - 1\right) \times \left(Prop\_Q_q^{CRSA} - 1\right)\right] \quad (2)$$

From the above equations, it is clear that

$$Param\_N_A{}^{CRSA} = Param\_N_B{}^{CRSA} \quad (3)$$

and $Porp\_\phi_A{}^{CRSA} = Prop\_\phi_B{}^{CRSA}$ for A and B (4)

The encryption key pair of A and B represented as

$$(Prop\_N_A{}^{CRSA}, Porp\_E_A{}^{CRSA}) \text{ and } (Prop\_N_B{}^{CRSA}, Prop\_E_B{}^{CRSA})$$

are to be obtained. The $Param\_E^{CRSA}$ is obtained by randomly selecting numbers such that it is a co prime of $Prop\_\phi^{CRSA}$ or in other terms:

$$\mathcal{FN}_{GCD}(Prop\_E^{CRSA}, Prop\_\phi^{CRSA}) = 1 \quad (5)$$

where $\mathcal{FN}_{GCD}(x, y)$ represents the greatest common divisor function between two variables x and y.

The decryption key pair of A and B is represented by $(Prop\_N_A{}^{CRSA}, Prop\_D_A{}^{CRSA})$ and $(Prop\_N_B{}^{CRSA}, Prop\_D_B{}^{CRSA})$ and the Property $Prop\_D^{CRSA}$ is computed based on the following equation:

$$Prop\_D^{CRSA} = (Prop\_E^{CRSA})^{-1} Mod(Prop\_N^{CRSA}) \quad (6)$$

Let Enc_X represent the encrypted data X. The encryption operation is defined as follows:

$$Enc_X = Y^{Prop\_E^{CRSA}} Mod(Prop\_N^{CRSA}) \quad (7)$$

The commutative RSA decryption operation on the encrypted data $\mathbb{B}$ is defined as

$$Dec_Y = Y^{Prop\_D^{CRSA}} Mod(Prop\_N^{CRSA}) \quad (8)$$

b) Commutative property of RSA Algorithm

The commutative property of the RSA algorithm adopted in SMFCP can be proved if data X encrypted by A and then encrypted by B provides the same resultant if the encryption is performed by B followed by the encryption performed by A, i.e.,

$$\mathrm{Enc^B(Enc_x{}^A)} \equiv \mathrm{Enc^A(Enc_x{}^B)} \quad (9)$$

$$\mathrm{Enc^B}\left(\mathrm{X^{Prop\_E_A{}^{CRSA}}\ Mod(Prop\_N_A{}^{CRSA})}\right) \equiv \mathrm{Enc^A}\left(\mathrm{X^{Prop\_E_B{}^{CRSA}}\ Mod(Prop\_N_B{}^{CRSA})}\right) \quad (10)$$

$$\mathrm{X^{\left(Prop\_E_A{}^{CRSA} \times Prop\_E_B{}^{CRSA}\right)}\ Mod\left(Prop_{N_A}{}^{CRSA}\right) = X^{\left(Prop\_E_B{}^{CRSA} \times Prop\_E_A{}^{CRSA}\right)}\ Mod(Prop\_N_B{}^{CRSA})} \quad (11)$$

As $\mathrm{Prop_{N_A}{}^{CRSA} = Prop\_N_B{}^{CRSA}}$ it can be concluded that

$$\mathrm{X^{\left(Prop\_E_A{}^{CRSA} \times Prop\_E_B{}^{CRSA}\right)}\ Mod\left(Prop_{N_A}{}^{CRSA}\right) = X^{\left(Prop\_E_B{}^{CRSA} \times Prop\_E_A{}^{CRSA}\right)}\ Mod(Prop\_N_A{}^{CRSA})} \quad (12)$$

And hence $\mathrm{Enc^B(Enc_X{}^A) \equiv Enc^A(Enc_X{}^B)}$ (13)

IV. Proposed Commutative RSA Core Based on Serial Montgomery and Parallel Montgomery

The dominant goal of this research work is to implement and illustrate the efficiency and robustness of commutative RSA cryptography approach for multiple MIMO or transceiver systems and for this purpose, we have implemented Commutative RSA cryptography core among multiple FPGA devices. In order to optimize the performance as well as memory occupancy, highly effective system architectures like Montgomery modular multiplication based on Radix-2 has been developed. Such implementation causes the reduction in memory occupancy as well as the speed is also enhanced many folds. These implemented approaches have been discussed in the following sections.

a) Montgomery Algorithm

Montgomery multiplication [20] is an efficient method for modular multiplication with an arbitrary modulus, particularly suitable for implementation on general-purpose computers and embedded micro-processors. The method is based on a representation of the residue class modulo M. The algorithm uses simple divisions by a power of two instead of divisions by M, which are used in a conventional modular operation. The Montgomery multiplication (MM) is the basic operation used in modular exponentiation, which is required in the Diffie-Hellman and RSA public-key cryptosystems.

Montgomery's modular multiplication algorithm employs only simple additions, subtractions, and shift operations to avoid trial division, a critical and time-consuming operation in conventional modular multiplication. The price paid is the need to convert operands into and out of Montgomery's domain, which is almost negligible in some particular applications such as cryptosystems.

Montgomery modular multiplication is one of the fundamental operations used in cryptographic algorithms, such as RSA and Elliptic Curve Cryptosystems. The Multiple-Word Radix-2 Montgomery Multiplication algorithm represents a now-classic architecture for implementing Montgomery multiplication in hardware. With properties optimized for minimum latency, this architecture performs a single Montgomery multiplication in approximately 2n clock cycles, where "n" is the size of operands in bits.

In many cryptosystems, such as RSA, computing M is a crucial operation. The reduction of M is a more time-consuming step than the multiplication A . B without reduction. Montgomery introduced a method for calculating products $(\mathrm{mod\ M})$ without the costly reduction $(\mathrm{mod\ M})$, since then known as Montgomery multiplication. M is assumed to be an odd integer. Montgomery multiplication of A and B $(\mathrm{mod\ M})$, denoted by $\mathrm{MP(A, B, M)}$ is defined as $\mathrm{A\,.\,B.}\,2^n\,(\mathrm{mod\ M})$ for some fixed integer n. Since Montgomery multiplication is not an ordinary multiplication, there is a conversion process between the ordinary domain (with ordinary multi-plication) and the Montgomery domain. The conversion between the ordinary domain and the Montgomery domain is given by the relation $\mathrm{A} \leftrightarrow \mathrm{A}'$ where $A' = \mathrm{A.}\,2^n(\mathrm{Mod\ M})$.

Mathematically, it can be written as:

$$\mathrm{MP}(A', \mathrm{B}', \mathrm{M}) = \mathrm{A}'.\mathrm{B}'.2^{-\mathrm{n}} = (\mathrm{A}.2^n).(\mathrm{B}.2^n).2^{-\mathrm{n}} = \mathrm{A.B.}\,2^n = (\mathrm{A.B})'(\mathrm{mod\ M}). \quad (14)$$

The conversion between each domain can be done using the same Montgomery operation, in particular $\mathrm{A}' = \mathrm{MP}(\mathrm{A}, 2^{2\mathrm{n}}\,(\mathrm{mod\ M}), \mathrm{M})$ and $\mathrm{X} = \mathrm{MP}(\mathrm{A}', 1, \mathrm{M})$, where $2^{2n}\,(\mathrm{mod\ M})$ can be precomputed. Despite the initial conversion cost, we achieve an advantage over ordinary multiplication if we do many Montgomery multiplications followed by an inverse conversion at the end, which is the case, for example, in our proposed RSA.

b) Radix-2 Modular Multiplier

The optimized algorithm for Radix-2 Modular multiplier for Montgomery multiplication is given as follows:

$$\boldsymbol{Input}: Odd\ M, n = \lfloor log_2 M \rfloor + 1, \quad (15)$$

$$A = \textstyle\sum_{i=0}^{n-1} a_i\,.\,2^i, with\ 0 \le A, B < M \quad (16)$$

$$\boldsymbol{Output}: \boldsymbol{C} = MP(A, B, M) \equiv A.B.2^{-n}(mod\ M), 0 \le C < M \quad (17)$$

$$1.1\ \mathrm{X}[0] = 0; \quad (18)$$

$$1.2\ For\ \ i = 0\ to\ n-1\ \ \boldsymbol{do};$$

$$1.3 \begin{cases} q_{\ i} = (a_i.b_0) \oplus \mathrm{X}[i] o; \\ \mathrm{X}[i+1] = \frac{X[i] + a_i.b + q_{\ i}.m}{2}; \end{cases} \quad (19)$$

$$1.4\ \mathrm{X}[n] > M\ \ \textbf{then}$$

$$1.5[\mathrm{X}[n] = X[n] - M;$$

$$1.6\ \textbf{return}\ \ \boldsymbol{C} = \mathrm{X}[n] \tag{20}$$

The above mentioned algorithm represents the Pseudocode for the Radix-2 Montgomery multiplication, where we choose $n = \lfloor log_2 M \rfloor + 1$. n is the size of M in bits.

The verification of the above algorithm may be presented as follows:

Consider X[i] given as

$$\mathrm{X}[i] \equiv \frac{1}{2^i}\left(\sum_{j=0}^{i-1} a_j . 2^j\right).B(Mod\ \ M), \tag{21}$$

With X[0]=0. Then $X[n] \equiv A.B.2^{-n}(mod\ M) = MP(A,B,M).X[n]$ (22)

can be computed iteratively using the following dependence:

$$\equiv X[i+1] \equiv \frac{1}{2^{i+1}}\left(\sum_{j=0}^{i} a_j . 2^j\right).B \tag{23}$$

$$\equiv \frac{1}{2^{i+1}}\left(\sum_{j=0}^{i} a_j . 2^j + a_i . 2^i\right).B \tag{24}$$

$$\frac{1}{2}\left(\frac{1}{2^i}\left(\sum_{j=0}^{i-1} a_j . 2^j\right).B + a_i . B\right) \tag{25}$$

$$\frac{1}{2}(X[i] + a_i . B)(mod\ \ M). \tag{26}$$

Therefore, depending on the parity of $\mathrm{X}[i] + a_i.Y$, we do compute $\mathrm{X}[i+1]$ as or $X[i+1] = \frac{a[i]+a.B+M}{2}$ so as to make the numerator divisible by 2.

Since $B < M$ and $\mathrm{X}[0] = 0$, one has $0 \le X[i] < 2M$ for all $0 \le i < n$. In References [21] and [22], the result of a Montgomery multiplication is presented as $A.B.2^{-n}(mod\ M) < 2M$ when $A, B < 2M$ and $2^n > 4M$. As a result, by redefining "n" to be the smallest integer such that $2^n > 4M$, the subtraction at the end of algorithm can be avoided and the output of the multipication can be directly used as an input for the next Montgomery multiplication.

c) Modular Multiplication Algorithms

In RSA, the public encryption key is a pair of positive integers (E, N) and the private decryption key is another pair of positive integers (D, N). To encrypt a message using the key (E, N) the following structural approach have been implemented. Fig. 1 represents the Serial Montgomery multiplication, whereas the parallel Montgomery is presented in Fig. 2. It encompasses two Montgomery multipliers connected in parallel. In our research work, we have implemented $Radix-2$ Modular multiplier based multiplication architecture. A brief description of the employed algorithm is as follows:

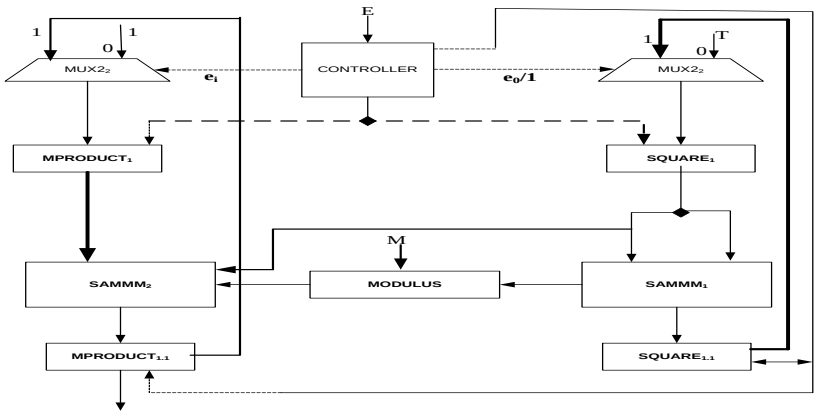

Figure 1 : Serial Montgomery Multiplication Architecture

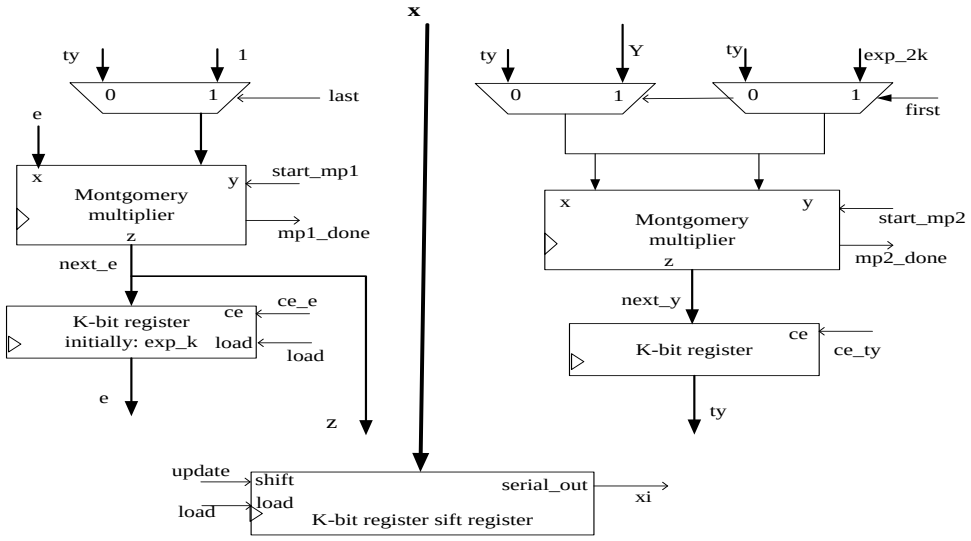

Figure 2 : Montgomery exponentiation (MSB first) with two Montgomery's multipliers in parallel

V. Hardware Design

Fig. 2 presented earlier shows the architecture of a 32-bit RSA processor based on the proposed Commutative RSA algorithm. We use four 32-bit linear shift registers to store operands needed in computing 32-bit RSA operation. The operations of the RSA processor are described in the following. In the initial stage, commutative RSA operands are loaded into shift registers serially through an input buffer. While loading message M into the text register, we shift the exponent register until the first nonzero is the most significant bit and count the number of bits of exponent $\log_2 E$. After the initial stages, we start the multiplier. Once the first output bit of the multiplier is ready, we start the Montgomery module immediately. So the execution time of CPA, multiplier, and Montgomery module is almost overlapped. Therefore, the function units of our design are fully utilized during computation.

Carry-Propagation Adder and Serial Parallel Multiplier: The carry-propagation adder converts the carry-save form of the output from the Montgomery module to non-redundant binary form. It generates one bit output per cycle to the serial-parallel multiplier for the next iteration. The serial-parallel multiplier is used to realize the multiplication and square of two n +1 bit numbers. It first generates the $n+2$ lower bits of a product serially to the Montgomery module, and then it stops and holds the n higher bit of the product. The n higher bits of the product will be added with the output of the Montgomery module to get the modular multiplication result.

The multiplier itself is a linear array type with a special input circuit. When the multiplier is generating a product of two numbers, the parallel input $M0$ is ready in the text register and another operand can arrive in serial. However, if we want to square one number, a serial input of the operand will make the multiplier fail. We solved this problem by scheduling the serial input operands and insert some zeros to avert the failure of the squaring operation.

Montgomery Module: The Montgomery module is shown in Fig. 2 and the overall operation for Montgomery modular multiplication and its functional approach has already been presented in previous sections. The variable $X[0]$ refers the n+2 lower bit of the product from the multiplier. $X[0]$ enters the Montgomery module one bit per cycle from the lower bit to the higher bit in series. The reduction step is a shift-and-add operation that is very similar to the basic step of a multiplication. The quotient determination is a parity decision on the summation of the intermediate result and the carry. This can be done simply by an exclusive-OR gate with inputs of X[i] and the LSB of the intermediate result in the previous iteration. After $n+2$ iterations, the Montgomery module will add X $[n+2]$ and the n higher bits of the product from the multiplier together. The result is then sent to the carry-propagation adder for the next modular multiplier iteration.

In this work, we have developed two CRSA cryptography cores. First model represents the Serial Montgomery multiplier based design, while the second describes the optimized Parallel Montgomery based CRSA cryptography core implementation. In parallel Montgomery approach, two Montgomery multipliers have been used in parallel.

The results obtained after implementation have been summarized in the following sections.

VI. Results

The robust commutative RSA core, whose details were presented in earlier sections, has been implemented on multiple FPGA devices for simulation and illustration of data authenticity among multiple user terminals in a communication environment. The

proposed work for the implementation of commutative RSA cryptography core has been simulated with three individual FPGA devices. The implementation of FPGA cores do signify the MIMO or multiple transceiver terminals in multiuser communication environment. The design has been coded in VHDL and has been simulated using Xilinx Design Suite 14.3 targeted on Virtex-5, xc5vlx330t-2-ff1738FPGA. In this work, two systems have been developed as mentioned earlier. One is the Serial Montgomery based Cryptography core and the second is our proposed Parallel Montgomery based cryptography core. The results obtained for both architectures have been compared. Considering the performance parameters like Memory occupancy, speed, power consumption, delay and throughput, it has been found that the Parallel Montgomery performs better than Serial Montgomery (SM) based Commutative RSA implementation. The delay in Parallel Montgomery based CRSA is 13.78% lower as compared to Serial Montgomery based CRSA cryptography core. Similarly, the throughput of Parallel Montgomery based CRSA is 12.11% higher than the serial Montgomery based CRSA architecture. Even in the proposed system, the trade-off between power consumption is also very small and it is only 0.03% higher in Parallel Montgomery based CRSA.

The simulation results for encryption and decryption obtained by the Serial Montgomery based $CRSA$ core is presented in Fig. 3 and Fig. 4 respectively. The functional verification of the Parallel Montgomery based $CRSA$ cryptographic core is shown in Fig. 5 and Fig. 6.

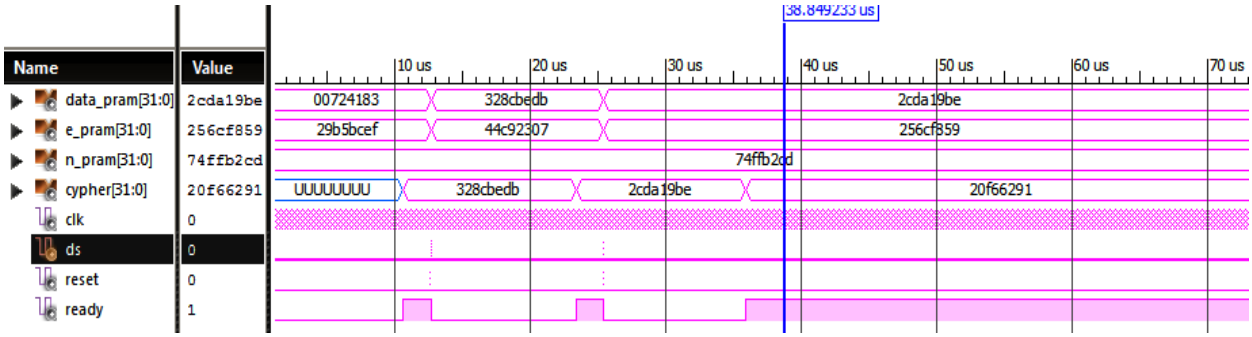

Figure 3 : Simulation Waveforms Using Serial Montgomery based : Encryption

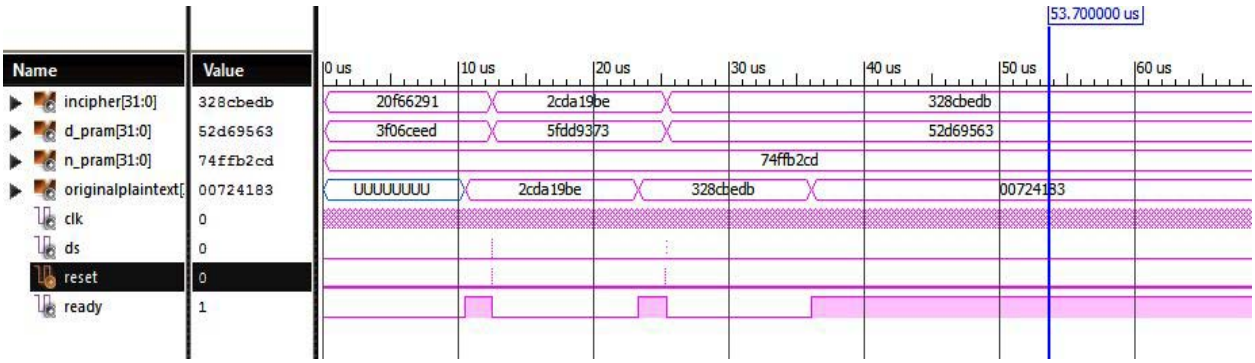

Figure 4 : Simulation Waveforms Using Serial Montgomery based : Decryption

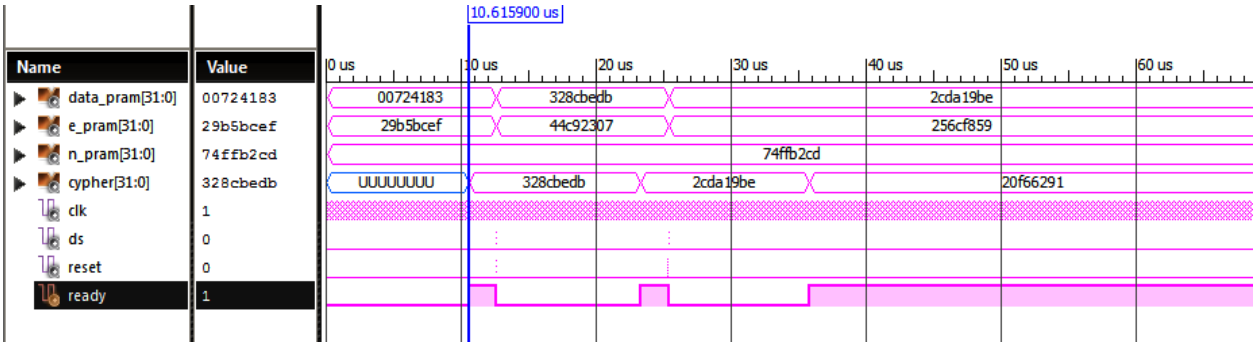

Figure 5 : Simulation Waveforms Using Parallel Montgomery based : Encryption

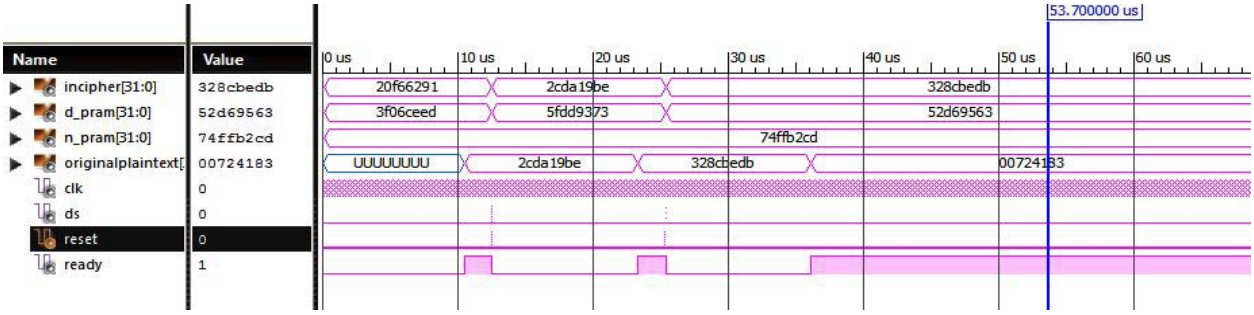

Figure 6 : Simulation Waveforms Using Parallel Montgomery based : Decryption

The results obtained for comparative simulation are presented in the following.

Table 1 : Comparison for Chip Resource Utilization in Serial and Parallel Montgomery based CRSA cryptography Core

CRYPTOGRAPHY CORE	CRSA	CRSA
CIRCUIT	SERIAL MONTGOMERY	PARALLEL MONTGOMERY
DEVICE	xc5vlx330t-2-ff1738	xc5vlx330t-2-ff1738
SLICE LUT	913	844
LUT USED AS LOGIC	913	813
OCCUPIED SLICES	290	311

Table 2 : Comparison for Power consumption in Serial and proposed Parallel Montgomery based Commutative RSA cryptography core

CRYPTOGRAPHY CORE	CRSA	CRSA
CIRCUIT	SERIAL MONTGOMERY	PARALLEL MONTGOMERY
DEVICE	xc5vlx330t-2-ff1738	xc5vlx330t-2-ff1738
STATIC POWER (mW)	3516.7	3516.75
DYNAMIC POWER (mW)	4.76	5.72
TOTAL POWER (mW)	3521.46	3522.47

Table 3 : Performance (Delay, Frequency and Throughput) Analysis for Serial and Parallel Montgomery Based CRSA Cryptography Core

CRYPTOGRAPHY CORE	CRSA	CRSA
CIRCUIT	SERIAL MONTGOMERY	PARALLEL MONTGOMERY
DEVICE	xc5vlx330t-2-ff1738	xc5vlx330t-2-ff1738
FREQUENCY (MHz)	199.57	227.08
DELAY (ns)	5.01	4.40
THROUGHPUT(kbps)	779.58	887.02

The graphical comparison for the performance of Serial and Parallel Montgomery based Commutative RSA architectures has been presented in Fig. 7 to Fig. 10.

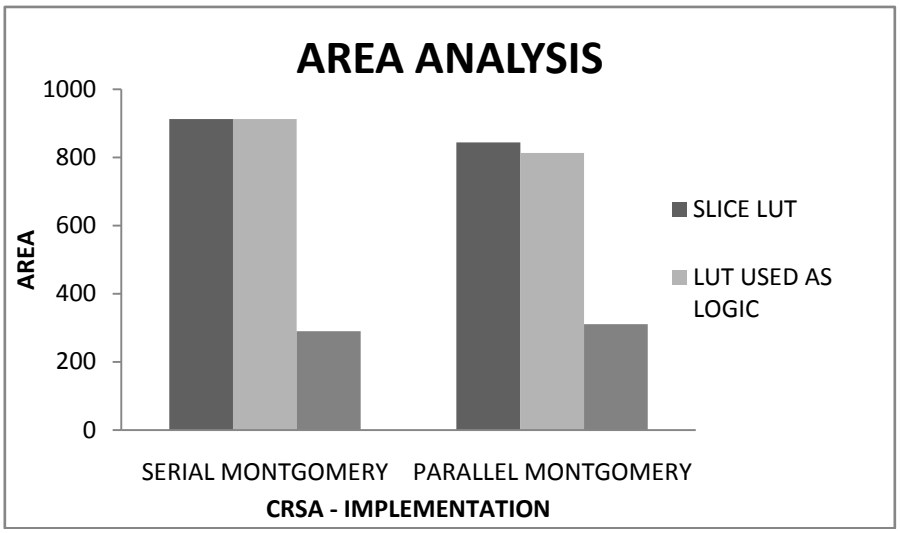

Figure 7 : Chip Resource Utilization Analysis for serial and parallel Montgomery based CRSA

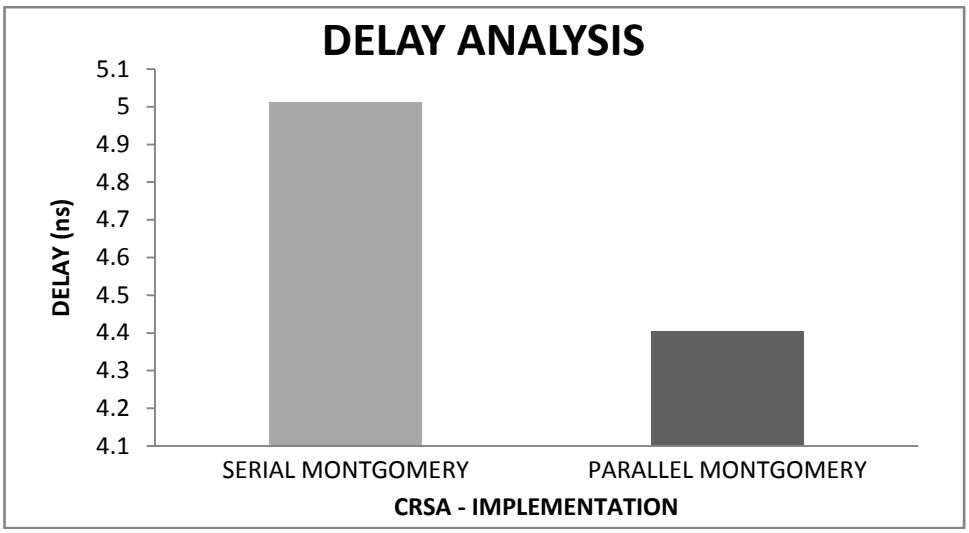

Figure 8 : Delay analysis for serial and parallel Montgomery based CRSA

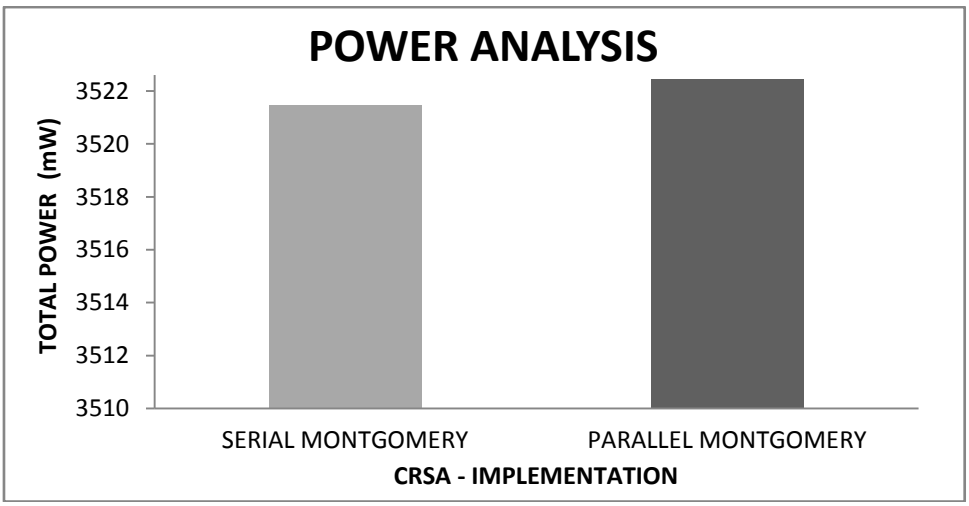

Figure 9 : Power analysis for serial and parallel Montgomery based CRSA

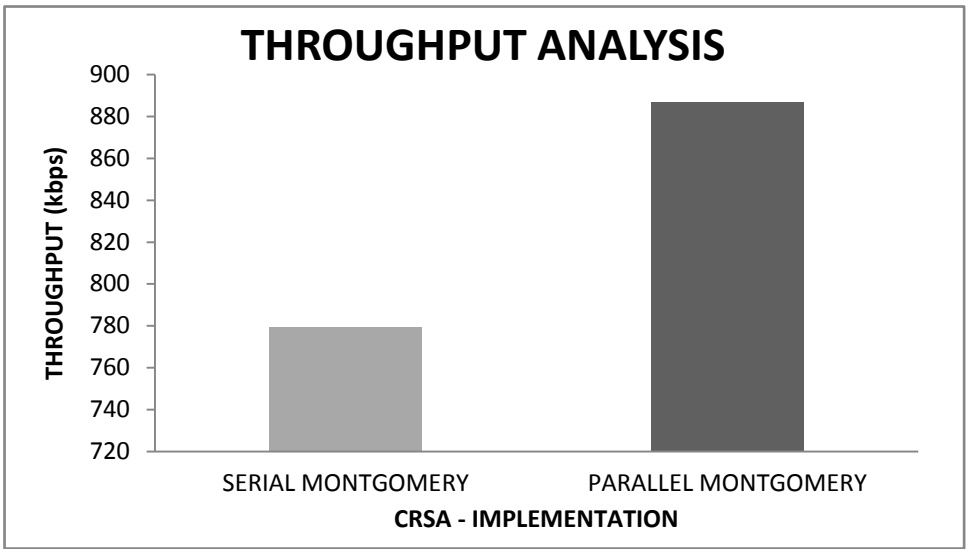

Figure 10 : Throughput analysis for serial and parallel Montgomery based CRSA

VII. Conclusion

A noble security or authentication public key cryptography technique called Commutative RSA has been implemented for multiple MIMO or transceiver terminals for accomplishing the goal of data security in multiuser communication environment. The commutative RSA approach has been implemented with multiple FPGA cores that functions as individual transceiver terminal and performs its encryption and decryption individually without affecting the original data. The two approaches based on Montgomery multiplication with Radix-2 multiplier have been designed and individual modules for Serial Montgomery (SM) and Parallel Montgomery have been simulated. The results obtained have been compared and it has been found that the proposed Parallel Montgomery (PM) architecture performs better as compared to Serial Montgomery. The proposed PM based CRSA cryptography core has exhibited 12.1% higher throughput as compared to Serial Montgomery based CRSA. Similarly, the frequency or speed of the proposed system is also higher. The proposed system exhibits trade-off of 0.03% in power consumption. Thus considering various aspects of this research work, it can be stated that the proposed Parallel Montgomery based Commutative RSA performs better than the serial based Montgomery multiplication application.

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Cognitive Radio Approach : Spectrum Sensing

By Sunil Sharma
Vinayaka Missions University, India

Abstract- In present days the wireless communication has developed quickly. This demand on wireless application has put several limitations on the existing radio spectrum which is precious and limited. Various frequency bands are not used properly in the fixed spectrum assignment but, the cognitive radio more helpful to utilize these frequency bands which are called as white spaces. This is an exclusive approach to improve use of radio electromagnetic spectrum. There are four methods to establish the cognitive radio. This report explain the first method i.e. spectrum sensing and describe the issues, techniques and challenges of this method.

GJRE-F Classification : FOR Code: 890405

Strictly as per the compliance and regulations of :

Cognitive Radio Approach : Spectrum Sensing

Sunil Sharma

Abstract- In present days the wireless communication has developed quickly. This demand on wireless application has put several limitations on the existing radio spectrum which is precious and limited. Various frequency bands are not used properly in the fixed spectrum assignment but, the cognitive radio more helpful to utilize these frequency bands which are called as white spaces. This is an exclusive approach to improve use of radio electromagnetic spectrum. There are four methods to establish the cognitive radio. This report explain the first method i.e. spectrum sensing and describe the issues, techniques and challenges of this method.

I. Introduction

The available Electromagnetic Spectrum band is becoming piled up day by day, as there is increasing demand for the requirement of wireless communication applications. Several researchers stated that the licensed spectrum is not use correctly because of static allocation spectrum. However, it is more complex to discover available bands either to develop vacant band or to set up a new service. To overcome these problems the researchers implement Dynamic Spectrum Management this improves the available spectrum utilization.

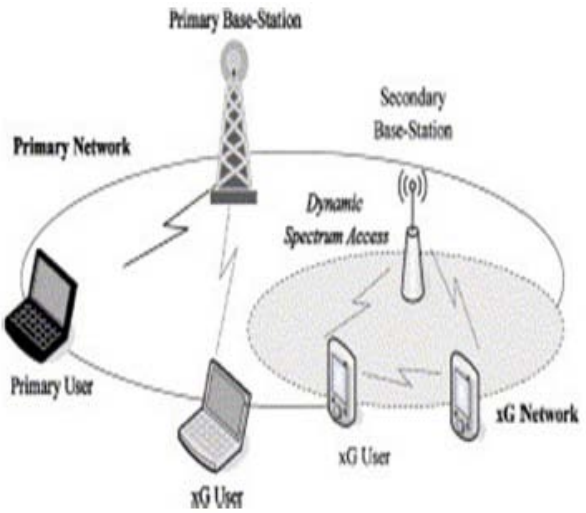

Figure 1 : Dynamic Spectrum Access

The cognitive radio works by depending on the principle of dynamic Spectrum Management which avoids the problems of utilization of spectrum in wireless communication. This radio service supplies highly reliable communication and in this communication the secondary users (unlicensed users) utilizes the unused spectrum of the primary users (licensed users). Depending on the interaction with environment this cognitive radio technology provides different transmission parameters such as networking, operating frequency, protocol and wave form etc. the below figure shows the Dynamic Spectrum Access in Cognitive Radio, Cognitive radio technology has four key functions they are:

a) Spectrum Sensing: this function recognizes the unused frequency bands and presence of licensed users i.e. Spectrum hole (white space) in those licensed bands.
b) Spectrum management: this function recognizes the time period of the unlicensed users (secondary users) can use those white spaces.
c) Spectrum Mobility: this function maintains the unbroken communication during the transition to better spectrum.
d) Spectrum Sharing: this function used to share the spectrum hole (whiter space) in between the unlicensed users (secondary users).

The radio spectrum technology should be categorized into 3 types based on the sub bands and occupancy they are:

White spaces: This type of space is free for the RF interferers but not for noise because of artificial and natural sources.

Gray spaces: This color space is partially covered with noise as well as interferers.

Black spaces: this total color space is full up due to the joint presence of interfering signals plus noise and communication.

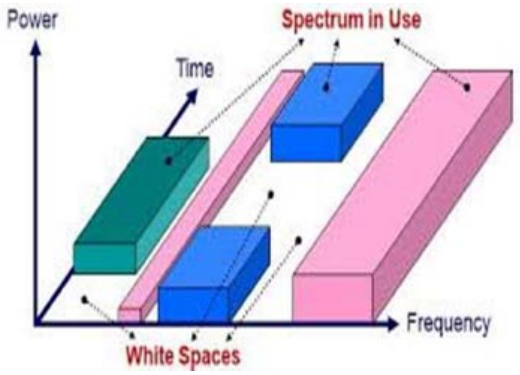

Figure 2 : White Spaces and Used Frequencies in Licensed Spectrum

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Compared to various techniques and method, Spectrum sensing is the difficult task for formation of cognitive radio based communication.

II. Spectrum Sensing

The primary aim of this cognitive radio technology is to the secondary users need to identify the presence of primary users and to depart the frequency band quickly and emerge the equivalent primary radio to avoid interference to primary users.

Spectrum sensing technique is classified into two types. They are:

Direct Techniques: this is also called as frequency domain approach. This technique estimation is complete directly from the signal approach.

Indirect Technique: this technique also called as time domain approach and this technique estimation is carried out by using autocorrelation of the signal.

Several classifications depending on the needs of spectrum sensing as discussed below:

a) Spectrum Sensing for Spectrum opportunities

Primary transmitter detection: the detection and presence of primary users performance is depending on the received signal of CR users. This detection could be done with various approaches such as energy based detection, waveform based detection, Primary Transmitter Detection, matched filter (MF) based detection, covariance based detection and cyclostationary based detection etc.

Cooperative and collaborative detection: the key signals of spectrum sensing are detected by cooperating or interacting with other users. This method can be executed as either speared the indirect approach by the external detection or spectrum load smoothing algorithm or by accessing the spectrum coordinated by spectrum server.

b) Spectrum Sensing for Interference Detection

i. Interference temperature detection: in this method the CR system uses the ultra wide band (UWB) technology. In this approach the secondary users synchronized with primary users and utilizes low transmit power and this signal or power controlled by the interference temperature level. Hence, this approach solves the problems of primary users.

ii. Primary receiver detection: in this approach the spectrum and interference opportunities are recognized by primary receiver's local oscillator leakage power.

c) The Proposed Spectrum Decision Framework

The main function of CR scenario is to spectrum sharing, spectrum access and spectrum sensing related to MAC and PHY layers. The upper protocol layer performs the operations of CR capabilities and the QOS issues, decision-making and monitoring functions could be done in the transport, application and network layer. Issariya studied and explain the CR network's performance issues of the transport layer. Chowdhury, Lee and Akyildiz defined the open research issues, various key challenges and concern performance which had appeared in the transport layers in Cognitive Radio Ad-Hoc Networks (CRAHNs).

According to Chowdhury, Lee and Akyildiz the connectivity in Cognitive Radio Ad-Hoc Networks is also spectrum dependent, which means the disconnection can be detected by spectrum handover or presence of primary users. Hence, this disconnection is detected and addressed through several innovative approaches. The main distinction of the traditional routing protocol is that the CR based routing protocol controlled the functions of primary users and its service interruption losses to establish the best routes.

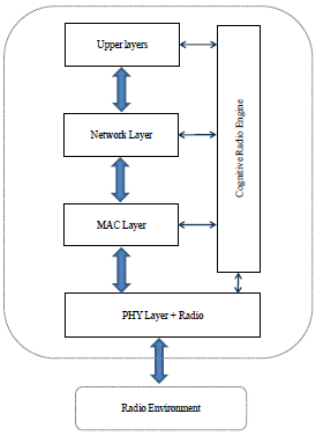

Figure 3 : Generic Cognitive Radio Architecture.

In cognitive radio networks the secondary users not have the rights to forward packets during sensing. So, the sensing function can be considered at the transport layer to avoid the pocket losses and excessive re-transmissions on the paths with each node in sensing state, particularly the interaction between MAC and transport entities and multi-hop distributed networks. Generally, the transport protocol needs to be spectrum-aware in CR scenarios and also require latest algorithms. Chowdhury, Lee and Akyildiz illustrate the TCP-based protocol for Cognitive Radio Ad-Hoc Networks and the main aim behind this approach is to address the transport layer challenges in Cognitive Radio Ad-Hoc Networks (CRAHNs).

III. Classification of Spectrum Sensing Techniques

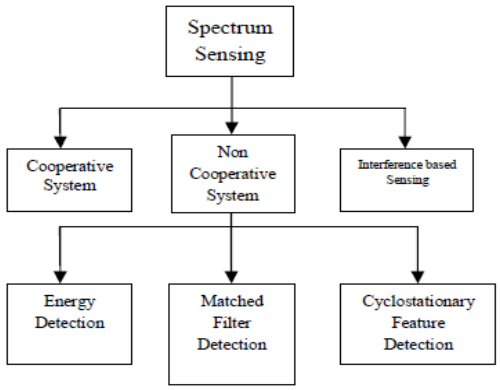

Figure 4 : Spectrum Sensing Techniques

a) Primary Transmitter Detection

This section describes the several primary transmitter detection techniques. They are

i. Energy Detection.

ii. Matched Filter.

i. *Energy Detection:* this technique not utilizes the previous information of primary signal energy.

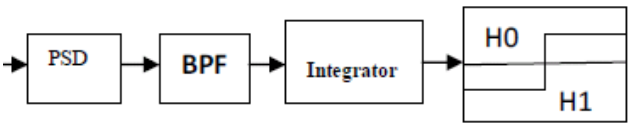

Figure 5 : Block Diagram of Energy Detection

Where H0 = Absence of User.
H1 = Presence of User.

The above figure represents the block diagram of energy detection. In this energy detection technology the signal is passed through band pass filter with W bandwidth and it is integrated over different time intervals. To detect the existence of absence of the primary user the integrator block output is compared with the predefined threshold value. This threshold value is variable or fixed this could be depends on the channel condition.

$y(k) = n(k)$..... H0

$y(k) = h * s(k) + n(k)$..... H1

Where $y(k)$ = sample to be analyzed at each instant k.

$n(k)$ = noise of variance $\sigma 2$.

The $y(k)$ allows the received samples sequence i.e. $k\epsilon\{1, 2....N\}$ at the signal detector, then a decision rule can be stated as,

H0..... if $\varepsilon > v$

H1..... if $\varepsilon < v$

Where $\varepsilon = E\,|y(k)|2$

The expected energy of the received signal and v is preferred for the noise variance i.e. denoted as $\sigma 2$. But, ED escorted by few disadvantages they are:

- ED cannot be used to discover the spread spectrum signals.
- Detection performance is subject to the precariousness of noise power.
- Sensing time taken to achieve a given probability of detection may be high.

ii. *Matched Filter*

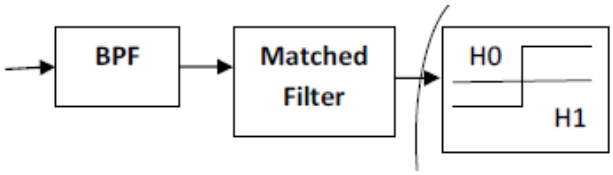

Figure 6 : Block Diagram of Matched Filter

Where H0 = Absence of User.

H1 = Presence of User.

Matched filter is also called as liner filter this could be designed to maximize the output signal to noise ratio for a given input signal. This filter detection can applied due to the secondary users has previous knowledge of primary users. The correlation is equal to function of matched filter in which the unidentified or new signal is curl with filter and the impulse response is time shifted and mirror version of a reference signal. Matched filter operation is expressed as:

$$Y[n] = \Sigma\, h[n-k]\, x[k]$$

Where 'x' = unknown signal

'h' = impulse response of matched filter

Matched filter detection process useful for the knowledge from the primary users is known to the cognitive users.

Advantages: the detection of matched filter is taking less time because it needs only O (1/SNR) samples to meet a given probability of detection constraint. However, the matched filter detection is best detection in stationary Gaussian noise because of the primary user signal is recognized to the cognitive radio user.

Disadvantages: matched filter detection process needs a previous knowledge of each primary signal. If matched filter not working properly then it gives poor information to the users. The major disadvantage of this matched filter is to every time the cognitive radio require devoted receiver for all types of primary user.

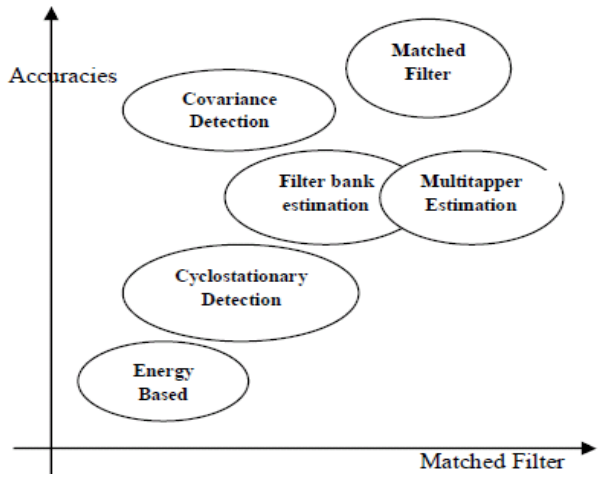

Figure 7 : Sensing accuracy and complexity of various sensing methods

b) Cooperative Techniques

Decentralized Uncoordinated Techniques: in this technique the Cognitive Radio will detects and vacate the channel independently, it could be done if the primary user find the channel without informing the other users. Compared to coordinated technique this technique don't have any disadvantages because in this technique the CR users will experience at poor channel recognition and discover the channel incorrectly thus it causing interference at the primary receiver.

Centralized Coordinated Techniques: this technique has the cognitive radio controller. This controller gives the information about the detection of cognitive radio in the presence of primary user. Therefore, by using broadcast method the controller provide the information to all cognitive radio users. This information supply procedure categorized into two types they are:

- Totally cooperative technique: in this technique nodes are helps to communicate each other's knowledge and to sensing the channel.
- Partially cooperative technique: in this technique the network nodes useful only for sensing the channel.

Decentralized Coordinated Techniques: this coordination technique strengthening the cognitive radio network without the need of controller. This technique involved several algorithms such as clustering scheme or gossiping algorithms, where cognitive users meet to clusters, auto coordinating themselves. Cooperative spectrum sensing improves the use of control channel and these channels can implement by underlying the UWB channel or detecting frequency channel.

Advantages of Cooperation: Cognitive users cooperating selflessly to sense the channel and this channel have more benefits such as channel Impairments like multipath fading, impose high sensitivity requirements inherently limited by cost and power requirements, shadowing and building penetration losses.

- *Disadvantages:* the cooperative technique has several disadvantages also like the Cognitive Radio user needs to execute sensing at periodic time intervals as sensed information become fast due to various factors like channel impairments and mobility etc.

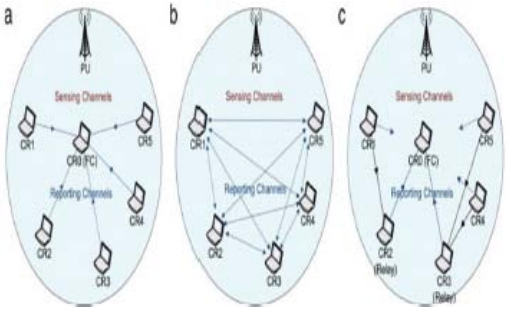

Figure 8 : a-Centralized Coordinated, b-Decentralized Coordinated and c-Decentralized Uncoordinated

Interference Based Detection: this section explains the interference based detection. In this detection method Cognitive users would operate in spectrum underlying approach.

Primary Receiver Detection: the primary receiver produces the leakage power of local oscillator through its RF front end and receiving the data from its primary transmitter. This method detects the presence of primary users by increasing low cost sensor node that is near to primary user's receiver detects the LO leakage power produces by the RF front end of the primary user's receiver which are within the communication range of CR system users. Then the local sensor intimate this sensed report to CR users. Hence, these users recognize the spectrum occupancy status and also identify the spectrum opportunities to operate CR users in spectrum overlay.

Interference Temperature Management: the major function of this Interference Temperature Management is to arrange an upper interface limit for specified frequency band in given geographic location. However, the CR users do not have the problem with interference while using the particular frequency band in particular area. The CR user transmitters manage their interference by varying their transmission power but it could be done by depending on their particular location with respect to primary users. Majorly this method focused on measuring interference at the receiver. The operating principle of this Interference Temperature Management is like an UWB technology where the CR users are permitted to synchronize and transmit synchronously with primary users. Low transmit power is controlled by the interference temperature level so as not to cause harmful interference to primary users.

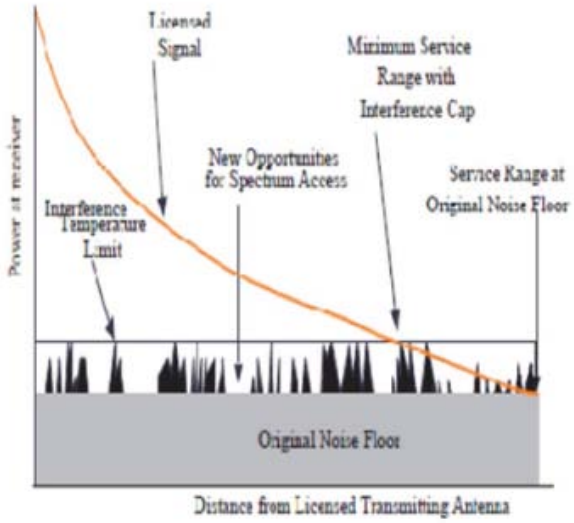

Figure 9 : Inference Temperature Model

IV. Issues in Spectrum Sensing

Channel Uncertainty: Because of fading or shading of the channel there will be uncertainties in the received signal strength which will lead to wrong interpretation. To avoid this Cognitive Radios must have high sensitivity so that he can differentiate between faded primary signal and a white space. If the fading is severe, a single cognitive radio cannot give high sensitivity so handle this we go for a set of cognitive radios which share their local measurements and collectively decide on the occupancy state of a licensed band.

Noise Uncertainty: The detection sensitivity can be defined as the minimum SNR at which the primary signal can be accurately detected by the cognitive radio and is given by

$\gamma min = PpL(D+R)$

N

Where N= Noise power.

Pp= Power Transmitted by Primary User.

D= Interference Range of Secondary User.

R= Maximum distance between Primary Transmitter and corresponding Receiver.

The noise power estimation is limited by calibration errors as well as changes in thermal noise caused by temperature variations. Since a cognitive radio may not satisfy the sensitivity requirement due to underestimate of N, γmin should be calculated with the worst case noise assumption, thereby necessitating more sensitive detector [10].

Aggregate Interference Uncertainty: If multiple Cognitive Radios are operating same in same licensed band which will lead to spectrum sensing will be affected by uncertainty in aggregate interference. Even though the primary user is out of interference range this uncertainty may lead to wrong detection so this uncertainty will create a need of more sensitive detector.

Sensing Interference Limit: There are two factors for this issue that is when an unlicensed user may not know exactly the location of the licensed receiver which is required to compute interference caused due to its transmission and the second reason is that if a licensed receiver is a passive device, the transmitter may not be aware of the receiver. So these factors need attention while calculating the sensing interference limit.

V. Conclusion

As the usage of frequency spectrum is increasing, it is becoming more valuable. So we need to access the frequency spectrum wisely. For this purpose we are using Cognitive Radio. In our paper we discussed about the most important technique that is Spectrum sensing and the issues involved in it to establish the communication using Cognitive radio. We also said about important the importance of cooperation between Secondary users to avoid interference.

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A Field Test to Estimate Efficiency of Rewound Induction Motor

By V Saravanan, P M Arumugapandi & V. Vignaraj Ananth
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Abstract- When the cost of energy increases it is important to increase the activities to reduce the energy consumption of the system up to the maximum possible limits. This proposal establishes a very low cost and time saving method to determine efficiency of induction motor at onsite for achieving above mentioned goal. Reduction in energy consumption is achieved by replacing energy efficient motor in the place of old less efficient motor. For auditing purpose pulling out the device from its working environment may cause losses in production in case of industries. On site estimations are helps To resolve such problems this paper describes an onsite method which can capable to estimate the efficiency of new as well as rewound induction motors. Motor's efficiency computed by this method closely approaches the exact value this thing makes a greater confidence to estimate the saving potential.

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Keywords: efficiency, energy audit, energy efficient motor, induction motor, onsite test.

I. Introduction

There are several techniques available to solve the problem of gap between supply and demand. One among such techniques is using energy efficient devices instead of old less efficient devices. The proposed work focus on induction motor, which is the popular prime movers, consumes a larger portion of electrical energy in industries. A one percentage improvement in efficiency reduce drastically considerable amount of power consumption (700mw national whole) in India [1]. The proposed work helps to identify the inefficient motor and replaced with an efficient one.

This action can reduces burden to power system and save the cost of power of the industries. Induction Motors are commonly used prime mover and consume 60% of total power generated. 98% of industries uses induction motors as their drive in that 90% of induction motors are squirrel cage type less than 15 kW [1]. There are good savings potential is available to take audit and technical effort for reducing energy consumption of motor without negatively affecting the products, such think makes considerable amount of reduction in power consumption in the unit. The majority of motors in the field are induction motors. There are many methods relevant to field efficiency evaluation in the literature and new methods are appearing every year. As the cost of energy is growing at a high rate, the industries can save a considerable amount of money by replacing inefficient motors with new more energy-efficient ones. In the past, many methods were used to calculate the efficiency of induction motors, one common method is to test the motor under load conditions and then monitor the input and output at different load points using a dynamometer and torque transducer [2]. This is the most straightforward method to measure the output power directly from the shaft without any need to calculate losses. Conventionally, the shaft torque method offers the most accurate field efficiency evaluation method, however, this is not suitable for the field evaluation because this process involves the removal of motor from service to place it on a test stand and couple it to the dynamometer. It can be seen that this method is impractical and costly. Another accurate method for field efficiency evaluation relies on using the no-load and blocked-rotor test results to estimate the motor equivalent circuit parameters. The blocked-rotor test procedures require reduced voltage and frequency in addition to preventing the rotor from rotating which is a difficult task [2]. Comparison of actual motor efficiencies is certainly a valid tool to justify the use of one motor over another motor. In the field, one may estimate the efficiency based on information from the name plate and input measurements, such as the slip method(SM) and current method (CM) [2]. The slip method presumes that the per unit (p. u) of load is closely proportional to the p. u. of the ratio of measured slip to full-load slip and The current method presumes that the p. u. of load is also closely proportional to the p. u of the ratio of measured current to full-load current. Using SM and CM methods, a few problems may occur. First the nameplate efficiencies of a given motor can be evaluated according to different standards. The motor may have been rewound. Hence, the error in estimated efficiency could be very high. Numerical and genetic algorithm based efficiency determination via equivalent circuit model is discussed. Exact representation for all losses in equivalent circuit is not available predetermination perhaps closely compute motor

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parameter and not efficiency [3]. Similarly in [4] they additionally recognized stray load loss with respect to load and motor capacity as suggested by IEEE standard 112-1996 [5]. For predetermining the motor parameter we need sophisticated skill in evolutionary algorithm [4]. This proposed method simply based on motors torque slip relation as explained below.

II. Torque Slip Method

The torque exerted by the motor as a function of slip is given by a torque curve. Over a motor's normal load range, the torque line is close to a straight line, so the torque is proportional to slip. As the load increases above the rated load, increases in slip provide less additional torque, so the torque line begins to curve over. Finally at a slip of around 20% the motor reaches its maximum torque, called the "breakdown torque". If the load torque reaches this value, the motor will stall. At values of slip above this, the torque decreases. In 3-phase motors the torque drops but still remains high at a slip of 100% (stationary rotor), so these motors are self-starting.

A typical torque slip characteristic is shown in figure.1. The amount of torque can be produced by induction motor increases linearly as the slip increases [6], [7]. Beyond the full load operating point this relation become reverses. For small value of slip rotor reactance is negligible compared to rotor resistance. So torque is proportional to the slip when slip approaches unity or large values of slip, rotor reactance is large compared to rotor resistance so it is negligible compared to rotor reactance. Now torque is approximately inversely proportional to the slip as shown by hyperbola. Using this plot it is possible to predict induction motor the mechanical power output torque which is directly proportional to output power. The rotor reactance should be kept as low as possible otherwise torque developed is reduced. The maximum torque is independent of rotor resistance, but the value of slip at which maximum torque occurs is directly proportional to rotor resistance.

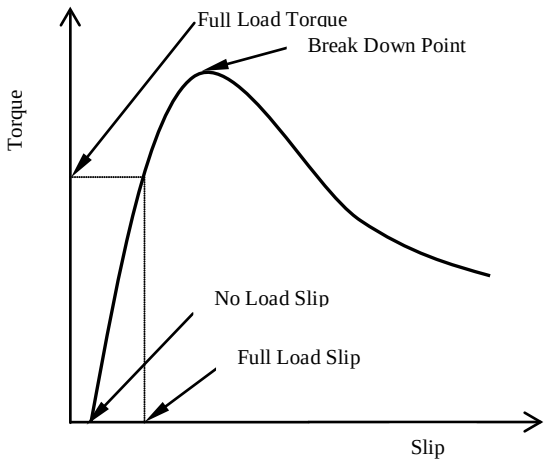

Figure 1 : Torque-slip characteristics of induction motor

Practically motor can be operate up to full load torque point beyond that no longer it can operate as motor and torque slip relation is common for all kind of induction motor. The main difference is only in altitude of full load torque. These inferences are reveals the way of simple on site measurement, the required data for estimating efficiency of induction motor via this test are operating speed, input power and name plate data of the motor. For constructing torque slip plot of test machine requires no load and full load speed of motor and full load power output, which are avail in the motor's data sheet. By knowing input power it is possible to compute the efficiency. Input power and operating speed of the motor can be measured using portable meters at the operating range. This proposal deals difficulties during efficiency estimation of induction motor in its operating environment. This method can be related to direct load test because the output of this method is torque output of motor then using equation (3) efficiency can be measured.

III. Formula Used

a) Slip

The rotating field revolves with the speed of synchronism, and if the rotor conductors were to revolve at the same speed there would not be any torque. Hence, there is a difference between rotor and rotating field speeds. The rotor speed is less than the rotating field speed and the difference in speed is known as the slip of motor. Generally, slip lies between 0 to 1.

$$\text{Slip} = \frac{N_S - N}{N_S} \quad (1)$$

b) Torque

The shaft of an ac induction motor rotates because of force created by the interaction between magnetic field of stator and the rotor of motor. The torque developed by the rotor is proportional to the product of rotor current and fundamental magnetic flux cutting the rotor. The total operating torque is the torque to produce the rated power at operating speed of the motor.

$$T = \frac{P \times 9.55}{RPM} \quad (2)$$

c) Power

The torque produced by an induction motor is a function of the shaft power and the shaft speed where the torque reduces with speed for constant power.

$$P = \frac{T \times RPM}{9.55} \quad (3)$$

This is the formula of power output of electric motor.

Where,

P - Power output of motor in kW
Ns - Synchronous speed of motor in RPM
N - Actual rotor rotating speed in RPM
RPM - Operating speed in RPM
T - Torque developed at rotor in Nm

IV. Test Procedure

In this section procedure of proposed method is explained. Initially we need to develop torque slip curve of the motor then for efficiency determination we measure input power and shaft speed of motor at its output terminal. Data required to construct the torque slip curve are full load power output in kW, Full load speed, No load speed in rpm.

The main steps involved in the field test are explained Choose the machine based on preliminary audit report, select suitable portable meters with greater accuracy, and allow the test machine to operate under normal operating range. Measure the power input to the motor and operating speed of motor using portable meters. With the help of data sheet given by manufacturer, construct the Torque Slip characteristics of the motor using no-load speed, full load speed and capacity with the equations (1), (2). Find out the slip of motor under operating condition using (1). With the aid of calculated slip value, compute the output torque by projecting the slip value towards curve and spot corresponding torque in torque plane. Using operating speed and computed output torque, calculate actual mechanical power output by using (3). By knowing power input of motor, it is possible to determine the efficiency of motor.

V. Results and Discussions

The parameter of importance in a motor is efficiency. The efficiencies of induction motors remain almost constant between 50 to 100 percentages of loading [4]. With motors designed to perform this function efficiently; the opportunity for savings with motors rests primarily in their selection and use. When a motor has a higher rating than that required by the equipment, motor operates at part load. In this state, the efficiency of the motor is reduced. Replacement of under loaded motors with smaller motors will allow a fully loaded smaller motor to operate at a higher efficiency.

Table 1 : Results of Direct Load Test

Power input (kW)	Torque (Nm)	Slip (%)	Efficiency (%)
2.45	12.19	2.60	76.00
3.28	16.60	3.26	76.90
3.48	18.79	3.46	81.80
4.15	22.88	3.90	83.00

Table 2 : Results of Torque-Slip Method

Power input (kW)	Torque (Nm)	Slip (%)	Efficiency (%)
2.45	12.00	2.60	74.00
3.28	17.00	3.26	77.98
3.48	19.20	3.46	81.00
4.15	22.95	3.90	82.78

Table 3 : Error In Torque Calculated By Field Test

Load (%)	T.R (Nm)	T.C (Nm)	Error (%)
60	12.19	12.00	1.59
75	16.60	17.00	2.40
80	18.79	19.20	2.10
90	22.88	22.95	0.87

Table 4 : Error In Efficiency Calculated By Field Test

Load (%)	E.R (%)	E.C (%)	Error (%)
60	76.00	74.00	1.44
75	76.90	77.98	1.40
80	81.80	81.00	0.98
90	83.00	82.78	0.24

Table 1 & 2 are shows results obtained by direct load test and on site efficiency estimation techniques respectively. In reference test all the readings are measured directly from the motor and efficiency were calculated by using standard formula, on the other hand Torque and power output of motor was predicted from torque slip plot for proposed field test and considered different load levels. They are 60, 75, 80 and 90% of motor's full load. Table 3 & 4 are shows the comparisons between efficiency and torque calculated from direct load test and proposed method respectively. T.R & T.C are torque calculated by reference test and field test respectively. E.R &E.C are efficiency of motor calculated by reference test and field test respectively. The deviations in onsite method were computed by comparing results with reference test. Error in calculations also tabulated in corresponding table, the maximum obtained results in onsite test 0 to ± 1.5% only(test was repeated for 5 times on same machine at same above mentioned load levels), this deviation in calculation of efficiency is tolerable. Commonly replacement policy is recommended only when measured motor efficiency is lesser than the efficient motor efficiency in the tune of 4% and more. inference provided by table is deviation in calculated result is maximum of ±1.5% ,it is tolerable, how means the effect of small deviation is just extent or minimize the payback period by one or two months.

Study of losses increment in induction motor with respect to rewinding count was simulated for two cases. Main variable parameter is motor's impedance. Of course motor impedance are direct responsible for losses each rewinding practice increase 18-25%of its actual losses. Main reason of losses increment due to rewinding practice are extra inactive copper, poor quality material unskilled labour etc, motor impedance increment rate per rewinding count is 25% of actual impedance.

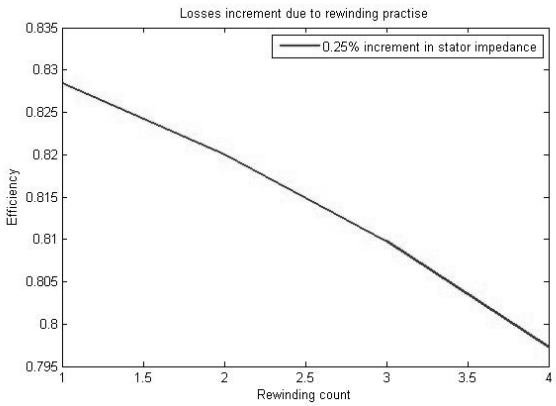

Figure 2 : study of losses increment case 1

VI. Rewound Loss Correction Factor

We cannot directly apply proposed Torque-Slip method to rewound induction motor because rewinding process may increase the losses and alter the capacity of motor as mentioned in the name plate and new capacity of motor is unknown. Such case we need some special calculation to incorporate that changes in motor, that incorporating all the losses in calculation is described as Rewound loss Correction Factor (RLCF) Suppose, One time rewound motor 30 hp motor its normal operating speed at full load is 2970 rpm after rewound its operating speed at full load is 2960 rpm. Speed reduction is 10 rpm.

$$RLCF = \Delta N_r / \Delta N_s \qquad (4)$$

ΔN_r -Change in speed of rotor with respect to normal rotor speed(rpm)

ΔN_s - Change in speed of stator with respect to normal stator speed(rpm)

For this case

$$RLCF = 1.33$$

Actual full load efficiency at normal condition is 92.2% remaining 7.8% goes as losses. In that 5.07% is copper loss and 2.73% other losses (constant, stray, mechanical losses) multiplying this factor with old losses we can estimate actual losses at rewound condition. Only witness parameter to indicate the changes in motor performance is speed of motor. When we know the actual losses it is possible to estimate efficiency of motor.

VII. Tools Description

Name and descriptions of tools are explained, which were used for measuring motor parameters.

- Portable digital power measurement setup Accuracy: +/- 0.5 of full scale for V&I
- Safey: IEC 1010, 600V CAT III
- CT flex rating: 200(expendable with suitable CT)
- Optical tacho meter (Non-contact laser tachometer) Digital Tachometer Automatic range Hand-held optical tachometer VC-623.

VIII. Conclusion

A simple low-cost and accurate method for determining induction motors efficiency at field has been described. The method relies on measuring the input power, and motor shaft speed. The motors' torque and power output are identified using the measured variables, name plate data. The efficiency is then determined using the calculated power output to input power measured. The new method has the potential of quickly estimating the motors' efficiencies on site. The information can then be used to guide future decisions regarding the investment in higher efficiency motors using payback period or present value analysis.

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- Fundamental goal
- To the point depiction of the research
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- Center on shortening results - bound background information to a verdict or two, if completely necessary
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Approach:

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- Leave out information that is immaterial to a third party.

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The page length of this segment is set by the sum and types of data to be reported. Carry on to be to the point, by means of statistics and tables, if suitable, to present consequences most efficiently.You must obviously differentiate material that would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matter should not be submitted at all except requested by the instructor.

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- Present a background, such as by describing the question that was addressed by creation an exacting study.
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	A-B	**C-D**	**E-F**
Abstract	Clear and concise with appropriate content, Correct format. 200 words or below	Unclear summary and no specific data, Incorrect form Above 200 words	No specific data with ambiguous information Above 250 words
Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
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References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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