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Bench Marking Models

Proportional Fair Multiusers

Discovering Thoughts, Inventing Future

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Proportional Fair Multiusers Selective and Switched Channel Scheduling Schemes

By Rupinder Kaur & Muhammad Ejaz Aslam Lodhi
Igit New Delhi, India

Abstract - Presents increasing demand of rates in any digital communication system that excites the research idea of scheduling channel access methodology so as to results in maximizing the sum rate. The reduction in feedback messages for channel state information provides great savings in channel bandwidth for multiuser switched diversity scheduling systems. The present proposed work demonstrates that maximization of sum capacity can be achieved using optimization of per user threshold rate along with some prior estimation of channel state information.The results shown in higher achievable rate. Furthermore the proposed novel multiuser switched diversity MUSD system also achieves proportional fairness criteria along with decentralization of optimization threshold channel.

Keywords : multiuser diversity; per user threshold; proportional fairness scheduling.

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Proportional Fair Multiusers Selective and Switched Channel Scheduling Schemes

Rupinder Kaur[α] & Muhammad Ejaz Aslam Lodhi[σ]

Abstract - Presents increasing demand of rates in any digital communication system that excites the research idea of scheduling channel access methodology so as to results in maximizing the sum rate. The reduction in feedback messages for channel state information provides great savings in channel bandwidth for multiuser switched diversity scheduling systems. The present proposed work demonstrates that maximization of sum capacity can be achieved using optimization of per user threshold rate along with some prior estimation of channel state information.The results shown in higher achievable rate. Furthermore the proposed novel multiuser switched diversity MUSD system also achieves proportional fairness criteria along with decentralization of optimization threshold channel.

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I. Introduction

One of the features of multiuser communication on fading channels is multiuser diversity [1]. By exploiting the fading conditions independently, the multiuser diversity gain can be obtained and scheduling only the users with good channels [2]. To maximize the capacity of information of the uplink in single-cell multiuser communications with frequency-flat fading at any given time, only one user is allowed to transmit with the best channel condition.

Transmitting over the best channel maximizes the system sum-throughput, but results in "Unfair" allocation of the wireless resources among the users. Proportional fair scheduler (PF) which has been studied in this paper provides a good compromise between multiuser diversity gains and fairness [3]. The main goal of this research work or project work is to develop a noble architecture or design of Multiuser switched diversity scheduling scheme that can accomplish the following objectives:

a) Obtain the fairness in Scheduling scheme

Design a system in which a single radio or air link resource can be used for Multi user communication scenario. In spite of conventional selection based scheduling here in this research work, a switching based scheduling scheme has to be obtained that may perform better than the existing systems.

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b) Comparison

A comparison of MUSD schemes with full-feedback multiuser selective diversity opportunistic scheduling schemes is needed to evaluate how much rate we lose due to the feedback savings.

c) Compare the developed system output

With existing full feedback multiuser diversity scheduling system In all wireless communication system, transmitter send pilot signal to all the receivers to measure the condition of channel mention in [4].in opportunistic system, mobile user continuously send the feedback information to base station which causes wastage of air link resources and mobile battery power.so there is need to reduce the feedback load by different methods[5]and [6]. Different methods that can be employed are lossy and lossless compression ,scalar quantization method, Schemes exploiting the fact that only the best user will be allowed to transmit (max-SNR scheduling), and consequently that feedback

Multiuser switched diversity is to find user with good channel condition instead of best user among all suggested in [7].so channel condition if acceptable or not will be determined by considering predefined threshold .per user channel state threshold will be used in this paper[8]. All the users are assigned with time slotted channel .each time slot channel will send one bit flag signal if its achievable rate is more than threshold [9] .so feedback in MUSD will be reduced by assigning this threshold and assigning time slotted channel to users instead of per user feedback channel. This method also removes the congestion by using ordered scheduling.

II. Review of Multiuser Selection Diversity

R Knopp and Humblet in [2] explained the power control mechanism at transmitter in which capacity is increased by transmitting one user at one time over the entire bandwidth having Best channel quality. Received power is estimated at base section to control the transmit power to obtain high capacity. D. Tse in [10] provide solution to multi path fading and losses by dynamically allocation to resources to users based on condition of channel quality of users. So when

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the reception at base station is week user as allocated with more power. T Ericksson and Tony Ottoson in [5] states that sum capacity can be increased by feedback reduction methods. Feedback can be minimized without losing gain by different methods. First: Quantization, in which SNR is quantized before transmission. Second: Max SNR, in which users with only high SNR send feedback. Users with low SNR is unnecessary. Third: Data Compression, In this lossy and lossless compression techniques are used. Lossy compression techniques are transform coding and linear prediction coding etc. lossless compression techniques are arithmetic coding and 54Lempel ziv etc. M. S Alouni in [11] explained that user transmit information only when its channel quality exceed threshold. if channel quality of number of users exceed threshold then random user is selected. But the problem occur when multiple users reply to same threshold then chances of collision occur. So Aim of this paper is to provide solution of various challenges occur in MUSD system. These challenges are; user with strong channel may not get access to the channel, so need is to obtain the fairness by scheduling the users with best channel conditions first rather than others; optimization at central scheduler is not easy because it needs knowledge of pdf of all the users [12]; comparison of multiuser switched diversity with full feedback is required to calculate how much rate is lost. We propose proportional fairness scheme in multiuser switched diversity scheduling by using per-user threshold optimization with the principal function of maximizing the sum of the logarithms of the achievable rates. For each user, independent equations are used that provide solution to optimization.

III. System Model

Consider if there is no delay in the decision of scheduling and block fading channel are used as medium between base station and users. Time slotted channel is used in orthogonal access scheme manner[13]. Each user is allocated with slotted channel include guard band and data burst .guard band is used to send flag signal to base station if its channel quality is higher than feedback threshold. Scheduling is done on following conditions if its channel quality is better than threshold Value [14]. Users prior to given one has achievable Rate less than threshold value. Consider if r_i^* is the threshold value of user i where achievable rate of user I is r_i. User i is scheduled only if $r_i^* < r_i$.r is vector of achievable rates of m users r= $[r_1\ r_2\ \ldots\ldots\ldots\ .\ r_M]$ in this paper, threshold is computed in term of achievable rate.

Channels are considered to be stationary and independent to each other. Probability density function of rate is $f_R(r)$ .pdf of m users are given by $\Pi_{I=1}^{M} f_{R_i}(r_i)$ .if γ_i is SNR of ith user than achievable rate in term of snr is given as $r_i = \log(1+\gamma_i)$ and interm of PDF of snr is $f_R(r) = \exp(r) f_r(\exp(r)-1)$.

Conditional and unconditional Expected achievable rates of user In switched scheduling systemic Average Achievable rate by each user is calculated terms of fri ($^{\gamma}$i). The conditional expected achievable rate by user i is given as

$$R^c_i = E[r_i | r \epsilon s_i] = \int_{r_i} r\, f_{R_i}(r_i)\, dr \quad (1)$$

Where E[] is the expectation operator. Whereas, the unconditional expected value of the achievable rate by user i, denoted as Ri, equals

$$R_i = E[r_i] = E[r_i | r \epsilon s_i].\ \Pr\{r \in Si\} = \Pi_{j<i} f_{Rj}(r_j^*).\int_{r_i^*} r\, f_{R_i}(r_i)\, dr \quad (2)$$

As the fading channels are independent so event r Si happens with probability Pr $\in$Si} = $\prod_{j<i} F_{R_j}(r_j^*)$ Users are scheduled by different time slotted channels.so channel access ratio can be calculated as

$$AR_i = (1 - F_{Ri}(r_i^*) .\Pi_{j<i} f_{Rj}(r_j^*)).$$

IV. Optimization of per user Threshold

In multiuser switched scheduling different users use its different threshold. in comparison to conventional system in multiuser switched scheduling higher capacity is obtained when the optimal threshold is used. Per user threshold can be optimized by maximizing the sum capacity of all users. Optimization problem can be formulated as

$$[\widehat{r_1^*} \ldots\ldots\ldots\ldots \widehat{r_M^*}]\ \arg\ \max_{[\widehat{r_1^*} \ldots\ldots\ldots \widehat{r_M^*}]} \emptyset \quad (3)$$

Threshold optimization of achievable rate is given by $\widehat{r_i^*}$ .the sum achievable rate, Φ can be maximized by equation $\emptyset = \sum_{i=1}^{M} R_i$ To obtain the optimal value of threshold, gradiant of $\emptyset$ is taken w.r.tr_i^* for three conditions .these are i>j, i=j, i<j and equate it equal to 0 solved using [9]. by putting values in $\frac{\partial \emptyset}{\partial r_i^*} = 0, \forall i \leq M$ M.Computing result will be

$$\widehat{r_i^*} = \frac{\sum_{j>i}^{M} R_j}{\Pi_{k<i+1} F_{R_k}(\widehat{r_i^*})} \quad (4)$$

maximize the sum capacity to obtain the optimal value of threshold is always not desirable as it causes problem in fairness so another method proportional fairness scheduler is used.

V. Proportional Fair Scheduler Scheme

Proportional fairness that provides a good trade-off between the aggregate rate over the network and fairness among user [15]. Contention problem in system can be resolved by Proportional fairness scheme by allocating each user with capacity according to its channel condition.in proportional fairness scheme

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optimization can be obtained by maximizing the sum of log of achievable rates $\emptyset = \sum_{i=1}^{M} \log(R_i)$ After taking the gradient and equate it equal to Zero, optimal value of threshold is obtained.

$$\frac{\widehat{r_i^*}\, f_{R_i}(\widehat{r_i^*})}{\int_{\widehat{r_i^*}}^{\infty} r f_{r_i}(r) dr} = M - i \tag{5}$$

M independent equations are used for optimizing the system instead of solving dependent equations in case of MUSD scheduling schemes. So channel of each individual user and location of each user will determines its optimal value of achievable threshold.so threshold value of each user is obtained locally in this case.so in this base station need not to have knowledge of pdf of all user channel thus eliminate the challenge of centralized threshold optimization of conventional MUSD schemes. Optimal value of threshold in the form of SNR is

$$\frac{\log(1+\widehat{\gamma_i^*}) F_{\tau_i}(\widehat{\gamma_i^*})}{\int_{\gamma_i^*}^{\infty} F_{\tau_i}(\gamma) \log(1+\gamma) d\gamma} = M - i \tag{6}$$

VI. Simulation Results Comparison with Ful-Feedback Schemes

The performance of MUSD scheduling schemes is compared with the performance of full-feedback selective scheduling schemes in given figures. Sum capacity for multiuser selective diversity is evaluated and then compared with switched diversity in which feedback bits are minimized by comparing the achievable rate with optimal threshold value. Analyse the case of independent and identically distributed Rayleigh block-faded channels. Comparison between multiuser switched and multiuser selective diversity schemes under i.i.d. Rayleigh blockfading conditions is considered for average SNR of 30db and eight no of users. The maximum sum achievable rates are used for the comparison. The sum capacity were computed for the MUSD scheme and selective system where the per-user thresholds optimization shows that switched diversity scheduling schemes operate within 0.3 bits/sec/Hz from the ultimate network capacity of full feedback systems in Rayleigh block fading conditions over wide range of SNR and for any number of users. Also proportional fairness is achieved as the no of user are increased.

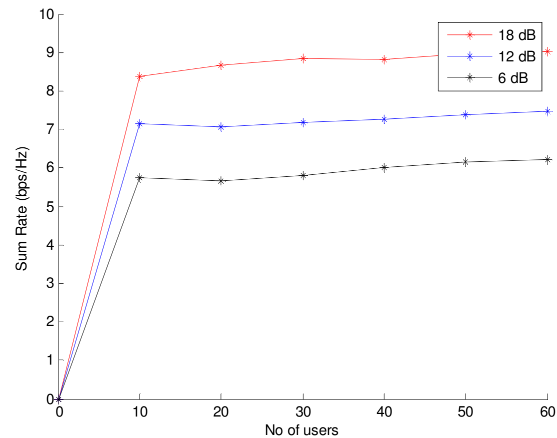

Figure 1: Maximum sum achievable rate of the selection diversity system

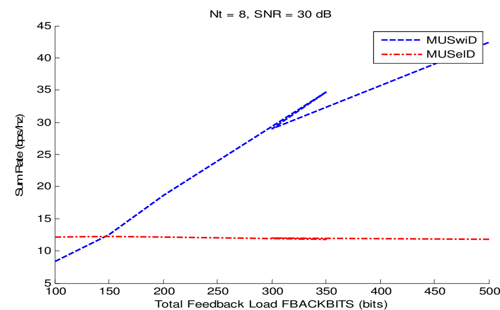

Figure 2 : Maximum sum achievable rate (capacity) comparison between the selection diversity system (dashed red lines) and the switched diversity system (dashed blue lines) as a function of the toatal feedback load in feedback bits. Results are based on average SNR of 30 db

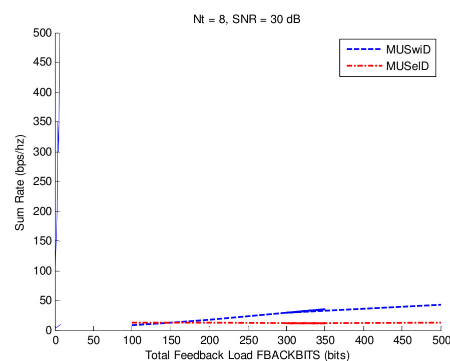

Figure 3 : Maximum sum achievable rate (capacity) comparison between the selection diversity system (dashed red lines) and the switched diversity system (dashed blue lines) as a function of the total feedback bits. Result is based on average SNR of 30db

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Bench Marking Models of Low Power VLSI Testing Strategies: Current State of the Art

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Abstract - Testing time, power dissipation and others are major challenging optimization problems while testing digital circuits and VLSI circuits. Unluckily, most of these problems are frequently solved by heuristic ways which do not assure best solution. The analysis of situation of art models and answers in such optimization problems were carried out in this paper, especially for power optimization in digital VLSI circuit testing.

Keywords : very large scale integration (VLSI), inte-grated circuit(ic), low power testing, bist, ate, scan test.

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Keywords : very large scale integration (VLSI), integrated circuit(ic), low power testing, bist, ate, scan test.

I. Introduction

The method of checking the fabricated IC's for any wrong behavior due to errors like rational error, holdup error, falsehood faults[1],etc is called VLSI testing [1][2][3].Testing is made by creating and putting test vectors which are a set of binary vectors in to the entry of the circuit. Error is found by checking the outcome for the said test vector with kept answers. High fault coverage is the main problem at the early stage of circuit design and testing. Due the latest emerging technology the focus is more towards the new target which has limited test data quantity, condensed test instant and small control testing etc. All possible errors have to be tested in the circuit. To test all the errors in the complete circuit we may require more test vectors. More than one error can be detected by a single test vector and for a single error more than one test vector can be generated. We must create a set of test vectors so that more number of errors can be covered with smallest amount of test vectors. The control dissipated during the normal mode of operation is much lesser when compared the power dissipated during testing of a circuit. The major cause for this difficulty is superior toggling count of the recall component like flip flops. The main aim of checking of chronological circuit is to know such series of test vectors that have more error coverage and also has an optimized toggling calculation. Reordering the test vectors in the examination sequences is the easiest way to improve the power in testing, by checking this the test vectors are not customized, the test reporting is conserved.

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In this paper during digital VLSI circuit testing we used the modern confirmation of the state of art models to improve the power consumption. The major reason for considering power usage throughout test application is that power and energy of a digital system are much higher in the test mode than in system mode [4, 5, and 6]. The motive is that control reduction system mode only starts a few modules where as the test patterns affect as many nodes swapping as probable at the same time. One more reason is the continuous practical contribution vectors functional to a specified circuit has a significant connection, while the connection between the successive test patterns can be very small [7].

II. Taxonomy of Low Power Testing

a) Problems of VLSI circuit testing in negligible power

The latest improvement of complex, high performance, low power devices put into practice in profound submicron technologies generates a new class of many difficult electronic products, like laptop computers, cellular telephones, audio and video based multimedia products, energy efficient desktop computers. Power management becomes a critical factor which cannot be ignored during test development because of this new class of systems. There are three key factors for checking the control properties of a scheme under test [2]:

- The Switching action created in the circuit throughout test application is directly corresponded by the consumed energy, and during the remote testing this has an effect on the battery life.
- The ratio between energy and the test time gives average power consumption. This factor is of high importance than the energy because hot spots and reliability problems are caused by high power consumption.
- The maximum switching action created in the circuit in test throughout one clock cycle is corresponded by the highest power consumption. The thermal and electrical limits of the mechanism and the system wrapping necessities [3] are determined by peak power.

Academic researchers have been carried out on low power design and separately tests have been conducted, during external testing or BSIT the industrial

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practices have needed ad hoc solutions for power consumption [8].The solutions include:

- To bear the high current during testing the power supply,
- Package and cooling is over sized.
- Tests are conducted at reduced operational frequency.
- Needs appropriate test planning and partitioning of the system.

While working with high density systems like modem ASICs and MCMs, in the design phase we have to assure all the power constraints so that we can conduct a non destructive test. Other than the need for stop the circuit under test (CUT) from destruction we also have to consider other factors for reduced power consumption during test application like price, dependability, presentation confirmation, independence as well as knowledge connected issues. All of these problems are discussed in the sequel.

The effect of strong limit on the energy dissipation is due to the constraints of consumer electronic products that need plastic packages. The CUT requires a highly costly package in effect as a lot of switching action during the test leads to an increased high current flow (an increased peak power).Furthermore, it has been found that wearing away of conductors and ensuing stoppage of circuits is caused by electro migration. Electro relocation rate, prominent temperature and existing thickness caused by extreme switching throughout test application are determined by the main parameters like temperature and current density which drastically lowers the dependability of circuits in test. In circuits equipped with BIST this phenomenon is very severe because these circuits are test regularly, for example in online BIST approach. Due to high activity not only the reliability but also autonomy of remote and portable systems motorized by batteries suffer. Remote systems frequently work mainly of their time in standby state with nearly no power consumption, intermittently by regular self tests. Therefore the lifetime of the batteries is increased by saving power during test mode.

The below two points emphasizes on importance of power minimization problem. Firstly, to get rid of too much of heat produced during test application the present tendency in circuit design towards circuit miniaturization (for portability for example) avoids the use of special cooling equipment. Next, the rising use of speed testing to find slow chips no more allows compensating the raise of power indulgence in test by reduced frequency of testing. Earlier, test was basically applied at rates much lesser that a circuit's normal clock rate because only the treatment of fixed at faults were considered to be important. Currently the test to recognize slow chips via delay testing is done by aggressive timing. The high order for presentation specialized dies contrived for use in MCMs is seen in this fact.

One more factor that demonstrates the criticality of this crisis is that the potential of a circuit in dispersing power is not constantly the same during the test and normal form of function. In practical checking of the die immediately after engraving on the wafer, the exposed die is not yet packed and has very less option for power or warmth indulgence. throughout it normal use, the is die is packed considering the quantity of power that needs to be dissipated and at times has extra options like heat dissipated fins. Therefore, during bare die testing because of the absence of packaging the conventional heat removal techniques cannot be used. The applications based on MCMs technology may have a problem because of this, for example, without the access to the completely tested bare dies we cannot realize the possible advantages in circuit density and performance. The overall yield and increasing production cost is affected if proper care is not taken to lower the power dissipation during bare die, the die in the test may be damaged. There are two other factors encouraging the lessening of power in check is given below. The first one is related to the problems found in testing memories via wafer probes[12].High Switching action during testing causes high power and ground noise which are mainly serious during the wafer probing since the power provide links are pitiable. The logical state of circuit lines are erroneously changes because of the high noise, because of which a few good dies fail the test, causing unavoidable loss of yield.

The next reason is concerned with the problems rising during BIST. External testing becomes very tough with modern technologies and Modem design, a promising solution to VLSI testing problems is emerged through BIST. The design used to test methodologies which aim at finding defective mechanism in a arrangement by adding test logic on the chip is called BIST. The Various advantages of BIST are enhanced testability, at regulator speed test of modules, minimum need for automatic test tools and support during system maintenance [12][13].Furthermore, with the upcoming core based "system-on-a-chip" designs, BIST has always been one of the most good testing methods as it helps to maintain the rational property of the design. In BIST, the creation of the patterns are generally got from the Linear Feedback Shift Register (LFSR), the advantage of this is compact size and the ability to work as a Signature analyzer too. Unluckily there in increase in total energy consumption because of the excitation from the LFSR therefore achieving acceptable coverage levels require larger test lengths. The autonomy of portable equipment is reduced with increase in energy consumption, mostly in application where periodical tests are applied. With this when the test vectors are used with supposed process occurrence, the normal

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power indulgence maximizes when compared to the power indulgence in the ordinary mode. This is because of the fact that when a given circuit in its normal mode of operation is applied with continuous functional input vectors has significant correlation; whereas consecutive vectors of a series created by an LFSR is proven to have less correlation [15]. This would compel the use of special packages and cooling systems to maintain the thermal conditions under specifications, therefore the final product cost is increased. It is very significant to lessen the power/energy indulgence in testing in order to assure the cost, performance verification, and autonomy and reliability constraints.

Let's look into another point related to scan supported BIST. Scan supported self test architectures are extremely famous because of it less impact on performance and area[14].Considering small power, scan supported architectures are incredibly costly because of every test outline is escorted with a alter operation with elevated power utilization to supply test model and check the test reply. This is popular in industrial surroundings. To limit the energy indulgence when scan shifting it had to convene the specific power restrictions throughout test mode and shun system destruction.

b) Low Power Testing Strategies

The power degenerates in a CMOS circuit come because of indict and release of capacitances in switching. To clarify this power indulgence through test, let us believe a circuit made up of N nodes, and a test succession of length L used to the circuit inputs. The regular power used at nodule i per switching is ½. C_i . V_{dd}^2 Here C_i is the equal productivity capacitance at nodule i and V_{dd}^2 the energy supply voltage. A high-quality estimate of the energy used at nodule in a time interval t is ½. S_i . V_{dd}^2 , here S_i is the regular number of changes during this period (also known as the switching movement factor at nodule i). Moreover, nodules linked to additional one logic gate in the circuit are nodules having a elevated productivity capacitance. Depending on this reality, and in a primary estimate, it can be said that productivity capacitance C_i is relative to the fan out at node i , named as F_i [Wang 1995]. Thus, an estimation of the energy E_i used at node i throughout the instance interval t is given by:

$$E_i = \frac{1}{2}.S_i.F_i.C_0.V_{dd}^2$$

C_0 is the least productivity capacitance of the circuit. As to the appearance, energy utilization at the logic stage is a task of the fan out F_i and the swapping task factor S_i. The fan out is shown by circuit topology, and the action feature S_i can be checked by a judgment simulator. The product $S_i.F_i$ is called weighted switching action (WSA) at node i and shows the only changeable part in the power used at nodule i in test application.

Based on the formulation above, the energy used in the circuit following function of a pair of succeeding input vectors (V_{k-1}, V_k) can be articulated by:

$$E_{Vk} = \frac{1}{2}.C_0.V_{dd}^2.\sum_i S_i(k).F_i$$

Here i ranges from corner to corner all the nodules of the circuit and $s_i(k)$ is the quantity of changeover initiated by V_k at node i. Currently, let us think the full test sequence of length L needed to reach the plan fault action. The whole power used in the circuit after the function of the whole test series is shown below; here k ranges from corner to corner all the vectors of the test series.

$$E_{total} = \frac{1}{2}.C_0.V_{dd}^2.\sum_i S_i(k).F_i$$

By clarity, energy is specified by the ratio linking power and occasion. The immediate power is usually estimated as the quantity of energy needed through a tiny instant of time t small such as the piece of a clock cycle instantly subsequent the system clock increasing or declining edge. Therefore, the immediate energy degenerate in the circuit after the submission of a test vector is shown by:

$$P_{inst}(Vk) = EVk / t_{small}$$

The peak power communicates to the greatest value of immediate energy checked during test. Consequently, this is shown in terms of the maximum energy used in a low moment of time in the test session:

$$P_{peak} = Max_k\, P_{inst}(V_k) = Max_k\,(E_{Vk} / t_{small})$$

At the end, the average power used in the test session could be checked from the whole power and the analysis time. Taking into account that the analysis time is said by the product L.T, where T matches to the supposed clock period of the circuit, the regular energy can be shown as follows:

$$P_{average} = E_{total} / (L.T)$$

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Though the expression on power and energy stated above is based on a simplified model, it is precise enough for the planned use of power analysis during test. Based on the above expression and considering that a given CMOS technology and a provided voltage for the circuit, it seems that the switching action factor is the only factor that has force on the power, peak power and average power. This tells us that most of the methods suggested till now for decreasing the power and energy during the test are based on the lowering of the swapping action aspect.

c) Low power external testing usimg Automatic Test Equipment

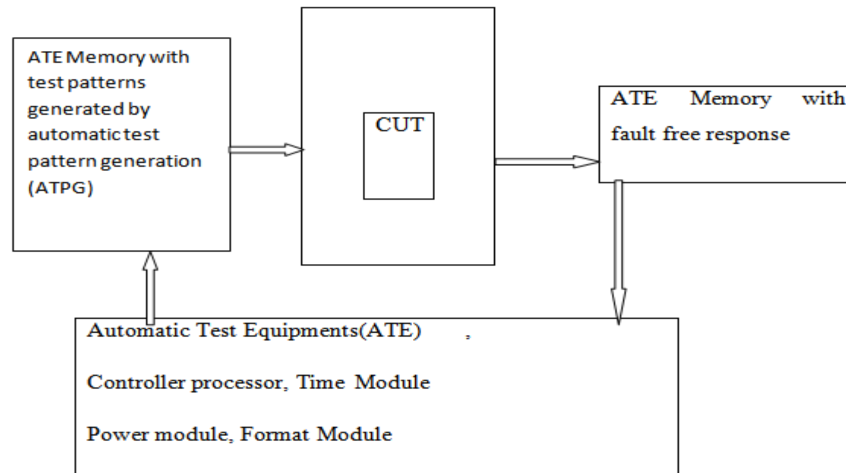

Figure 1 : Basic principle of external testing using ATE

Since the Design complexity of state of art VLSI circuits, automation is majorly considered for creating test process. The fundamental code of exterior testing using automatic test apparatus with the three basic components is shown in Figure 2: manufacturing defects, for integrated circuit parts are tested under this circuit; automatic test equipment (ATE) including control processor, timing module, energy module, and format module; ATE memory that gives analysis model and checks test responses. The summary of the previously outlined components are presented below [16].

The tests are applied to the circuit under test (CUT) which is piece of silicon wafer or packaged apparatus to detect manufacturing defects. Since checking will join and separate millions of pieces to ATE to independently test every part so the links of the CUT pins and bond pads to ATE has to be robust and easily changeable.

Control processor, timing module, power module and format module are there in the ATE. Control processor is a swarm computer which manages the flow of the test procedures and corresponds to the other ATE modules even if CUT is non faulty or faulty. The clock edges required for every pin in the CUT is defined by the timing module. The signal to the pin will go high or low based on the test model information with timing and format in sequence that is extended by the format module, the power supply to CUT is given by power module and it is accountable for exactly calculate power and voltages.

The ATE memory has test patterns given to the CUT and the anticipated non faulty responses are evaluated with the definite answer when testing happens. Voltage reply with mille volt correctness at a timing precision of hundreds of picoseconds is measured by State of art ATE [16]. Automatic test pattern generation (ATPG) algorithms are used to get test patterns or test vectors kept in ATE memory [17]. All through this paper from now on the test model and test vectors are made use of randomly. Random and deterministic algorithms are the classifications of ATPG algorithm. Random ATPG algorithms involve creations of random vectors and the test efficiency is got by error reproduction [24]. ATPG algorithms create tests by doing a structural net list at the logical level of concepts using a particular error list from a error world. Deterministic ATPG algorithms generate smaller and superior value tests in stipulations of test effectiveness when compared to Random ATPG algorithms, at the cost of extended computational time. Low controllability and capacity to scrutinize the inner nodules of the circuit are caused by the increased computational time related with deterministic ATPG algorithms. For sequential circuits this problem is extra severe in spite of the latest advancements in ATPG [18] computational time is huge, and test efficiency is not adequate. Additionally, the problem of getting increased test efficiency is very difficult and time consuming because of the increasing

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difference among the quantity of transistors on a chip and the inadequate input/output pins.

The technique that improves the testability, in conditions of controllability and capacity to observe, by including the test hardware and introducing particular test leaning decisions in the VLSI design flow is called Design for testability (DFT) as seen in Figure 1. This frequently results in smaller test application time, increased fault coverage and hence tests efficiency and easier ATPG. Scan based DFT is the most general DFT methodology wherever chronological basics are adapted to scan cells and initiated into a linear shift register. This made by keeping a scan mode for every scan cell where the information is not put in equivalent from the combinational part of the circuit, because it is shifted in order from the earlier scrutiny cell in the change register. Scan depending on DFT is additionally separated into entire scan and partial scan. The major benefit of full scan is that by changing all the chronological elements to scan cell that lessens the ATPG difficulty for chronological circuits to the additional computationally tractable ATPG for combinational circuits. In contrast, partial scan changes the subset of sequential elements going to lower test area slide at the expenditure of many complexes ATPG. How the test patterns are applied to CUT is described by the introduction of scan based DFT which leads to the change of the test application strategy. A test pattern is applied to each clock cycle in the case of amalgamation circuits or non scan series circuits, Every test model is used in a scan cycle when scan based DFT is used.

d) Low-Power Scan Testing

The problem of too much power during that test that is in the context of scan testing is much harsh than in practical mode. This is mainly due to the fact that application of every test model in a scan plan needs a quantity of shift clock cycles that add to an needless raise of switching activity [19][20]. A study reported in [21] expresses that when 10% 20% of the memory fundamentals (D flip flops and D latches) in a digital circuit modify state in one clock cycle in functional mode, 35% 40% of such memory elements while reconfigured as scan cells can swap state in scan testing. All scan cells can change state. One more report[22] further indicates that the power used during the functional operation is 3 times lesser than the power used in scan testing, in normal functional operation the power is 30 times lesser when compared to the peak power.

Scan design needs reconfiguration of memory elements (regularly D flip flops) in scan cells and next joining them jointly to create scan chains [19] [23] [20]. Every scan test pattern has to be first moved into the scan chains during slow speed testing. To do this we need to set the scan cells to shift mode and putting a quantity of load/unload (shift) clock cycles. In order to avoid high power dissipation scan shifting is usually done at low speed. To incarcerate the test reply of the plan into scan cells capture clock cycle is used. To do this we need to set the scan cells to normal/capture mode. For this setting generally a scan enable signal (SE) is used. The scan design is in shift mode when SE is set to 1 and when it is set to 0, the circuit is moved to normal/capture mode.

From the early 1990s, in the industry to check stuck at faults and bridging faults this slow speed scan test method has been extensively used. The Figure 7.2 shows the shift and capture operations for the classic scan design with the connected current waveform for every clock cycle. This current waveform changes from cycle to cycle since current is relative to the number of 0- to -1 and 1-to-0 changeover on the scan cells which in turn makes swapping in the circuit under test (CUT).

The excessive power during (slow- speed) scan testing can be divided into two sub problems: extreme power in the shift procedure (known as extreme shift power) and extreme energy in the capture procedure (known as extreme capture power) [Girard 20021]. When a lot of flip-flops change their output values at the same time after capture operation the latter is proposed to deal the issues that raises during the clock skew. Many methods have been intended to decrease shift power, capture power or both simultaneously during slow speed scan testing since the last ten years.

e) Low power testing in BIST

Lately new methods have come to handle with the energy and power issues in BIST. To shorten the BIST implementation of tough IC's, particularly during higher levels of test activity Zorian [25] offered a distributed BIST control scheme. When the average power is decreased as a result the temperature associated issues are avoided by the amplifying the check time limit. On the flip side the self-sufficiency of the system is not increased and the total energy remains the same.

Cheung et al. in [26] suggested a technique for the low power test of RAMs. It reduces the energy usage which conserves the test time; the average power is also reduced.

Based on the two different speed LFSRs [27] Wang et al. suggested a BIST strategy called Dual Speed LFSR. They attain a reduction in the regular energy and power usage between 13% and 70 % with no error of mistake treatment.

Lately, Hertwig et al [28] suggested a reduced power strategy for scan based BIST. Energy saving ranged from 70% to 90% evaluated to standard scan based BIST architecture is got from this original design of scan path elements. Zhang et al. in [29] suggested another low power method for scan – based BIST.

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The issue of power limitation in test application for BIST circuit is also seen in [30]. The major restriction is to decrease the energy consumption with changing the stuck at fault coverage. It is seen that energy consumption is not influenced by polynomial selection, regarding energy consumption seed of the LFSR is the major important factor. Thus, a technique based on simulated annealing algorithm is suggested to choose the seed of a known LFSR that gives the least power usage. The untried results collected on the ISCAS benchmarks display difference if the weighted swapping action starting from 147% to 889% based on the selected LFSR seed.

A test vector inhibiting method to sort the non-detecting sub sequences of a pseudo random test order created by a LFSR is shown by Girard et al. in[31]. To accumulate the initial and final vectors of the non detecting sub sequences to b filtered is done by using the decoding logic To carry out a discerning filtering action a D type flip flop functioning in the snap style is made use of to change the enable/disable mode of LFSR. Decrease in the energy consumption is in the choice from 18% to 78% with a small cost in conditions of region slide of the BIST structure (below than 3% of the circuit area). Manich et al. in [32], suggested a enhancement method where the filtering action is complete to all the non-detecting subseries. The main thought is based on the amalgamation of all the deciphered logic modules. For some of the experimented benchmark circuits Energy and average power usage savings can reach a level of 90%.

In [33], a original low power/energy BIST approach based on circuit partitioning is suggested. The aim of this approach is to reduce the average power and energy usage during pseudo-random testing and to decrease the peak power usage without changing the fault coverage. The main idea is to divide the actual circuit into two structural sub circuits so that every sub circuit can be sequentially tested through two various BIST sessions. The average power of the swapping action in a instance time (i.e. the average power) as well as the peak energy usage is reduced when dividing and planning the test session. Furthermore, the total energy usage during BIST is also decreased because the test length needed to check the two sub circuits is not so far from the experiment length for the actual circuit. By slightly modifying conventional TPG structures the suggested approach can be put to whichever test-per-scan or test-per-clock BIST schemes. Results on ISCAS circuits presents that regular energy lessening of up to 62%, high power decrease of up to 57%, and power decrease of up to 82% can be got at very less price in conditions of vicinity slide and with approximately no fine on the circuit with regards to timing.

III. Current State of the Art

The key idea for taking into account power usage in test application is that energy and power of a digital scheme are generally supreme in test mode than in system mode [34] [35] and [36]. The motive is that test models result as much nodes switching as possible but a energy saving system mode only triggers some modules at the identical time. One more motive is that succeeding practical input vectors put to a said circuit during system mode has a important connection, but the connection among successive test models can be very less [37].

In the last decade [-94, 116] there was extensive research done on less power model and testability of VLSI circuits. With the introduction of profound sub-micron technology and tense acquiesce and consistency restraint in order to execute a non-destructive test for supreme show VLSI circuits energy indulgence in test application should not to surpass the energy restraint set by the energy degenerate when the practical process of the circuit [52], [60], [69], [103], [111], [125]. This is because unnecessary energy indulgence in the test application that happens by elevated swapping action may cause the next two problems [69], [118], [126]:

i. Reduced reliability caused by the below two causes: heat indulgence and electro migration. Using the special cooling equipment to remove extra heat indulgence in test application that happens by supreme swapping action is tough and expensive as tests are used at superior levels of circuit incorporation such as BIST. Thus, extra warmth indulgence may cause everlasting harm of the circuit in test or influence the dependability by increasing corrosion mechanisms [118]. Also electro migration rate goes high with heat and present compactness that is not estimated by state of the art approaches [82], [117] which suppose signal correlations that are removed after DFT techniques such as scan or scan BIST are used.
ii. High power/ground noise joined with huge resistive voltage fall causes manufacturing yield loss. If one test is a exposed dice through manufacturing test making use of routine test tools (Section 1.2), energy should be complete during probes that have supreme inductance than the energy and ground pins of the circuit pack-age that leads to considerably higher power/ground noise. The other side shows resistive voltage fall that happens by big greatest immediate current going in the energy lines is miscalculated by methods [82], [117] because they assume signal connections that are damaged when making use of scan based DFT techniques. Thus, high power/ground noise joined with large resistive voltage drop can erroneously modify the judgment state of circuit lines cause a few fine circuits to fail the test, causing the unwanted loss of manufacturing yield.

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Design methods at the logic stage of concept causes sources of high power dissipation during test application and that can be further classified as:

a) The algorithms [42], [48], [81], [85], [108], [113], [115], [122] synthesizes the low power combinational circuits that look to optimize the signal or change probabilities of circuit nodes making use of the spatial addiction in the circuit (spatial connection), and presumptuous the change probabilities of first inputs to be known (temporal connection) [99]. The utilization of spatial and temporary associations in the practical process for less energy mixture of combinational circuits causes elevated swapping action through test application as connection between consecutive test patterns created by repeated test model creation (ATPG) algorithms is very less [109]. This is since a test pattern is created for a said goal error devoid of any thought of the earlier test model in the test series. As a result, increased switching activity is caused by lower connection between successive test patterns during test application and therefore energy indulgence when evaluated to practical process [126].
b) State job algorithms that use state change probabilities [46], [47], [49], [55], [98], [108], [116] synthesize the low power sequential circuits. The state changeover likelihood are calculated considering the key in likelihood allocation and the state changeover graph that are suitable in functional operation. When scan DFT technique is used these two hypotheses are not suitable in the test mode of operation. Whilst changing the test results, the scan cells are linked to uncorrelated values that destroy the connection between successive functional states. Moreover, in the case of data lane circuits with huge amount of states that are created for less energy making use of the relationships among information transfers [53], [84], [86], [87], [88], [89], [90], in the test manner scrutinize registers are linked uncorrelated values that are not at all get to useful process that may cause supreme energy indulgence in the efficient operation.

Design methods at the register-transfer stage of concept causes elevated energy indulgence in test application due to the following. Power aware architectural choice such as power managing where blocks are not concurrently activated during functional operation [45], [90] uses systems which include a elevated quantity of memory fundamentals and multifunctional implementation units. Therefore, motion-less blocks do not add to extravagance in the realistic procedure. The innovative standard for energy association is the systems and their work understanding varied workload in the practical process [44]. Nevertheless, such an supposition is not suitable in test application. To decrease test application time when the system is in the test mode, simultaneous impleme-ntation of tests is needed. Thus, by concomitantly implementing tests a lot of blocks will be energetic at the identical time heading to a difference with the energy management strategy. This will cause elevated power indulgence in test application in contrast to practical process.

To overcome the low connection between repetitive test vectors in test application in combinational circuits a new ATPG tool [126] was suggested. In spite of having, the objectives of protected and low-cost testing of low power circuits the method in [126] maximized the test application time. A special method for decreasing energy indulgence in test submission in combinational circuits is based on test vector order [61], [63], [72], [74], and [75]. The fundamental thought ahead of test vector order is to get a new array of the set such that connection between consecutive test patterns is maximized.

The severity of the test vector-ordering problem that is minimized to get a minimal cost Hamiltonian path in a full, undirected, and weighted graph due to the working time in [61] is very high. The elevated calculating time is triumphed over by the methods suggested in [63], [72], [74] where test vector order assumes a high relation among swapping action in the circuit under test and the hamming space [63], [74] or changeover density [72] at circuit primary inputs. For joined circuits employing BIST many methods for reducing power dissipation were planned newly [50], [57], [58], [71], [73], [95], [96], [97], [120], [123], [124]. In [120] the usage of two speed linear response shift register (DS-LFSR) lessens the changeover compactness at the circuit inputs causing redu-ced power indulgence. The DS-LFSR function with a unhurried and a standard speed LFSR, in order to amplify the association among successive patterns. It has to be known that the slow LFSR has both a unhurried clock and a standard clock as inputs; it also has a control signal that chooses the suitable clock based on the process. It was shown in [120] that test competence of the DS-LFSR is elevated than in the case of the LFSR based on a primal polynomial with a fall in energy indulgence at the cost of much complex control and clocking. Best influence sets for entry signal allocation are dogged in order to reduce average power [124], the best early circumstances in the cellular automata (CA) cells used for model creation [123] found when the peak power is reduced. It was confirmed in [50] that all the ancient polynomial LFSR of the identical size, generate the similar energy indulgence in the circuit under test, therefore recommending the use of the LFSR with the lowest number of XOR gates because it yields the least power dissipation by itself. A

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varied answer based on reseeding LFSRs and test vector restrained to filter a couple of non-detecting sub-sequences of a pseudorandom test series was planned in [-68, 70]. A sub-sequence is non-detecting if all the faults originate by it are also seen by additional notice sub sequences from the pseudorandom test series. An improvement of the test vector restraining methods was shown in [73], [95], [96], [97] where all the non-detecting sub-sequences are removed. The fundamental standard of filtering non-detecting series is to used for decoding judgment to find the primary and the final vectors of every non-detecting series. Later finding the initial vector of a non-detecting series, the restrained structure making use of a broadcast gates network facilitating signal spread [104], stops the submission of test vectors to the CUT. The seed memory is made of two parts which is the exact feature of the proposed BIST structure: the first part has seeds for arbitrary prototype challenging errors and the second part has seeds to inhibit the non-detecting series [71]. The seed memory joined with the interpreted logic is enhanced than only decoding logic in terms of less energy indulgence and elevated error treatment, at the cost of higher BIST area overhead.

For filtering non-detecting vectors motivated by the pre-computation structural design [39] is shown in[58] in different approaches. The MASK block is a circuit with a latch-based architecture or AND-based architecture which also removes or keeps unchanged the vectors made by the LFSR. The facilitate logic trappings a partly specific Boolean function whose on-set [62] is the set of the unchanged vectors and whose off-set is the set of the removed (non-detecting) vectors [58]. A progress in area overhead linked with filtering non-detecting vectors without fine in error coverage or test submission time was got making use of non-linear hybrid cellular automata [57]. The hybrid cellular automata creates test models for the CUT making use of cell configurations optimized for less energy indulgence under set error treatment and test application time constraints. The promptness of multiplier units and linear sized test set needs reaching elevated mistake treatment guide to competent low power.

BIST implementations for information trail [43], [76], [77], [78], [80]: In spite of the accomplishment kind of the test pattern producer, in terms of power dissipation [106] BIST architectures extensively differ one from another. The three diverse architectures were checked for energy indulgence, BIST area transparency and test application time. It was seen [106] that the architecture having an LFSR and a transfer register SR creates lower energy indulgence, BIST area transparency and test relevance time when evaluated to a single LFSR and two LFSRs with mutual feature polynomials. Though, this is achieved at the cost of subordinate error treatment and therefore decreased test competence owing to the customized series of model practical to the CUT that does not find all the accidental model unwilling faults.

The power dissipation as described in [70] is influence by circuit division into sub-circuits and cognized sub-circuit. Test development have the major reason for circuit partition is to get two diverse structural circuits of roughly the same size, so that every circuit can be sequentially experienced in two diverse sittings. To reduce the BIST area transparency of the ensuing BIST scheme, the quantity of associations among the two sub-circuits has to be as less as possible. It was revealed in [70] that by dividing a single circuit unit into two sub-circuits and implement two succeeding tests, reserves in energy indulgence can be got with approximately the similar test application time as in the case of a single circuit unit.

Even though the methods planned for reducing energy indulgence in test application in combinational circuits at the judgment stage of concept gives good results, they can additionally be joined with the methods proposed at register-transfer level.

A test pattern creation method for less energy indulgence was projected in [56] to reduce energy indulgence in non-scan chronological circuits in test application. The technique is developed on three self-regulating steps including unnecessary test model creation, power indulgence size and optimum test series assortment. The explanation suggested in [56] that is based on genetic algorithms gets significant savings in energy indulgence, that cannot be realistic to scan sequential circuits anywhere variable energy extravagance is the major contributor to the whole energy indulgence.

To reduce shifting energy indulgence in scan in order circuits, test vector inhibiting methods suggested for combinational circuits are comprehensive to scan in order circuits [59]. Whether the examination example to be shifted fit in to the subset of notice sequences is detected based on the substance of the LFSR the decoding logic. If the model is non-detecting the dissemination throughout the SR and scan chain is blocked. In [68] the test vector restrained method is complete where the modules and modes with the maximum power indulgence are recognized, and gating logic is initiated to lower power dissipation. In spite of considerable savings in energy indulgence vector recognition and gating logic begin not only important area overhead but also significant presentation degradation for changed scan cell design. In [114] a fresh scan BIST arrangement was suggested that A very elevated fault coverage can be got by a small number of clusters of test vectors based on the experimental observation in [114] a new scan BIST structure. Even though not targeted particularly for small energy indulgence in test application the approach in [114], gives elevated error treatment with connected scan

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pattern that can also cause less energy indulgence. A same method is in use in the little changeover random test model creator (LT-RTPG) projected in [121], where adjacent bits of the test vectors are allocated the same values in most test vectors. A straightforward and quick way to compact scan vectors with achievable devoid of more than energy indulgence was projected in [110]. All the preceding scan-based BIST techniques [59] [68] [110] [114] [121] initiate test area overhead and/or additional show degradation when compared to scan DFT techniques.

A diverse method [61] based on test vector and scan cell order reduces energy indulgence in full scan chronological circuits devoid of any overhead in test area or show deprivation. The input series at the main and pseudo inputs of the CUT, though uneven out test reply in the case of regular scan design is considerably customized when reorder scan cells and test vectors. The new series got after reorder will direct to lower switch action and therefore lessen energy indulgence due to superior connection between successive pattern at the main and pretend inputs of the CUT. Additional benefit of the post-ATPG method projected in [61] is that lessening of energy indulgence in test application got devoid of any cut in error treatment and/or augment in test application time. The method is test set dependent, which means that energy limit depends on the size and the worth of the test vectors in the test set. Due to its test set belief, the method planned in [61] is computationally not feasible because of big computational time needed to discover the huge design space.

A diverse method to get energy reserves is the use of extra key input vectors, leads to additional volume of test data [-88, 189]. The method planned in [119] exploits the unneeded in sequence that comes during scan shifting to reduce switch action in the CUT. Though shifting out the pseudo output part of the test reply in the clock cycles, the price of the main inputs is superfluous. Thus this superfluous data can be broken by compute an additional main input vector for every clock cycle of the scan cycle of each test pattern. On the other hand, in spite of getting considerable power savings the methods needed huge test request time, which is linked to a extensive computational time, and a big quantity of test data. The volume of test data is reduced in [79] where a D-algorithm like ATPG [38] is created to create an only control vector to mask the circuit action while variable out the test responses. Nothing like the method planned in [119] based on a huge number of additional main input vectors, the explanation presented in [79] employ a single extra chief input vector for all the clock cycles of the inspect cycle of each test pattern.

The input control method projected in [79] can additional be mutual with earlier projected scan cell and test vector order [61] to realize, though, modest savings in power dissipation in spite of a considerable decrease in volume of test data when compare to [119]. On the other hand, both methods based on extra main input vectors [-88, 189] needs elevated computational time and therefore are infeasible for great chronological circuits. In spite of their effectiveness for reducing energy indulgence in scan chronological circuits, the previous methods trade off one test parameter at the advantage of an additional test parameter of the scan based DFT technique. Thus new methods are needed for small to average sized and big scan serial circuits.

To defeat the difficulty of high power indulgence in test application at RTL, frequent power-constrained test preparation algorithms were projected under a BIST environment [51], [54], [91], [92], [93], [100], [101], [102], [105], [107], [125]. The method in [125] schedules the tests under power constraint by assemblage and order based on floor plan in sequence. An additional investigation in the explanation space of the development difficulty is provide in [54] where a provide distribution graph formulation for the test expansion complexity is given and tests are scheduled concomitantly devoid of more than their power restraint during test application. To shorten the preparation difficulty the bad case power indulgence (maximum immediate power indulgence) is used to distinguish the energy limitation of every test. The test compatibility graph is annotated with energy and test application time information. The power rating characterized by high power dissipation and test application time are used for scheduling unequal length tests under a power constraint. To conquer the recognition of all the cliques in a graph and the covering table minimization trouble applied in [54], which are well known NP-hard troubles, the solutions planned in [100], [101], [102] use list scheduling, left edge algorithm and a hierarchy growing method as an heuristic for the block test preparation difficulty. Power forced test preparation is comprehensive to system on a chip in [51], [105], [107]. Test communications and power unnatural test preparation algorithms for a scan-based architecture are accessible in [91], [92], [93].

All the earlier methods for power controlled test preparation have unspecified a fixed amount of energy indulgence associated with each test. This is an positive supposition that is not applicable when employ BIST for RTL data paths calculated for less energy due to ineffective energy indulgence.

Observation: The majority of the previous study in less energy testing is alert on scan-based circuits as whole-scan is the extensively adopt test approach in the industry. In a full-scan circuit, all the internal flip-flops (FFs) are replacing by scan-FFs and work in two modes through test: shift style and capture form. In shift style, scan-FFs form scan chains, through which test stimuli/responses can be shift in/out so that we are

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competent to control/observe all the inside memory elements. In capture mode, scan-FFs work as functional FFs such that the test stimuli are applied to the combinational section of the circuit and the test response are stored into these FFs themselves in the next clock cycle. It is probable that the test power usage exceeds the circuit's energy ranking in both shift mode and confine mode. Methods based on scan chain management (e.g, [127][128][134][139]) are very efficient in dropping scan shift power, but does not help in lessening scan capture power. There are also some other methods that decreases the switch actions of the CUT by captivating benefit of the 'don't-care' bits in test cubes, e.g., the low-power routine test pattern creation (ATPG) methods in [129][137] and the test vector treatment techniques in [130][133][135][138]. A few of them are able to decrease scan shift power whilst the others are supportive in decreasing scan capture power. Yet after apply the above methods, it is potential that there remain some patterns that exceed the circuit's power rating if the CUT is large. One answer in this case is to replay low power ATPG for the faults that were found by those problematic patterns [136]. On the other hand, even if such ATPG tools are available, they usually result in bigger test data volume and are computationally very costly. Another solution is to partition the original circuit into multiple sub-circuits and test them separately through clock gating [131]. This not only significantly reduces the power used in the logic part, but also decreases the power used in clock tree, which is a major contributor to test power consumption. Partitioning the circuit for test, nevertheless, frequently involve rerunning the lengthy ATPG procedure for the partition sub-circuits and solve the difficulty of how to get satisfactory responsibility coverage for the glue logic between sub-circuits. An motivating question is whether partition for test can be done with no mention the said limitations?

Regular power usage during scan testing can be managed by minimizing the scan clock occurrence, a well known explanation used in industry. In difference, peak power usage during scan testing is self-determining of the clock occurrence and therefore is greatly tougher to control. Among the power-aware scan testing methods shown, some of them relate openly to peak energy. As said in new industrial experiences [140], scan pattern in various designs may use greatly more peak power over the regular mode and can answer in failures in manufacturing test. For example, if the immediate energy is high, the temperature in some part of the die can go beyond the boundary of thermal ability and then reason immediate injure to the chip. In practice, demolition really happens when the immediate power exceeds the high power grant during many succeeding clock cycles and not just during in one single clock cycle [140]. Thus, such temperature-related or heat indulgence issue speak about more to important regular power than peak power. The main issue with extreme peak power concerns yield decrease and is made clear in the follow-up.

With elevated speed, too much peak power in test reason high rates of current (di/dt) in the energy and ground rails and therefore leads to high energy and ground noise (VDD or Ground bounce). This may incorrectly modify the logic state of some circuit nodes and reason some superior dies to fail the test, therefore leading to needless loss of yield. Likewise, IR-drop and crosstalk things are occurrence that may explain up an error in test mode but not in efficient mode. IR-drop refers to the quantity of reduction (increase) in the power (ground) rail voltage due to the confrontation of the devices among the rail and a node of attention in the CUT. Crosstalk relates to capacitive coupling between neighboring nets within an IC. With high peak power demands during test, the voltages at some gates in the circuit are minimized. This causes these gates to display superior delays, probably foremost to test fails and yield loss [10]. This experience is reported in many reports from a mixture of companies, in particular when at-speed changeover delay testing is done [140]. Typical example of voltage drop and ground rebound responsive applications is Gigabit switches contain millions of logic gates.

Methods based on scan chain handling [141] are very efficient in minimizing shift power, but generally do not help in falling detain power. In particular, the scan chain segmentation method is extensively utilized in the industry due to the fact that it is easy to execute and highly effectual in reducing shift power.

Several research groups have also proposed minimizing test power by modifying the circuit under test. This includes clock gating [142], insert circuitry among the scan chains and the combinational portion of the CUT to block changeover [143][144][145], scan enable disable [146] and circuit virtual partitioning [147]. Circuit alteration methods are able to minimize both shift power and capture power, though, frequently at a higher design-for-testability (DFT) cost.

When compared to the above DFT-based methods, minimizing test power during successful test scheduling and/or test cube treatment methods does not incur any DFT overhead.

Power-constrained test scheduling is frequently conducted in core-based testing, in which we cautiously select surrounded cores that are tested concurrently according to a agreed energy resources [148]. Often times only a little bits in a test model are necessary to notice all the fault enclosed by it; while the lingering bits are "don't-care bits" (also known as X-bits). here are also many methods that minimizes the switch behavior of the CUT by captivating improvement of this property, e.g., the low-power routine test model creation (ATPG) methods in [149][150][151], test compression approach

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in [152], and the assorted X-filling methods projected freshly in [153][154][155][156]. The test cubes may have as much as 95%~98% X-bits [157]. They can be generously filled with moreover logic '0' or logic '1' devoid of affecting the CUT's fault reporting. Low power X-filling methods use this quality to accomplish shift power and/or capture power decrease. As a absolutely software-based solution, these X-filling method do not initiate any DFT overhead and therefore are simply integrated into any test flow. It must also be noted that, even if the known test cube is fully particular, the don't-care bits can motionless be known with method such as the one projected in [158]. Filling X-bits to minimize scan shift power is to create less difference among adjacent scan cells.

Observation : It is shown in [153] that logic value difference occur in diverse position have diverse impact on the shift power indulgence. Filling X-bits to minimize capture energy is very diverse from the above. The aim is to minimize the hamming distance flanked by the input and output of each scan-FF in capture mode (denoted as the scan capture transition count), which is revealed to be closely connected with the circuit's switching activity. In [154], Wen et al. first existing low-capture power X-filling techniques (denoted as LCP-filling) in the literature. Their method tries to minimize the scan capture transition count as much as possible by filling X-bits one by one through implication and line justification ATPG procedures. The filling order of the X-bits extensively affects the results of their method and one of the main boundaries of their technique is that they try to lessen changeover in a single scan cell in every filling step, devoid of considering its effect on the other X-bits. To minimize the computational complexities of the ATPG measures utilized in [154], Remersaro et al [155] introduced a probability-based X-filling method (namely preferred fill) to decrease capture energy. On the other hand, their technique is not capable to weight X bits on capture power reduction efficiencies to get the optimal filling order among them. Because of their diverse objectives, low-shift power X-filling method may result in higher capture power indulgence, and vice versa. As a consequence, it is essential to consider both shift power lessening and capture power reduction during the X-filling development. [156] Takes a fully individual test set as input and generates a new test set with summary shift power and capture power. The authors first identify X-bits in the test set and then fill 50% of the X-bits using preferred fill [155] while the outstanding X-bits are filled next using adjacent fill [153].

Both shift power and capture power can be lessen with X-filling procedure in [156], filling half of the X-bits for capture power minimization and the other half for shift power minimization is not a very good approach. This is because; the shift power indulgence and the capture power indulgence should be dealt with another way. The major purpose in shift power lessening is to reduce the average test power indulgence as much as promising, so that we are able to use increased shift frequency and/or higher test parallelism to minimization of the CUT's test time and hence cut down the test cost; while the main duty in capture power minimization is to keep it under a safe peak power limit and it is needless to minimize it to be the least value.

Test during burn-in at the wafer level augment the repayment that are resulting from the burn-in procedure. The monitoring of de-vice responses while be relevant apt test stimuli during WLBI leads to the easier recognition of faulty devices. This process can be referred as "WLTBI"; it is also referred to in the literature as "test in burn-in" (TIBI) [159], "wafer-level burn-in test" (WLBT) [162], etc. WLTBI technology has lately made fast advances with the arrival of the "known good die" (KGD) [163], i.e., devices that are sold as tested bare die. KGDs are construction blocks of complex system-in-package (SiP) de-sign, wherever chips with various functionalities are united in a single package. The mounting order for KGDs in complex system-on-a-chip (SoC)/SiP architectures, multichip modules, and stacked memories, show the significance for cost effectual and feasible WLTBI solutions [160]. WLTBI will also make possible advance in the manufacture of 3-D ICs, where exposed dies or wafers have to be checked prior they are perpendicularly stacked. WLTBI can therefore be seen as an facilitate technology for cost competent manufacture of reliable 3-D ICs. The vital methods used for the testing and burn-in of entity chips are the similar as those used in WLTBI. Test and burn-in need the accessibility of fitting electrical excitation of the device/die under test (DUT), irrespective of whether it is done on a package chip or a bare die. The only dissimilarity lies in the mode of delivery of the electrical excitation. Mechanically contact the leads provide electrical unfairness and excitation during conservative testing and burn-in. In the case of WLTBI, this excitation can be provided in any of the following three ways: the probe-per-pad method, the sacrificial metal method, and the built-in test/burn-in method [164].

The built-in test/burn-in technique involves the use of on-chip design-for-test (DFT) communications to get WLTBI. This method allows wafers to undergo full-wafer contact using far fewer probe contacts. The existence of complicated built-in DFT features on current day ICs makes "monitored burn-in" possible. Monitored burn-in is a process where a DUT is provided with input test patterns; the output responses of the DUT are monitored online, thereby leading to the identification of failing devices. It is therefore clear that WLTBI has a important possible to lower the generally product cost by flouting the barrier among burn-in and test process. As a result, ATE manufacturers have lately introduce WLBI and test gear that give full-wafer

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contact during burn-in and also provide test monitoring capabilities [160], [162], [165].

There are many practical challenges connected with WLTBI; these comprise full contact burn-in and competent thermal control [164]. Winning WLTBI process also needs during understanding of the thermal characteristics of the DUT. To keep the burn-in time to a least, it is necessary to test the devices at the superior end of their temperature cover [161]. Furthermore, the junction temperature of the DUT need to be maintain in a small window such that burn-in prediction are precise.

For scan testing Power management for WLTBI is very significant. The semi-conductor industry [166] is now extensively used in Scan-based testing. Although, scan testing leads to composite power profiles in test application; in exacting, there is a important variation in the energy usage of a device below test on a cycle-by-cycle basis. In a burn-in environment, the high inconsistency in scan power negatively affects prediction on burn-in time, ensuing in a device individual subjected to extreme or inadequate burn-in [167]. Erroneous prediction may also effect in thermal runaway. Dynamic burn-in using a full-scan circuit automatic test pat-tern creation (ATPG) was projected in [168] with the aim of increasing the number of transition in the scan chains.

Observation : In the semiconductor industry the maximum power usage of ICs in scan-based testing is a severe apprehension in the semiconductor industry; scan power is regularly some times more than the device power indulgence in normal circuit operation [169]. Too much power usage in scan testing can lead to yield defeat. As a consequence, power reduction during test pattern application has lately expected a lot of concentration [170],[171], [172], [173], [174], [175]. Research has alert on model order to lessen test power [170], [176], [177]. The pattern-ordering difficulty has been mapped to the well-known wandering salesman trouble (TSP) [176], [177]. The burn-in at wafer-level needs low variation in power usage during testing semiconductor devices [161]. The need of WLTBI is not addressed in the test-pattern re-ordering method that reduces the dynamic power usage. Particular methods need to be urbanized to address this feature of low-power testing, i.e., the order of test model to reduce the overall variation in power usage.

IV. Conclusion

As devices grow in gate count, scan test data volume and function time grows as well, even for single-stuck-at faults with single-detection. This causes a grave difficulty on manufacturing test because, as test data volume increase, it takes more tester memory to hold the whole test set, and longer to bring the test set through restricted test channels, both important to higher test cost. In addition, considerable research on low power design and testability of VLSI circuits have been shown that the power used in test mode of operation is frequently much higher than the power used in normal mode of process due to the high swapping action in the nodes of the circuit under test which may effect in increased dynamic power indulgence or higher supply current demand. This can reduce the dependability of the circuit under test due to high temperature and current solidity which cannot be tolerated by circuits designed using power reduction method. Unnecessary power indulgence may root hot spots that could harm the CUT. High supply current may cause extreme power supply droop causing to bigger gate delays that cause good chips to fail tests causing yield loss.

Many studies from academia and industry have revealed the need to minimize energy expenditure during test of digital and memory designs. This need is caused by the fact that generally test power could be more than twice the power used in normal functional mode. Since test throughput and developed yield are frequently exaggerated by test power, different test solutions have been projected over the past decade. In this chapter, we converse many low-power test solutions to tackle the above-mentioned problems. Both structural and algorithmic solutions are described the length of with their collision on parameters such as fault reporting, test time, area transparency, circuit show penalty, and design flow alteration. These explanations cover a wide spectrum of difficult environments, together with scan testing, scan-based BIST, test-per-clock BIST, test compression, and memory testing.

External testing with ATE becomes very expensive, as the complexity of modern chips increases. The BIST design technique has been extensively adopted in the design of VLSI circuits in order to facilitate the chip to test itself and to evaluate its answer with a satisfactory cost. On the other hand, the main problem in logic BIST methods is that energy utilization during BIST can go beyond the power rating of the chip or enclose. High average power can cause heat of the chip and high peak power can create noise-related failures. It is predictable that low power test compression methods and functional test techniques need to be projected to like-minded with logic BIST effectively.

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Three-Point Binary Median Filter Implementation using Single-Electron Transistor

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Abstract - Non-linear filters are large family of filters used in signal and image processing. They have found numerous applications such as in digital image restoration, speech processing and coding, digital TV applications, etc. In this paper, three-point median filter is designed using single-electron transistor. In single-electron transistor bits of information are represented by the presence or absence of electrons at conducting islands. Single Electron Transistor (SET), distinguished by a very small device size low power dissipation, high speed and high performance, is one of the most promising nano electronics devices to replace conventional CMOS. The SET technology offers the ability to control the motion of individual electrons in the designed circuits . The Non-linear filter is simulated using a Monte Carlo technique by PSPICE9.1 and their correct and stable logical operation is confirmed.

Keywords : coulomb blockade, electron states, SET, single -electron circuits, Non-linear filters; image processing.

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Three-Point Binary Median Filter Implementation using Single-Electron Transistor

Anbarasu Paulthurai [α], Balamurugan Dharmaraj [σ] & S. Rajasekaran [ρ]

Abstract - Non-linear filters are large family of filters used in signal and image processing. They have found numerous applications such as in digital image restoration, speech processing and coding, digital TV applications, etc. In this paper, three-point median filter is designed using single-electron transistor. In single-electron transistor bits of information are represented by the presence or absence of electrons at conducting islands. Single Electron Transistor (SET), distinguished by a very small device size low power dissipation, high speed and high performance, is one of the most promising nano electronics devices to replace conventional CMOS. The SET technology offers the ability to control the motion of individual electrons in the designed circuits . The Non-linear filter is simulated using a Monte Carlo technique by PSPICE9.1 and their correct and stable logical operation is confirmed.

Keywords : coulomb blockade, electron states, SET, single-electron circuits, Non-linear filters; Image processing.

I. Introduction

The downscaling of complementary metal-oxide semiconductor (CMOS) technology is still in rapid progress and the increase in power consumption has become a major limiting factor in constructing large-scale integrated circuits. Consequently, the single-electron transistor (SET) has attracted considerable attention in recent years because of its potential for high packing density and low power consumption.[1] A variety of useful devices and concepts utilizing the single-electron tunneling features, such as, cellular automata, the binary decision diagram device,[2] and SET logic gates,[3,4] have been proposed and tested by actual devices.

To operate a SET circuit at room temperature, Coulomb islands constituting the circuit should be made extremely small to provide large charging energy that is sufficient to overcome thermal agitation. However, since the operation of a SET is strictly controlled by the amount of charge induced at the center island, reducing capacitances by scaling of a device should be accompanied by increased voltage and current levels.

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Thus, in contrast to the MOS transistor, the power consumption of a SET increases as the possible operation temperature rises, and the possibility of the integration of above $10^{11}/cm^2$ is questionable, since on the order of 10^{-9} W will be dissipated per elementary gate at room temperature [5].

Non-linear filters include well-known filter classes, such as rank order filters (median, min, max, etc.), morphological filters (opening, closing), etc. Rank order filters exhibit excellent robustness properties and provide solutions in many cases, where linear filters are inappropriate. Linear filters have poor performance in the presence of noise that is not additive as well as in cases, where system non-linearities on non-Gaussian statistics are encountered [6].

In this paper we present the implementation of three-point median filter using single-electron transistor. The single-electron transistor circuits have been designed and simulated using a Monte Carlo method [7].

II. Single-Electron Circuits

Single-electron circuits consist of conducting islands, tunnel junctions, capacitors, and voltage source. The islands are arbitrarily connected with tunnel junctions, capacitors and voltage sources. The basic principle of single electronics is that one needs Coulomb energy E_c to charge an island with an electron. This energy is:

$$E_c = \frac{e^2}{2C_i} \quad (1)$$

Where C_i is the capacitance as 'seen' by the island and e is the elementary charge. Electrons tunnel independently from island through tunnel junctions. To assure that electron states are localized on islands all tunnel resistances must be larger than the fundamental resistance R_q:

$$R > R_q = \frac{h}{e^2} \cong 25{,}813\ \Omega \quad (2)$$

Where h is Planck's constant.

To simulate the tunneling of electrons from island to island in a single-electron circuit, one has to determine the rates of all possible tunnel events. The tunnel rate of a possible tunnel event depends on the change in the circuit's free energy caused by this particular event [8]. The free energy F of a single-electron circuit is the differences of the electronic

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energy, U stored in its capacitances and the work done by the voltage sources of the circuit W:

$$F = U - W \tag{3}$$

The electrostatic energy is given by:

$$U = \frac{1}{2}(q, v)\binom{V}{Q} \tag{4}$$

Where, q and v are the unknown parts of the island charge and voltage matrices, respectively, and Q and V are the known parts of the island charge and voltage matrices, respectively. The work done by the voltage sources is given by:

$$W = \sum_n \int V_n(t) i_n(t) dt \quad (5) \tag{5}$$

Where $V_n(t)$ is the voltage of the nth voltage source and $i_n(t)$ is the current through the nth voltage source.

The tunnel rate $r$for a particular tunnel event is given by:

$$r = \frac{\Delta F}{\left(e^2 R_T\left(1 - exp\left(-\frac{\Delta F}{kT}\right)\right)\right)} \tag{6}$$

Where ΔF is the change in free energy caused by this particular tunnel event, (index) R_T is the tunnel resistance of the tunnel junction through which the electron is transported, and kT is the thermal energy (k is the Boltzmann's constant, and T is the temperature). Once the tunnel rates for all possible tunnel events are known the actually occurring event is determined using a Monte Carlo method combined with an exponential distribution of tunnel events [8]. The time duration of a particular event is given by:

$$\Delta t = -\frac{\ln(r)}{r} \tag{7}$$

Where r is an evenly distributed random number in the interval [0, 1]. Among all possible tunnel events, the event with the shortest time duration takes place [9].

a) The SECS simulator

SECS is a single electron circuit simulator based on the Monte Carlo method. The circuit is designed using ORCAD Capture CIS. A single electron component library has been developed for this purpose. This library includes the components of node, ground node, capacitor, tunnel junction and source. The node component can be used either as potential node or charge node. In the second case the background charge can be set to a desired value. The tunnel junction parameters are its capacitance and resistance. The resistance of a tunnel junction includes the modeling of the density of states and the transmission probability. In the single electron component library there are five types of sources, constant, linear, pulse, sinusoidal and a combination type source, which is used when a combination of values between two or more sources is needed, as for example in the stability plot diagram. This design environment provides great convenience for designing and manipulating large circuits.

The simulation uses the description of the circuit provided by ORCAD. Initially SECS parses the description of the circuit and performs a circuit error check. Then the simulation is initiated according to the parameters of temperature and simulating time defined. During the simulation, the free-energy of the circuit at each time step is calculated. Then the difference of the circuit's free energy is calculated for every possible tunnel event DF. From the difference of the circuit's free energy a rate, G, is calculated for all possible events. The tunneling rate is used to calculate the time interval t, for every event to appear. The event that will eventually take place is the one that corresponds to the smallest time interval. The voltages and charges are updated according to the chosen tunnel event and the time advances according to$t$. Following this procedure by the time that the simulation ends the macroscopic behavior of the circuit is determined. This algorithm provides a real time simulation of the behavior of the circuit. Simulation results are obtained in a graphical form of plots of voltage, current, charge and free-energy versus time [10].

III. Power Consumption in SET Circuits

In general, there are three components that constitute the amount of power consumed in circuit operation: dynamic, short-circuit, and leakage power. The dynamic power is consumed due to the charging and discharging of the output capacitance C_L when logic switching occurs, and thus, is inevitable in circuit operation. Short-circuit power occurs when both the nSET and pSET are turned-on simultaneously, conducting short-circuit current from the supply to the ground. The power resulting from the short-circuit current is only a minor fraction of the total dissipation, as long as the output transient times are relatively large compared to the input rise and fall times. However, the short-circuit power in SET circuits is also a function of operation temperature, and, as the temperature increases, it make up a considerable portion of the total power.

The most significant component of the power consumed in the SET circuit is the leakage power. An ideal complementary circuit does not dissipate power when the input does not change. However, in a circuit composed of SETs, leakage power is dissipated by the thermal enhancement of normal tunneling and co-tunneling. The static leakage power due to the thermal enhancement of normal tunneling makes up a considerable portion of the total power as the operation temperature increases.

Because the dynamic power has a quadratic dependence on the supply-voltage, and both the current

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level and voltage level rise as the dimensions of SETs are scaled down, supplyvoltage scalability, while device parameters[11].

IV. Basic Single-Electron Logic Gates

a) The single-electron and gate

The SET AND gate is shown in Fig. 1. The circuit comprises Six Single Electron Transistor (3 nSET and 3 pSET). Instead of two paralleled sourcing (upper) transistors connected to V_{dd} and two series-connected sinking (lower) transistors connected to ground. As with the NAND gate, SET transistors U_1 and U_3 work as a complementary pair, as do transistors U_2 and U_4. Each pair is controlled by a single input signal. If either input A or input B are "high" (1), at least one of the lower transistors (U_3 or U_4) will be saturated, thus making the output "low" (0). Only in the event of both inputs being "low" (0) will both lower transistors be in cutoff mode and both upper transistors be saturated, the conditions necessary for the output to go "high" (1).The AND function built up from the basic NAND gate with the addition of an inverter stage on the output. The voltage V_{dd} is constant and its value is 25mV.

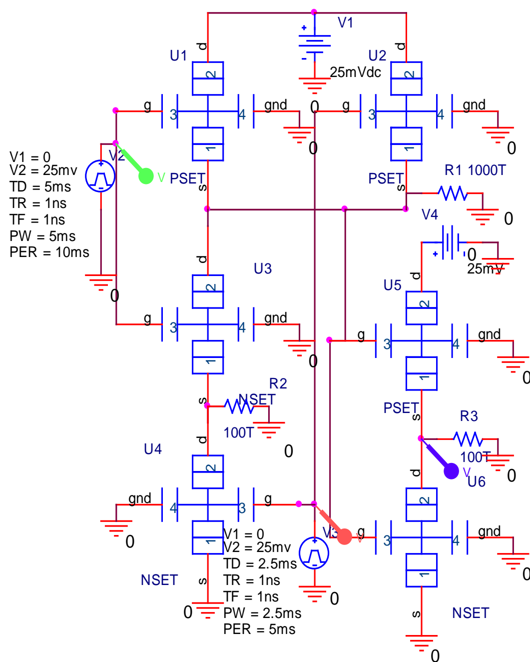

Figure 1 : Internal Circuit of AND gate

The operation of the AND gate is shown in Fig. 2. Fig. 2(a) and (b) shows the time variation of input voltages V_1 and V_2, respectively. The inputs are piece-wise constant and apply all possible combinations of logic '0' and '1' to the gate. Fig. 2(c) shows the time variation of output voltage.

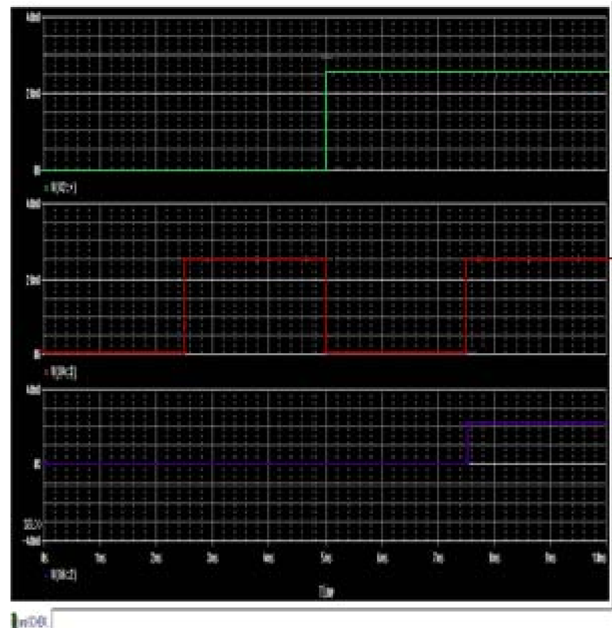

Figure 2 : Simulated input (A, B) and Simulated output (C)

b) The single-electron OR gate

The SET OR gate is shown in Fig. 3. The circuit comprises eight Single Electron Transistor (4 nSET and 4 pSET). As with the NOR gate, SET transistors U_1 and U_4 work as a complementary pair, as do transistors U_2 and U_5 likeU_3 and U_6 . Each pair is controlled by a single input signal. In this circuit upper transistors U_1, U_2 and U_3areserially connected and lower transistors U_4, U_5 and U_6 connected in parallel sourcing to ground. As with the NOR gate, SET transistors U_1 and U_3 work as a complementary pair, as do transistors U_2 and U_4. Each pair is controlled by a single input signal. If both the input A and input B are "high" (1), both the lower transistors (U_3 and U_4) will be saturated, thus making the output "low" (0).

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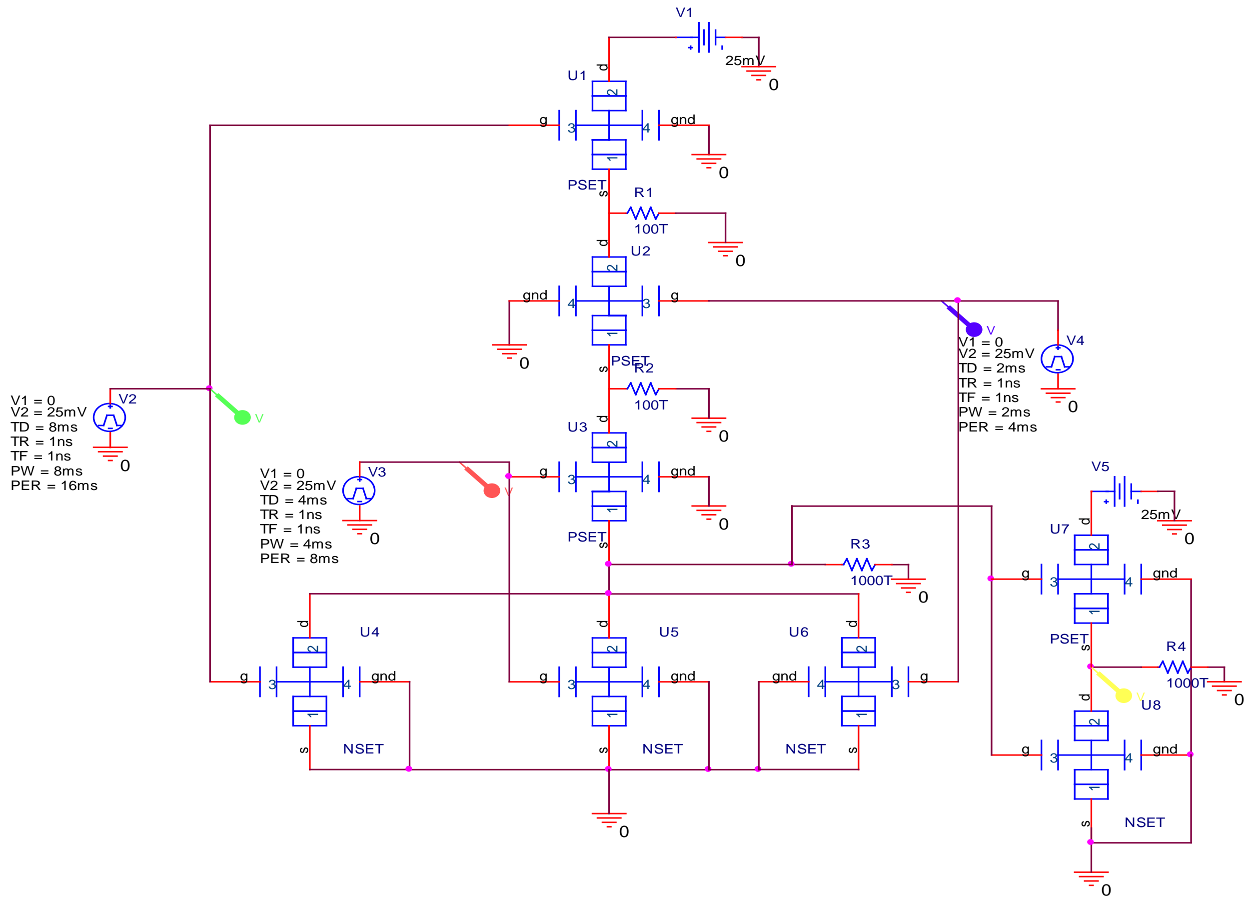

Figure 3 : Internal Circuit of OR gate

Only in the event of both inputs being "low" (0) will both lower transistors be in cutoff mode and both upper transistors be saturated, the conditions necessary for the output to go "high" (1).The OR function built up from the basic NOR gate with the addition of an inverter stage on the output. The voltage V_{dd} is constant and its value is 25mV.

The operation of the OR gate is shown in Fig. 4. Fig. 4(a), (b) and (c) shows the time variation of input voltages V_1, V_2 and V_3, respectively. The inputs are piece-wise constant and apply all possible combinations of logic '0' and '1' to the gate Fig. 4(d) shows the time variation of output voltage

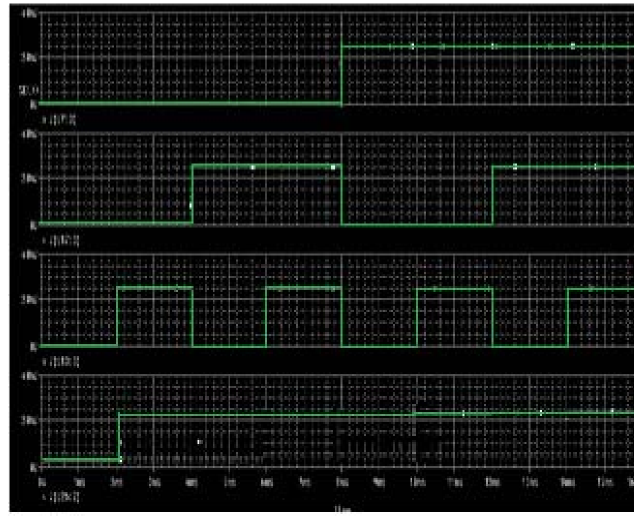

Figure 4 : Simulated input (A B C) and Simulated output (D)

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V. THE BINARY MEDIAN FILTER

A commonly employed filter for restoring binary images is the median filter. Given a window W containing an odd number of pixels, say n, the binary median filter is defined in the following manner for each pixel z, W is translated to z and the filter outputs 1 if more than n/2 pixels in W_z are onevalued; otherwise the filter outputs 0. Medians are used to suppress impulse noise and exhibit good edge preservation if not excessive and uncorrupted image does not possess much fine detail.

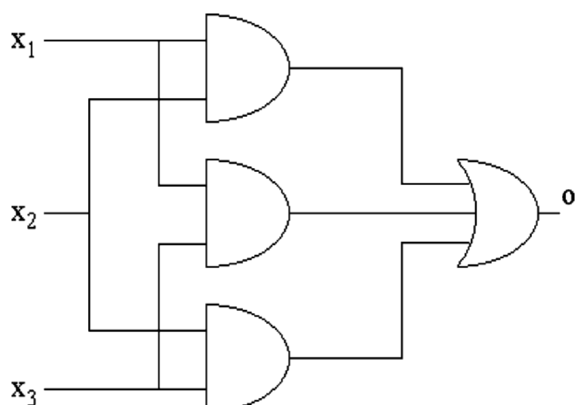

Figure 5 : Logic circuitry for three-point binary median filter implementation

A Boolean function is a binary function $h(x_1,x_2.x_n)$ defined on n binary variables [12]. Since each variable can take on two values, 0 or 1, there are 2^n possible arguments for h. In conjunction with a window W, a Boolean function defines a binary window operator J on binary images via the one to-one correspondence between the variables and pixels in the window. J(A) is defined at a pixel z by translating the window to z and applying the Boolean function h to the binary values in the translated window. As an example, consider the median function. The window consists of three pixels. For instance, it might be the pixel at which the value is being computed together with its left and upper neighbors. Or it might be a three-point filter defined on a binary digital signal, which is a subset of the set Z of integers or, equivalently, an one-dimensional string of 0 and 1 s. Logically [12],

$$h(x_1;x_2;x_3)=x_1x_2+x_1x_3+x_2x_3$$

If the input signal is

000001100100111011000111100000

Then, the filtered output is

000001100000111111000111100000

The filter is implemented by the gate structure shown in Fig. 5.

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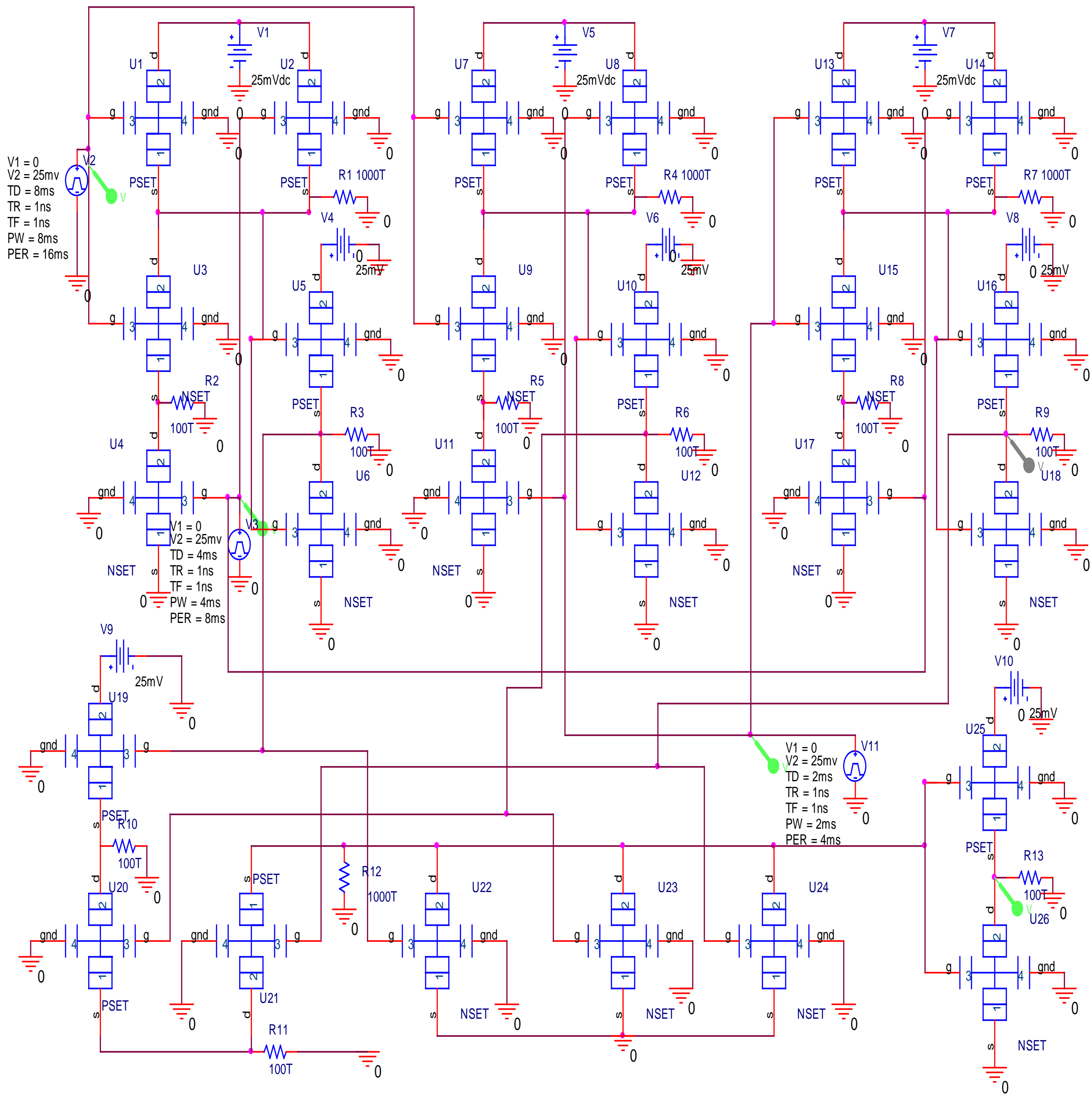

Figure 6 : The single-electron circuit for the three-point binary median filter

The single-electron circuit for the three-point binary median filter is shown in Fig. 6. The single-electron filter comprises three two-input single-electron AND gates and one three-input single-electron OR gate. The single-electron AND gate comprises three NSET and three PSET which are U_1–U_6. The OR gate comprises four NSET and four PSET which are U_{19}–U_{26}. The inputs X_1–$X_3$and the output of the logic circuit shown in Fig. 5, correspond to the input voltages V_1–V_3 and the output voltage of single-electron circuit is shown in Fig. 6. Power to the single-electron circuit is supplied by the voltage sources V_1, V_4-V_{10}. These voltage sources are all equal and are connected to drain. The ground voltages, all equal to $0V$. The input voltages are applied to the gate of the SET and, therefore, no electron transport from the voltage sources to the circuit or vice-versa is possible. The output of the three AND gates, are connected to the inputs of the OR gate.

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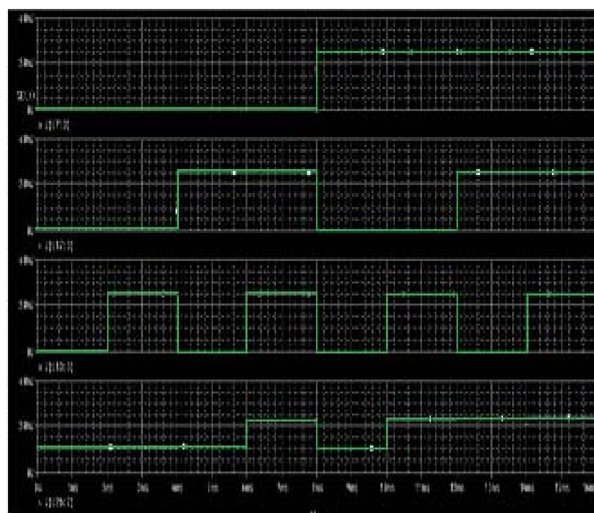

Figure 7 : The operation of the single-electron three-point binary median filter. (a)–(c) Time variations of the input voltages V1–V3, respectively. (d) Time variation of the charge at the output node N14

Fig. 7 shows the operation of the single-electron three point binary median filter. The time variations of the input voltages V1, V2 and V3 are shown in Fig. 7(a)–(c), respectively. The input voltages are piece-wise constant and apply all possible combinations of logic '0' and '1' to the filter. Fig. 7(d) shows the time variation of the voltage at the output. The voltage V_0 at the output section varies from $0$to $25mV$. The electron is well confined into the output section and the single-electron operation is stable.

VI. Conclusion

The imaging algorithms tend to be computationally intensive, especially when directly implemented on standard sequential hardware. Real-time processing for digital imaging concerns efficient deterministic implementation of algorithms. In this paper we designed a three-point median filter using nano electronic single electron circuitry. This nano electronic filter was simulated by using *PSPICE 9.1* at the voltage of$25mV$. The proposed non-linear filter is constructed by 26 transistors and 13 resistors, using single electron transistor (SET) .The proposed three-point median filter implementation using single-electron transistor has the potential advantages of less power, smaller area requirements and faster processing compared to conventional microelectronic implementation.

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A Novel Unified Power Quality Conditioning System for Power Quality Improvement and Bidirectional Power Flow Control for Windmill

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Abstract - This paper proposes a new approach of unified power quality conditioner which is made up of a matrix converter to mitigate the current harmonics, voltage sags and swells and control the power flow with Bi directional capability for windmill. Matrix converter injects the compensation voltage on the load-side, so it is possible to mitigate the voltage sag/swell problems, resulting in an efficient solution for mitigating voltage and current related power quality problems. Thus, the proposed topology can mitigate the voltage fluctuations and current harmonics without energy storage elements and the total harmonic distortion produced by the system also very low. Due to the bidirectional power flow capability of matrix converter the proposed unified power quality conditioner capable to control the power flow of the windmill more over it also transfer power bi -directional. The space-vector modulation (SVM) is used to control the matrix converter. Matlab/Simulink based simulation results are presented to validate the approach.

Keywords : matrix converter, unified power quality conditioner, current harmonics, voltage sag/swell, non linear load, windmill, matlab/ simulink.

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A Novel Unified Power Quality Conditioning System for Power Quality Improvement and Bidirectional Power Flow Control for Windmill

Gl.Valsala [α] & L. Padmasuresh [σ]

Abstract - This paper proposes a new approach of unified power quality conditioner which is made up of a matrix converter to mitigate the current harmonics, voltage sags and swells and control the power flow with Bi directional capability for windmill. Matrix converter injects the compensation voltage on the load-side, so it is possible to mitigate the voltage sag/swell problems, resulting in an efficient solution for mitigating voltage and current related power quality problems. Thus, the proposed topology can mitigate the voltage fluctuations and current harmonics without energy storage elements and the total harmonic distortion produced by the system also very low. Due to the bidirectional power flow capability of matrix converter the proposed unified power quality conditioner capable to control the power flow of the windmill more over it also transfer power bi -directional. The space-vector modulation (SVM) is used to control the matrix converter. Matlab/Simulink based simulation results are presented to validate the approach.

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I. Introduction

Power quality is the set of limits of electrical properties that allows electrical system to function in a proper manner . Power quality problems produced by a large increase of the load current, like starting a motor or transformer energizing. The flexible AC transmission system (FACTS), improve the reliability and quality of power transmission system, the custom power devices enhance the quality and reliability of power that is delivered to customers[1]. The main causes of a poor power quality at customer side are harmonic currents, poor power factor, supply voltage variations, etc. [2]. In recent years the demand for the quality of electric power has been increased rapidly. Unified power quality conditioner (UPQC) is one of the best customs Power devices used to compensate both source and load side problems [3]. It consists of shunt and series converters connected back to back to a common DC link. It can perform the functions of both D-statcom and DVR. Fig. 1 shows a basic system configuration of a general UPQC consisting of the combination of a series active filter and shunt active filter [4]. The main aim of the series active filter is harmonic isolation between a distribution system and a load. It has the capability of voltage flicker/ imbalance compensation as well as voltage regulation and harmonic compensation at the utility-consumer point of common coupling (PCC). The shunt active filter is used to absorb current harmonics, compensate for reactive power and negative-sequence current, and regulate the DC-link voltage between both active power filters [5].

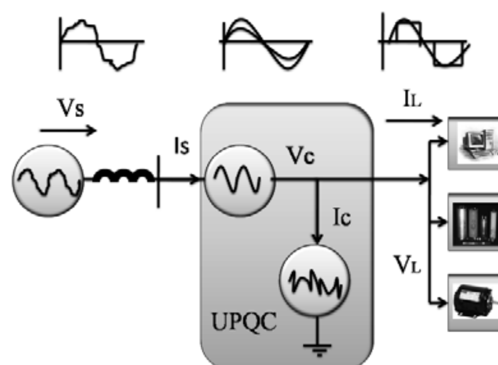

Figure 1 : Basic structure of unified power quality conditioner

Unified power quality conditioner consists the DC bus and its DC capacitor must be designed. Dec capacitor achieves two goals, i.e., to comply with the minimum ripple requirement of the DC bus voltage and to limit the DC bus voltage variation during load transients. But the proposed matrix converter based UPQC there is no need of DC capacitor.

All the series active filter is controlled by the voltage source converter. But voltage source converter has some draw back present. Due to switching loss, capacitor leakage current, etc., the distribution source must provide not only the active power required by the load but also the additional power required by the VSI to maintain the DC-bus voltage constant. Unless these losses are regulated, the DC-bus voltage will drop steadily. Moreover VSC based converter produces more harmonics and switching losses high.

The windmill is the most important non conventional energy source. Various wind turbine

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generators available to convert wind energy to electrical energy. Particularly induction type wind turbine generator is commonly used for its rugged construction ,long life and more power handling capacity. This type of windmill affected by power quality problems like voltage sag,swell and current harmonics.[6] Induction type wind generator initially drawn current from the grid and deliver power through same grid.here the power is bidirectional. Many FACTS are used to solve the power quality issues in windmill [7] .Conventional unified power quality conditioner VSC based converter used,which is unidirectional. So conventional power unified quality conditioner not suitable for induction type windmill.

In this paper a matrix converter based unified power quality conditioner compensates voltage sag and swell and current harmonics compared and bidirectional power flow capability

II. Matrix Converter

In this paper proposes a matrix converter based unified power quality conditioner for wind mill instead of VSC based unified power quality conditioner. Although matrix converter was initially introduced as an AC Driver, due to its advantages may be used in voltage compensation applications like series active filter, DVR [8] and shunt active filter [9].

A matrix converter can operate as a four quadrature Ac-Ac converter circuit. The output voltage, frequency and its amplitude and also the input power factor can be controlled by utilizing the proper modulation method (SVM). The main drawbacks of this topology are the need for fully controlled bi-directional switches and complex algorithm to perform commutation. The nine matrix converter switches can be represented as a 3×3 matrix

$$S = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \quad (1)$$

The relationship between load and input voltages can be expressed as

$$[v_A v_B v_C] = S[v_a v_b v_c]^T \quad (2)$$

Input phase currents can be related to the output phase currents (9), using the transpose of matrix

$$[i_a i_b i_c]^T = S^T [i_A i_B i_C]^T \quad (3)$$

III. Proposed Unified Power Quality Conditioner for Windmill

The proposed unified power quality conditioner for wind mill is designed using a matrix converter is shown if figure 3. l_{abc} are the smoothing inductor. $C_{(abc)}$ is the smoothing capacitor. One step up transformer is used for step up the matrix converter input voltage. So the matrix converter injects the significant current to PCC for current harmonic mitigation.

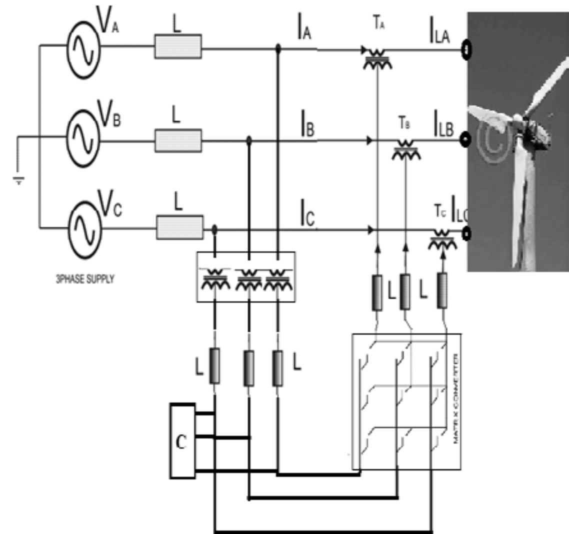

Figure 2 : Proposed unified power quality conditioner

In this paper, the step up transformer was simply modeled by a current source (i_{trans}) and the focus to put on the control of the input current for the active filtering function. Because matrix converter transfer ratio is limited to 0.876.

In series part a unified power quality conditioner is designed using the same matrix converter topology. .Series filter removes the voltage ripples. The series transformer also called injection transformer which injects the appropriate voltage to the load to compensate the voltage and removes the harmonics. more over the series part control the power flow bi directionally by adjusting the matrix converter switching.

Figure.4 shows the fundamental representation of matrix converter based unified power quality conditioner for windmill. V_{pcc} is the point of common coupling. $V_s\angle 0$ is the source voltage. $I_c\angle\beta$ Is the injected current for current harmonic mitigation $A_m\angle\alpha_m$ is the matrix converter amplitude and its phase angle.

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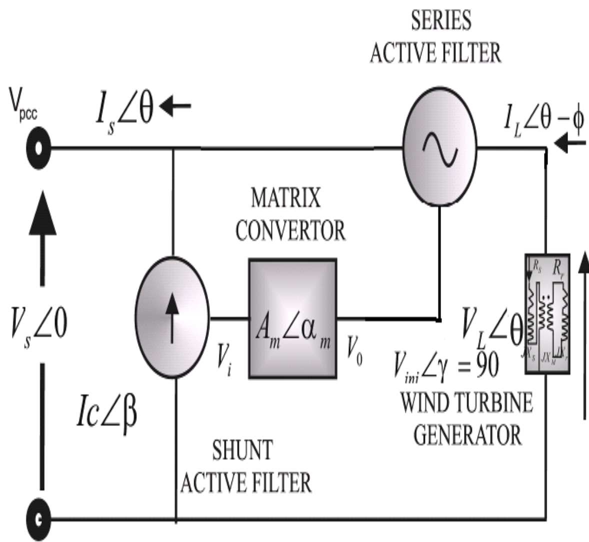

Figure 4 : Fundamental diagram of proposed unified power quality conditioner connected to an induction wind turbine generator

$V_{inj}\angle\gamma=90$ is the injection voltage for voltage compensation. UPQC's series active filter work as isolators, instead of generators of harmonics and, hence, they use different control strategies. Now, here UPQC's series active filters working as controllable voltage sources. With this approach, the evaluation of the reference voltage for the series filter is and shunt active filter required.

IV. The Control System of Matrix Converter Based Unified Power Quality Conditioner for Windmill

a) Series part control system of UPQC

The output terminal voltage and input terminal current consider the low frequency transformation function (4) and set a sinusoidal input voltage, as follows:

$$\bar{v}_{abc} = V_i \begin{bmatrix} \cos(\omega_0 t + \alpha_0) \\ \cos(\omega_0 t + \alpha_0 - 2\pi/3) \\ \cos(\omega_0 t + \alpha_0 + 2\pi/3) \end{bmatrix} \tag{4}$$

$$\bar{v}_{ABC} = D\bar{v}_{abc} = (aD_1 + (a-1)D_2)\bar{v}_{abc} = qV_i \begin{bmatrix} \cos(\omega_0 t + \alpha_0) \\ \cos(\omega_0 t + \alpha_0 - 2\pi/3) \\ \cos(\omega_0 t + \alpha_0 + 2\pi/3) \end{bmatrix} \tag{5}$$

Where ϕ is the output (or load) angle. Using equation (5), the MC output currents can be written as follows:

$$\bar{i}_{abc} = D^T \bar{i}_{ABC} = qI_o \left\{ a \begin{bmatrix} \cos(\omega_i t + \varphi_i) \\ \cos(\omega_i t + \varphi_o - 2\pi/3) \\ \cos(\omega_i t + \varphi_o + 2\pi/3) \end{bmatrix} + (1-a) \begin{bmatrix} \cos(\omega_i t + \varphi_o) \\ \cos(\omega_i t + \varphi_o - 2\pi/3) \\ \cos(\omega_i t + \varphi_o + 2\pi/3) \end{bmatrix} \right. \tag{6}$$

Assume the desired input current to be

$$\bar{i}_{ABC} = I_o \begin{bmatrix} \cos(\omega_0 t + \alpha_0 + \varphi_0) \\ \cos(\omega_0 t + \alpha_0 + \varphi_0 - 2\pi/3) \\ \cos(\omega_0 t + \alpha_0 + \varphi_0 + 2\pi/3) \end{bmatrix} \tag{7}$$

Where φ_i is the input displacement angle.

$$\bar{i}_{abc} = I_i \begin{bmatrix} \cos(\omega_i t + \alpha_i + \varphi_i) \\ \cos(\omega_i t + \alpha_i + \varphi_i - 2\pi/3) \\ \cos(\omega_i t + \alpha_i + \varphi_i + 2\pi/3) \end{bmatrix} \tag{8}$$

b) Power flow control

Considering a symmetrical and balanced three-phase system and applying Kirchhoff laws to the AC line currents are obtained in coordinates

$$\frac{di_d}{dt} = \omega i_q - \frac{R_2}{L_2} i_d + \frac{1}{L_2}(vL_d - vRo_d \tag{9}$$

$$\frac{di_q}{dt} = \omega i_d - \frac{R_2}{L_2} i_q + \frac{1}{L_2}(vL_q - vRo_q \tag{10}$$

The active and reactive power of end generator is given in dq coordinates by

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_d & v_q \\ v_q & -v_d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{11}$$

The active and reactive power P and Q are given by (12) and (13) respectively

$$Q = -v_d i_q \tag{12}$$

$$P = v_d i_d \tag{13}$$

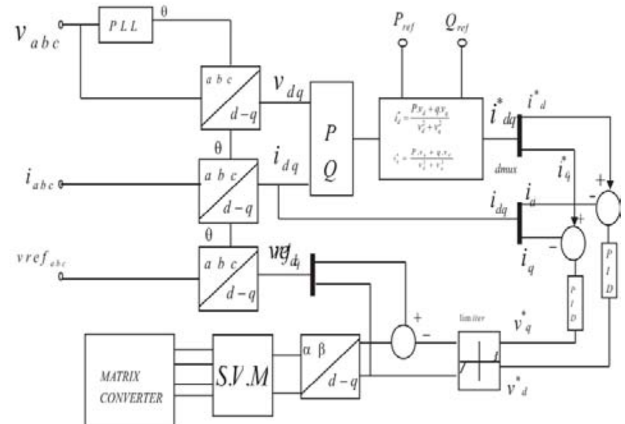

Figure 5 : Control system of series part of proposed unified power quality conditioner

$$i^*_d = \frac{P.v_d + q.v_q}{v_d^2 + v_q^2} \tag{14}$$

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$$i^*_q = \frac{P.v_q + q.v_d}{v_d^2 + v_q^2} \tag{15}$$

Reference *dq* currents converted to a reference voltage as shown in equation

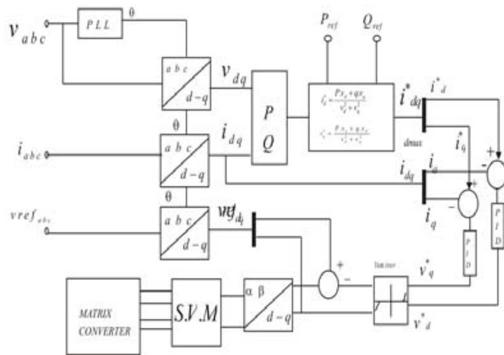

Figure 6 : Control system of shunt part of proposed unified power quality conditioner

$$v^*_d = i_d - i^*_d \tag{16}$$

$$v^*_q = v_q - v^*_q \tag{17}$$

For space vector modulation *dq* values converted to $\alpha\beta$ coordinates.

c) Shunt part control system of UPQC

The load current is measured and transformed from the fixed *abc*-reference frame to the rotating *dq*-reference frame using the relation (18) and the angle of the voltage at the Point of Common Coupling (PCC).

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{18}$$

Since the rotating *dq* reference frame is based on the angle of the voltage at the PCC, the d and q load current components represent respectively the active and reactive components of the load current. The control objective is to compensate all the load current components except for the fundamental active load current component. Therefore a High Pass Filter (HPF) is introduced to filter out the fundamental component of the active current. Only the harmonic and reactive components remain in the current reference. The active current that is produced by the transformer also needs to be added to the active current reference as the matrix converter . Finally are obtained the references d^*_{mc}, q^*_{mc} and which are provided to the outer current control loop. All entities marked with asterisk are reference values as opposed to real/measured values.

To control the current we use eq. (19)

$$L_f \frac{d}{dt}\overline{i_{mc}} = \overline{v_{pcc}} - \overline{v_c} \tag{19}$$

When eq. (20) is converted into the rotating *dq*-reference frame, cross-coupling terms appear as shown in eq. (21). Which must be compensated. When transforming to the rotating *dq* reference frame again cross coupling terms appear

$$C_f \frac{d}{dt}\begin{bmatrix} v_{c-d} \\ v_{c-q} \end{bmatrix} = \begin{bmatrix} i'_{mc,d} \\ i'_{mc,q} \end{bmatrix} - \begin{bmatrix} i_{mc,d} \\ i_{mc,q} \end{bmatrix} - \omega C_f \begin{bmatrix} -v_{c,q} \\ v_{c,d} \end{bmatrix} \tag{20}$$

$$L_f \frac{d}{dt}\begin{bmatrix} i_{mc-d} \\ i_{mc-q} \end{bmatrix} = \begin{bmatrix} v_{pcc} \\ 0 \end{bmatrix} - \begin{bmatrix} v_{c,d} \\ v_{c,q} \end{bmatrix} - \omega L_f \begin{bmatrix} -i_{mc,q} \\ i_{mc,d} \end{bmatrix} \tag{21}$$

Table 1 : Simulation parameter of matrix converter based UPQC

Parameter	Value
V_{source}	440v
L_s	2mh
L_f	0.5mh
c_f	200μf
R_f	0.1Ω
C_i	2μf
Matrix converter Switching frequency	1200Hz
Power system frequency	60Hz

Table 1. Shows the system parameters of the proposed matrix converter based series active filter.

V. Simulation Results

In this work three phase matrix converter based unified power quality conditioner used to compensate the voltage sag/swell, current harmonics and control power flow and transfer power bi-directional for an induction wind mill connected network. The source voltage is 440 Vrms, 60Hz. Table 1 shows the proposed system main parameters. It includes source impedance parameters L and C values for passive branches used system has been simulated. All the simulation is performed by the Matlab/Simulink model in discrete form. The sample time of the discrete value is 3×10^{-4}sec

a) Result for proposed UPQC based compensation for current harmonics

Figure 7 shows the matrix converter based shunt active filter to mitigate the current harmonics efficiency compared to conventional techniques. Figure 7. (a) Shows the supply voltage and the waveform is sinusoidal. Figure7. (b) Shows the waveform of current after proposed compensation. The wave form also sinusoidal and the harmonic content is Low/. Figure7. (c) Shows the total harmonic distortion level. The total harmonic distortion is 2% only. It is clear from figure 7. (c) that the current injected by the matrix converter

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compensates the harmonic of the nonlinear load. The THD of the source current is reduced from 30% to 2%

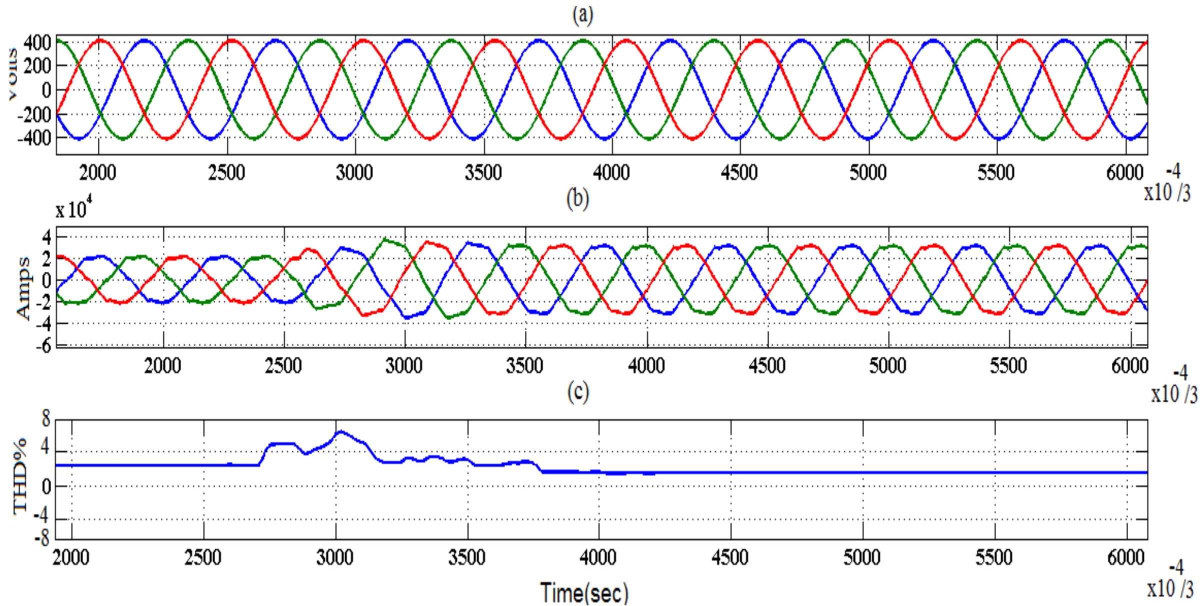

Figure 7 : Proposed matrix converter controlled current harmonic mitigation

(a) Supply voltage (b) supply current after proposed compensation (c) total harmonic distortion of supply current

b) Result in proposed UPQC based compensation for voltage sag /swell condition

Figure 8 shows the single phase representation of the proposed unified power quality conditioner in another case2. The supply voltage is 440 volts and load also reduced. Figure.8a shows the supply voltage at sag and swell conditions. At 0.1 sec to 0.2the voltage sag accrued the voltage sag voltage is at 100 volts. Moreover the voltage sag accrued at 0.3 sec to 0.4 sec of 50 volts. Figure 8.b shows the matrix converter based compensation compensate the voltage sag and swell. Figure 8 .c shows the output of the matrix converter total harmonic distortion. It contains less than 2% of harmonic present.

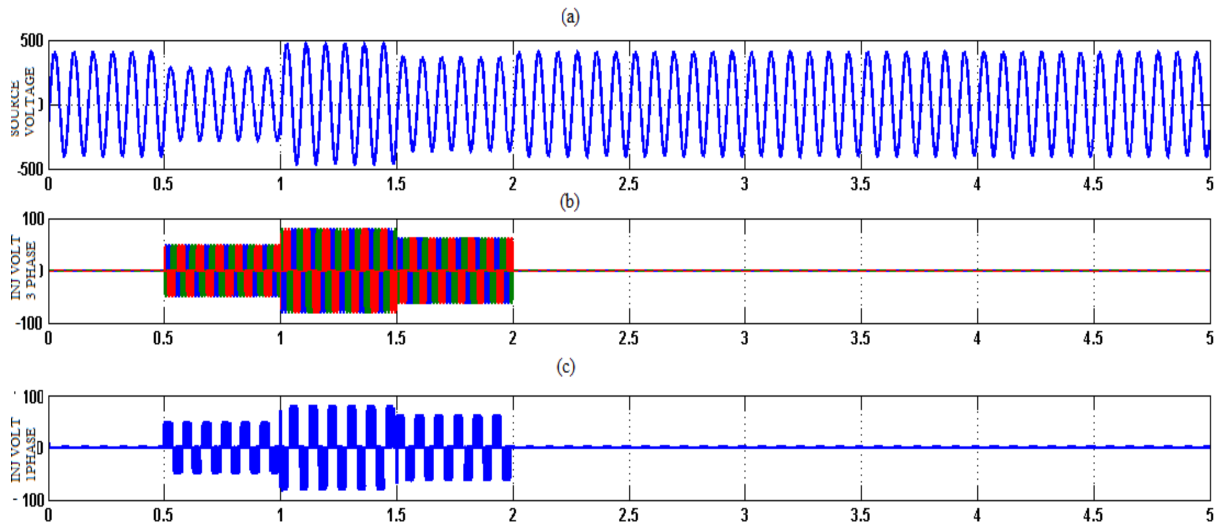

Figure 8 : Proposed matrix converter based UPQC voltage compensation (single phase)

(a) Load voltage after proposed compensation (b) supply voltage (c) total harmonic distortion of load voltage

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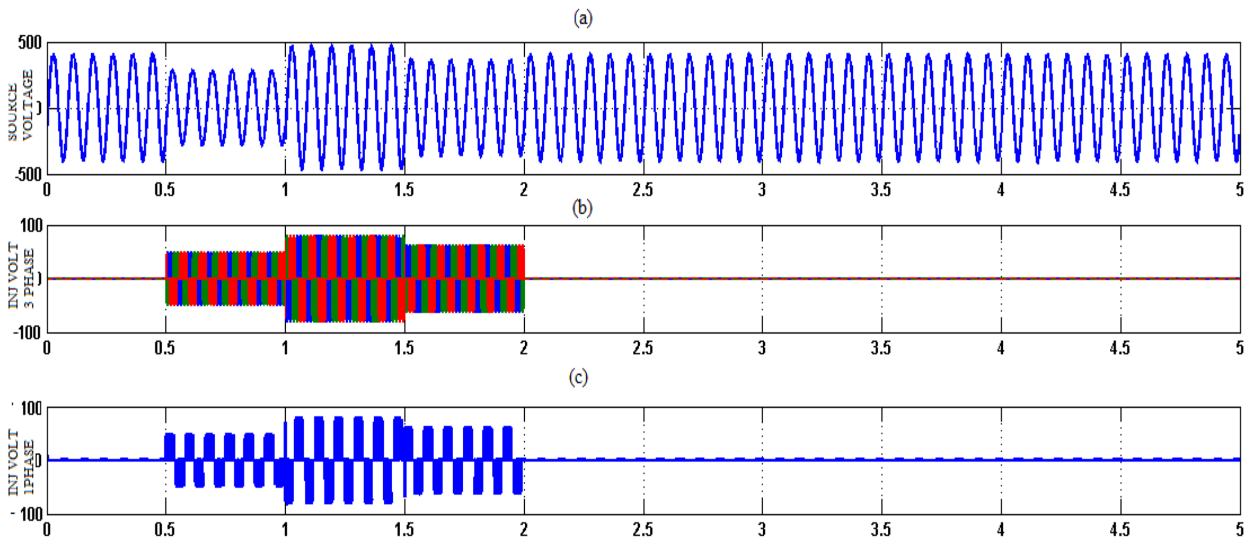
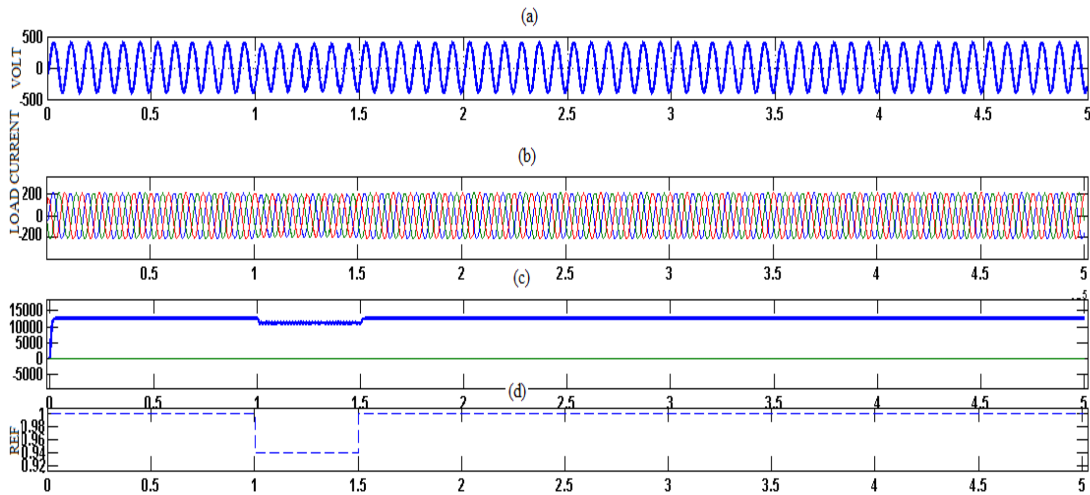


c) Result For injected voltage for voltage sag and swell conditions

Figure 9 : Injected voltage (a) supply voltage (b) injected voltage3 phase (3phase) (c) injected voltage (single phase)

Figure 9. shown the voltage injection through proposed unified power quality conditioner. Figure 9. (a) Shows the fluctuated voltage. The Figure 9. (b) Shows the corresponding injected voltage through the transformer and its matrix converter output voltage shown in figure 9(c).



d) Result For power flow control using a matrix converter based UPQC

Figure 10 : Power flow control using a matrix converter based unified power quality conditioner

Fig 10 shows the power flow control using the proposed matrix converter based unified power quality conditioner. fig10.(a) shows the load voltage. The nominal load voltage is 440 v. Fig 10. (b) Shows the load current.fig10.(c) shows the real power is controlled at 1 sec to 1.5 sec. figure 10. (d) Shows the P ref Value.

The $P_{Reference}$ value set 1 per unit. So the full power is allowed to the load via unified power quality conditioner. After 1 sec the power is set at0.94 per unit. Up to 1.5 sec/. The unified power quality conditioner series part controls the power as shown the simulation result.

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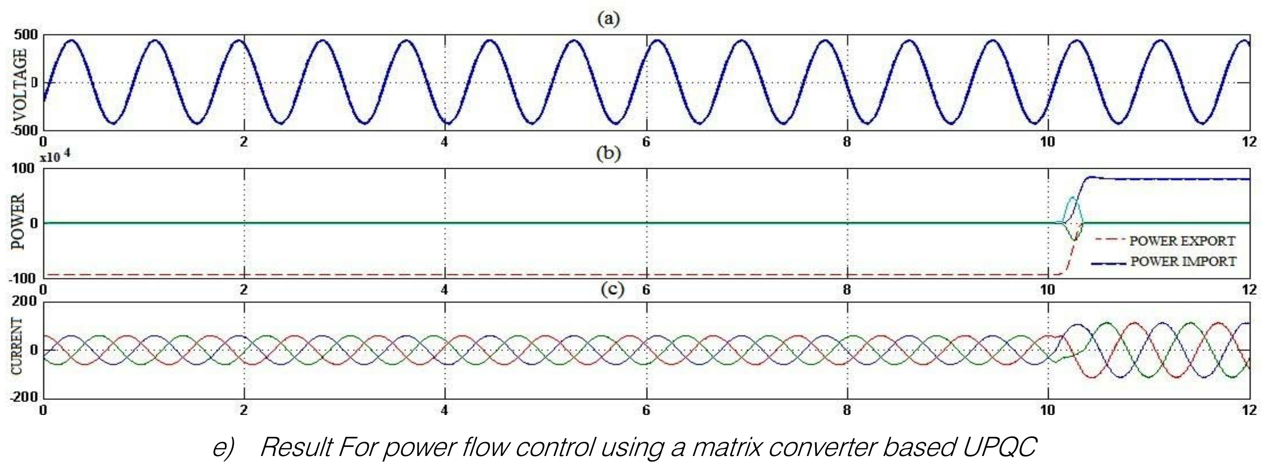

e) Result For power flow control using a matrix converter based UPQC

Figure 11 : Bi-directional power flow using a matrix converter based unified power quality conditioner

Fig 11 shows the bidirectional power flow capability of matrix converter based unified power quality conditioner connected windmill Fig11 (a) shows the windmill terminal voltage of 440volts.figure11 (b) shows the wind mill's power is fed to grid from 0sec to 10 sec. So the matrix converter based unified power quality conditioner transfer power from the load side to source side hence the power flow is negative. After 10.3 sec the wind mill is disconnected from the load side. So the power transfer is stopped and the load consumes power from the source side. So the power flow is another direction as shown in figure power 11.(b). Fig 11 (c) shows the corresponding current from the source. Due to wind mill connected to load side the source side load demand is shared by the wind mill power. After disconnecting the wind mill at 10.3 sec the source current is increased as shown.

VI. Conclusion

In this paper investigated the use of matrix converter based unified power quality conditioner to mitigate the voltage sag/swell, current harmonics and power flow. This paper also analyzed the bidirectional power capability Unified Power Quality Conditions. This can be achieved by change switching of matrix converter .The proposed UPQC's Series active filter handles both balanced and unbalanced Situations without any difficulties and injects the appropriate voltage component to correct any abnormalities in the supply voltage to keep the load voltage balanced and constant at the nominal Value. Moreover this control the power to the load also. The proposed unified power quality conditioner is implemented to wind mill the power transfer also achieved. Moreover the shunt control system controls the remove the current harmonic of load. Based on simulation results the matrix converter based UPQC also mitigates the current harmonics efficiently with low total harmonic distortion, voltage ag and swell and control the power flow bidirectional.

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A Review on UPQC for Power Quality Improvement in Distribution System

By B. Gopal, Pannala Krishna Murthy & G.N. Sreenivas
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Abstract - In recent years, Power engineers are increasingly concerned over the quality of the electrical power. In modern power system consists of wide range of electrical, electronic and power electronic equipment in commercial and industrial applications. Since most of the electronic equipments are nonlinear in nature these will induce harmonics in the system, which affect the sensitive loads to be fed from the system. One among the many compensating devices is Unified Power Quality Conditioner (UPQC) which specifically aims at the integration of series-active and shunt-active power filters to mitigate any type of voltage and current fluctuations and power factor correction in a power distribution network, such that improved power quality can be made available at the point of common coupling. In This paper presents a comprehensive review on the unified power quality conditioner (UPQC) to enhance the electric power quality at distribution levels. This is intended to present a broad overview on the different possible UPQC system configurations.

Keywords : power quality (PQ), harmonics, voltage sag, voltage swell, active power filter (apf), unified power quality conditioner (UPQC).

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A Review on UPQC for Power Quality Improvement in Distribution System

B. Gopal[α], Pannala Krishna Murthy[σ] & G.N. Sreenivas[ρ]

Abstract - In recent years, Power engineers are increasingly concerned over the quality of the electrical power. In modern power system consists of wide range of electrical, electronic and power electronic equipment in commercial and industrial applications. Since most of the electronic equipments are nonlinear in nature these will induce harmonics in the system, which affect the sensitive loads to be fed from the system. One among the many compensating devices is Unified Power Quality Conditioner (UPQC) which specifically aims at the integration of series-active and shunt-active power filters to mitigate any type of voltage and current fluctuations and power factor correction in a power distribution network, such that improved power quality can be made available at the point of common coupling. In This paper presents a comprehensive review on the unified power quality conditioner (UPQC) to enhance the electric power quality at distribution levels. This is intended to present a broad overview on the different possible UPQC system configurations.

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I. Introduction

The quality of the power is effected by many factors like harmonic contamination, due to the increment of non-linear loads, such as large thyristor power converters, rectifiers, voltage and current flickering due to arc in arc furnaces, sag and swell due to the switching (on and off) of the loads etc. These problems are partially solved with the help of LC passive filters. However, this kind of filter cannot solve random variations in the load current waveform and voltage waveform. Active filters can resolve this problem, however the cost of active filters is high, and they are difficult to implement in large scale. Additionally, they also present lower efficiency than shunt passive filters [1].

This paper focuses on a unified power quality condition (UPQC). The UPQC is one of the APF family members where shunt and series APF functionalities are integrated together to achieve superior control over several power quality problems simultaneously. It is noticed that more than half of the papers on UPQC have been reported in the last five years, which indeed suggest the rapid interest in utilizing UPQC to improve the quality of power at the distribution level [2],[3].

The UPQC is a combination of series and shunt active filters connected through a common DC link capacitor. The main purpose of a UPQC is to compensate for supply voltage power quality issues such as, sags, swells, unbalance, flicker, harmonics, and for load current power quality problems such as, harmonics, unbalance, reactive current and neutral current [4].

II. Power Quality Problems

Power quality is very important term that embraces all aspects associated with amplitude, phase and frequency of the voltage and current waveform existing in a power circuit. Any problem manifested in voltage, current or frequency deviation that results in failure of the customer equipment is known as power quality problem.

The increasing number of power electronics based equipment has produced a significant impact on the quality of electric power supply. The lack of quality power can cause loss of production, damage of equipment or appliances, increased power losses, interference with communication lines and so forth. Therefore, it is obvious to maintain high standards of power quality [3].

The major types of power quality problems are: Interruption, Voltage-sag, Voltage-swell, Distortion, and Harmonics.

a) Interruption

Figure 1 : Interruption

An interruption is defined as complete loss of supply voltage or load current as shown in Fig. 2.Interruptions can be the result of power system faults, equipment failures, and control malfunction. There are

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three types of interruptions which are characterized by their duration:

1. The momentary interruption is defined as the complete loss of supply voltage or load current having a duration between 0.5 cycles & 3 sec.
2. The temporary interruption is the complete loss lasting between 3 seconds and 1 minute,
3. The long term interruption is an interruption Which has a duration of more than 1 minute.

b) Voltage Sags

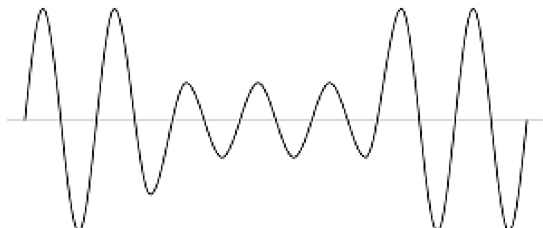

Figure 2 : Voltage Sags

Voltage sags (dips) are short duration reductions inrms voltage caused by short duration increases of the current. The most common causes of the over currents leading to voltage sags are motor starting, transformer energizing and faults. A sag is decrease in voltage at the power frequency for duration from 0.5 cycle to 1min. Voltage sags are usually associated with system faults but can also caused by energisation of heavy loads at starting of large motors as shown in Fig. 3.

c) Voltage Swells

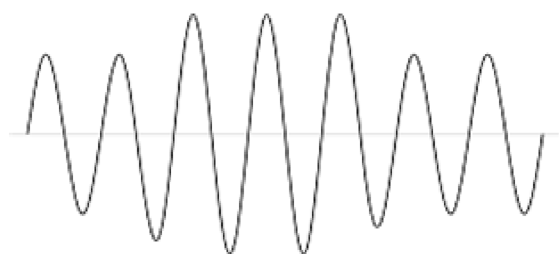

Figure 4 : Voltage Swells

Voltage swell is an rms increase in the ac voltage, at the power frequency, for duration from a half cycle to a few seconds as shown in Fig 4. Voltage swells are normally due to lightning, switching and sudden decreasing in loads, which leads to damage to the motors, electronic loads and other equipments. The severity of voltage swell during a fault condition is a function of fault location, system impedance and grounding.

d) Waveform Distortion

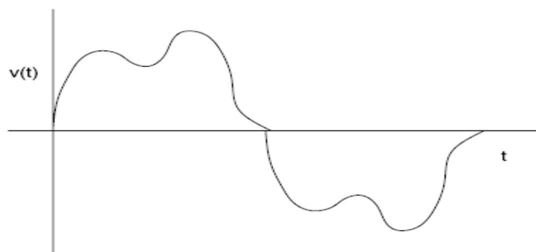

Figure 3 : Distorted Waveform

Voltage or current waveforms assume non-sinusoidal shape called distorted wave as shown in Fig 5. When a waveform is identical from one cycle to the next, it can be represented as a sum of pure sine waves in which the frequency of each sinusoid is an integer multiple of the fundamental frequency of the distorted wave.

e) Harmonics

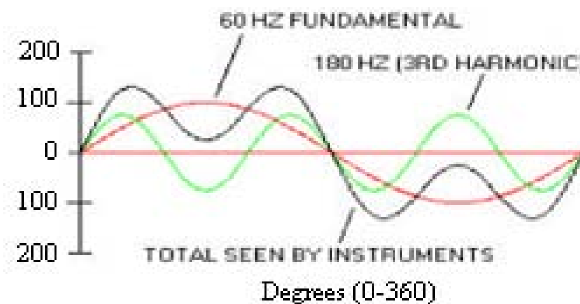

Figure 4 : Waveform with 3rd Harmonic

Harmonics are sinusoidal voltages or current having frequency that are integer multiples of the fundamental frequency. Here, 3rd harmonics is seen in the Fig. 6.

In order to meet PQ standard limits, it may be necessary to include some sort of compensation. Modern solutions can be found in the form of active rectification or active filtering. A shunt active power filter is suitable for the suppression of negative load influence on the supply network, but if there are supply voltage imperfections, a series active power filter may be needed to provide full compensation

III. Basic Configuration of UPQC

In recent years, solutions based on flexible ac ransmission systems (FACTS) have appeared. The application of FACTS concepts in distribution systems has resulted in a new generation of compensating devices. A unified power-quality conditioner (UPQC) is the extension of the unified power-flow controller (UPFC) concept at the distribution level. It consists of combined series and shunt converters for simultaneous

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compensation of voltage and current imperfections in a supply feeder. However, a UPFC only needs to provide balance shunt and/or series compensation, since a power transmission system generally operates under a balanced and distortion free environment. On the other hand, a power distribution system may contain dc components, distortion, and unbalance both in voltages and currents. Therefore, a UPQC should operate under this environment while performing shunt and/or series compensation [5].

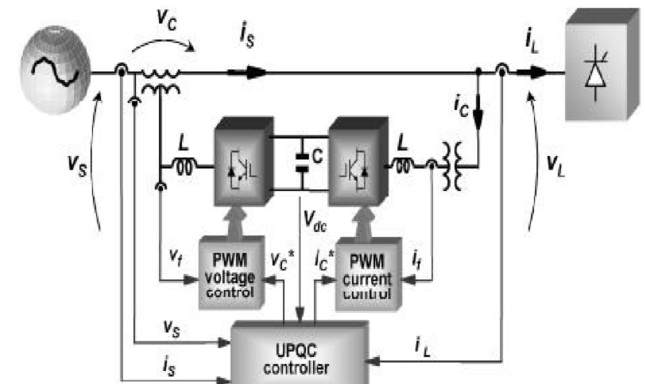

Figure 5 : Basic Configuration of the UPQC

The main purpose of a UPQC is to compensate for supply voltage power quality issues, such as, sags, swells, unbalance, flicker, harmonics, and for load current power quality problems, such as, harmonics, unbalance, reactive current, and neutral current. Fig.1 shows a single-line representation of the UPQC system configuration. The key components of this system are as follows.

1. Two inverters one connected across the load which acts as a shunt APF and other connected in series with the line as that of series APF.
2. Shunt coupling inductor L_{Sh} is used to Interface the shunt inverter to the network. It also helps in smoothing the current wave shape. Sometimes an isolation transformer is utilized to electrically isolate the inverter from the network.
3. A common dc link that can be formed by using a Capacitor or an inductor. In Fig. 1, the dc link is realized using a capacitor which interconnects the two inverters and also maintains a constant self supporting dc bus voltage across it.
4. An *LC* filter that serves as a passive low-pass filter (LPF) and helps to eliminate high- frequency switching ripples on generated inverter output voltage.
5. Series injection transformer that is used to connect the series inverter in the network. A uitable turn ratio is often considered to reduce the current or and voltage rating of the series inverter.

The integrated controller of the series and shunt APF of the UPQC to provide the compensating voltage reference V_C* and compensating current reference I_C * to be synthesized by PWM converters [6], [7].

The shunt active power filter of the UPQC can compensate all undesirable current components, including harmonics, imbalances due to negative and zero sequence components at the fundamental frequency. In order to cancel the harmonics generated by a nonlinear load, the shunt inverter should inject a current as governed by the following equation:

$$I_C(\omega t) = I^*_L(\omega t) - I_S(\omega t) \quad (1)$$

Where $I_C(\omega t)$, $I^*_L(\omega t)$, and $I_S(\omega t)$ represent the shunt inverter current, reference load current, and actual source current, respectively.

The series active power filter of the UPQC can compensate the supply voltage related problems by injecting voltage in series with line to achieve distortion free voltage at the load terminal. The series inverter of the UPQC can be represented by following equation:

$$V_C(\omega t) = V^*_L(\omega t) - V_S(\omega t) \quad (2)$$

Where $V_C(\omega t)$,$V^*_L(\omega t)$,and $V_S(\omega t)$ represent the series inverter voltage, reference load voltage, and actual source voltage, respectively[8] [9].

IV. Classification of UPQC

The Unified Power Quality Conditioner are classified on various bases like converter used, topology, supply type and compensation method. The UPQC is classified in two main groups which is based on, Physical structure and Voltage sag compensation [4].

a) Physical Structure

The key parameters that attribute to these classifications are: Type of energy storage device used, Number of phases, and Physical location of shunt and series inverter.

1. Converter based classification
   a. VSI (voltage source inverter)
   b. CSI (current source inverter)
2. Supply system based classification
   a. Single-phase
      i. Two H-bridge (total 8 switches)
      ii. 3-Leg topology (total 6 switches)
      iii. Half Bridge (total 4 switches)
   b. Three-Phase
      i. Three-wire
      ii. Four-wire

- Four-Leg
- Split Capacitor
- Three-H Bridge

3. UPQC Configuration based classification
   a. UPQC-R (Right Shunt)
   b. UPQC-L (Left Shunt)
   c. UPQC-I (Interline)
   d. UPQC-MC (Multi-Converter)

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e. UPQC-MD (Modular)
f. UPQC-ML (Multilevel)
g. UPQC-D (Distributed)
h. UPQC-DG (Distributed Generator integrated)

b) Voltage Sag Compensation

The voltage sag on a system is considered as one of the important power quality problems. There are mainly four methods to compensate the voltage sag in UPQC-based applications.

1. UPQC-P (Active Power Control)
2. UPQC-Q (Reactive Power Control)
3. UPQC-VAmin (Minimum VA Loading)
4. UPQC-S (Active-Reactive Power Control)

Table 1 : Comparison between Voltage Source Inverter and Current Source Inverter

Voltage Source Inverter (VSI) based	Current Source Inverter (CSI) based
1. The UPQC may be developed using PWM voltage source inverter	1. The UPQC may be developed using PWM current source inverter
2. VSI shares a common energy storage capacitor (C_{dc}) to form the dc-link	2.CSI shares a common energy storage inductor(L_{dc}) to form the dc-link
3. Advantages: - Lower cost, - Smaller physical size, - Lighter in weight, - Cheaper, - Capability of multilevel operation, - Flexible overall control, - High efficiency near nominal operating point.	3. Advantages: - Open loop current control is possible, - High efficiency when the load power is low.
4. Disadvantages: - Low efficiency when the load power is low, - Limited life time of the electrolyte capacitor.	4. Disadvantages: - Bulky and heavy dc inductor, - High dc-link losses, - Low efficiency near nominal operating point, - It cannot be used in multilevel operation.
5. The VSI based UPQC system configuration is shown in given Fig. 7.	5. The CSI based UPQC system configuration is shown in given Fig. 8.

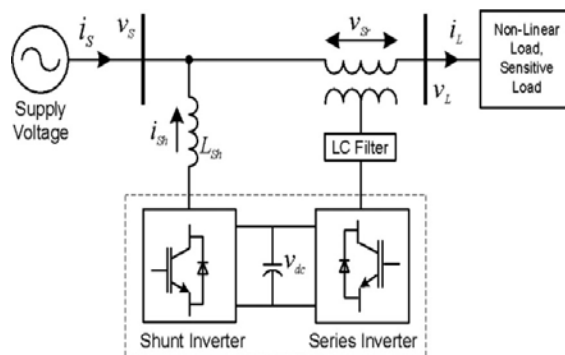

Figure 6 : VSI based UPQC system configuration

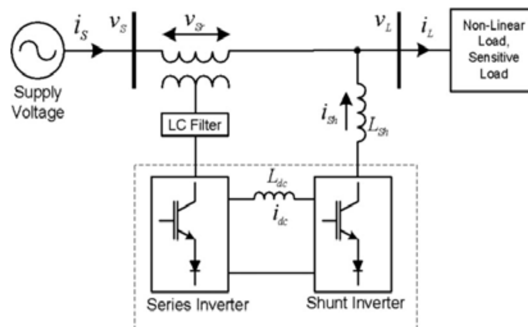

Figure 7 : CSI based UPQC system configuration

From the comparison given in TABLE-1one can find that VSI based UPQC topology is more popular than CSI based UPQC topology.

To mitigate power quality problems in the distribution system and UPQC's different configurations are classified based on the type of supply system. There are mainly two types of supply a) single-phase and b) three-phase.

Single-phase two-wire two-Hbridge UPQC configuration is as shown in Fig. 9. Another two topologies first is 3-leg topology (total 6 switches). Apart from total 6 switches, 4 switches are used in series inverter and 2 switches are used in shunt inverter. Second alf-bridge topology, 2 switches are used in series inverter and 2 switches used in shunt inverter [10].

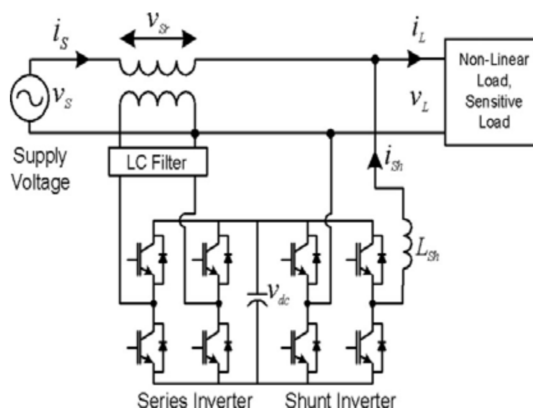

Figure 8 : Single-phase Two-wire UPQC based on

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Two H-bridge configuration (eight switches)

Three-phase three-wire UPQC configuration is as shown in Fig 10. Several non-linear loads, such as, diode rectifier, adjustable speed drives (ASD), controlled rectifier etc. are fed from three-phase three-wire UPQC system [11] [12].

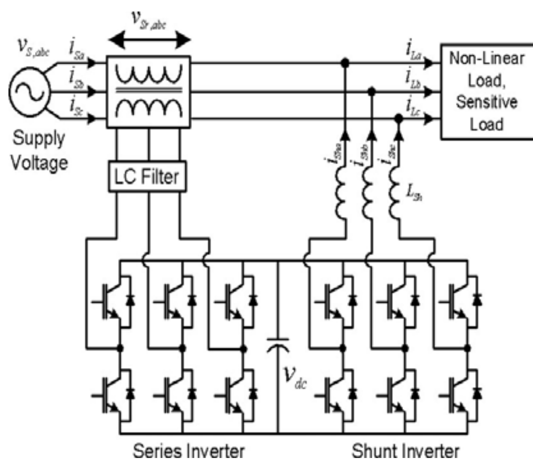

Figure 9 : Three-phase Three-wire (3P3W) UPQC

The combinationof three-phase and single-phase loads are supplied by three-phase four-wire (3P4W) UPQC configuration.

For neutral current compensation in three-phase four-wire (3P4W) system, various shunt inverter configurations are given, namely, four-leg (4L), two split-capacitor (2C) and three-H bridge (3HB) [13] [15].

The 3HB topology use three single-phase H-bridge inverter connected to same dc bus of the UPQC. The 2C topology use two split-capacitor on dc side and the midpoint of two capacitor is at zero potential which is used as connection point for the fourth wire. Among all three topologies four-leg (4L) is give better control over neutral current due to four-leg. In this paper three-phase four-wire based on four-leg (4L) shunt inverter topology [24], is shown in Fig. 11.

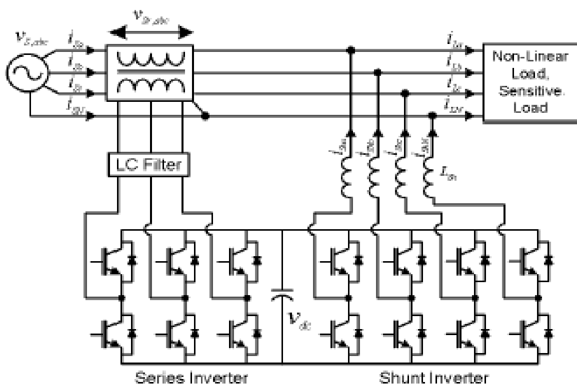

Figure 10 : Three-phase Four-wire (3P4W) UPQC based on Four-leg (4L) shunt inverter topology

The comparison of single-phase UPQC and three- phase UPQC is given in TABLE-2 which gives detailed information about both the sources.

Table 2 : Comparison between Single-phase UPQC and Three-phase UPQC

Single-phase UPQC (1P UPQC)	Three-phase UPQC (3P UPQC)
1. Single-phase UPQC is possible in single-phase two-wire (1P2W)	1. Three-phase UPQC is possible in three-phase three-wire or three-phase four-wire (3P3W or 3P4W)
2. Single-phase UPQC is further classified on: (i) Two H-bridge (ii) 3-Leg topology (iii) Half Bridge	2. Three-phase four-wire UPQC is further classified on: (i) Four-Leg (ii) Split Capacitor (iii) Three-H Bridge
3. In single-phase system load reactive current, current harmonics are major problems	3.- In three-phase three wire system apart from reactive current, current harmonics additional problem is current Unbalance. In three phase four-wire system additional neutral current problem
4. Voltage related power quality problems are similar for both single and three phase system except voltage unbalance compensation is not required in single-phase system	4. Voltage related power quality problems are similar for both single and three phase system except voltage unbalance com-pensation is required in three-phase system

There are various types of configurations of UPQC is given in above classification. Fig. 7 to 11 all are represents right shunt UPQC (UPQC-R) and when in Fig. 7 to 11 shunt inverter is located in left at that time it is called left shunt UPQC (UPQC-L). Among this two configurations UPQC-R is commonly used because current flow through series transformer is mostly sinusoidal. The UPQC-L is rarely used due to interference between shunt inverter and passive filters.

First, the comparison between Interline UPQC (UPQC-I) and Multi-converter UPQC (UPQC-MC) [23] is given in TABLE-3.

Table 3 : Comparison between Interline UPQC and Multi- converter UPQC

Interline UPQC (UPQC-I)	Multi-converter UPQC (UPQC-MC)
1. In Interline UPQC two inverters are connected between two distribution feeders.	1. In UPQC-MC third converter is added to support dc bus.
2. One inverter is connected in series with one feeder while other inverter is connected in shunt with other feeder.	2. The third converter is connected either series or parallel with feeder.
3. UPQC-I can control and	3. It can control and

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manage flow of real power between two feeders.	manage flow of real power between multi feeders.

Second, the comparison between Modular UPQC (UPQC-MD) and Multi-level UPQC (UPQC-ML) [20], [26], [27] is given in TABLE-4.

Table 4 : Comparison between Modular UPQC and Multi-level UPQC

Modular UPQC (UPQC- MD)	Multi-level UPQC (UPQC-ML)
1. In UPQC-MD several H-bridge modules are connected in cascade in each phase.	1. UPQC-ML is based on 3- level neutral point clamped topology.
2. The H-bridge modules for shunt inverter is connected in series through multi-winding transformer, while, series inverter is connected in series with using series transformer.	2. In UPQC-ML three-level topology require double semiconductor switches.
3. UPQC-MD can be useful to achieve higher power levels.	3. UPQC-ML can also be useful to achieve higher power levels.

Third, the comparison between Distributed UPQC (UPQC-D) and Distributed Generator Integrated UPQC (UPQC-DG) [14] [16] [19] [21], is given in TABLE-5.

Table 5 : Comparison between UPQC-D & UPQC-DG

Distributed UPQC (UPQC-D)	Distributed Generator Integrated UPQC (UPQC-DG)
1. UPQC-D topology is also known as 3P3W to 3P4W Distributed UPQC because 3P-4W system is realized by using 3P3W system.	1. The UPQC can be integrated with one or several DG systems which are nown as UPQC-DG.
2. In UPQC-D system the neutral of series transformer is used as neutral of 3P4W system.	2. The output of DG system is connected to dc bus of UPQC to compensate voltage and current related problems.
3. Fourth leg is added to 3P 4WUPQC to compensate neutral current flowing towards transformer neutral point.	3. In UPQC-DG battery can be added at dc bus which is used as stored power and used as backup which give benefit for removing voltage interruption.

Finally, the classification is based on voltage sag compensation is given in this section. There are mainly four methods to compensate voltage sag in UPQC based applications, The comparison between Active Power Control (UPQC-P) and Reactive Power Control (UPQC-Q) is given in TABLE-6.

Table 6 : Comparison between Active Power Control and Reactive Power Control

Active Power Control (UPQC-P)	Reactive Power Control (UPQC-Q)
1. The voltage sag is mitigated by injecting active power through series inverter of UPQC.	1. The voltage sag is mitigated by injecting reactive power through series inverter of UPQC.
2. In Active Power Control P is referred as active power.	2. In Reactive Power Control Q is referred as reactive power.
3. To compensate equal percentage of sag UPQC-P requires smaller magnitude of series injection voltage compared to UPQC-Q.	3.To compensate equal percentage of sag UPQC-Q requires larger magnitude of series injection voltage compared to UPQC-P.

The comparison between Minimum VA Loading (UPQC-VAmin) and Active-Reactive Power Control (UPQC-S) [29],[30], [31], is given in TABLE-7.

Table 7 : Comparison between Minimum VA loading and Active & Reactive Power Control

Minimum VA loading (UPQC-VAmin)	Active & Reactive Power Control (UPQC-S)
1. This method is used which is injected certain optimal angle with respect to source current.	1. In UPQC-S the series inverter is delivered both active and reactive power.
2. The series voltage injection and the current drawn by shunt inverter must need for determining Minimum VA loading of UPQC.	2. The series inverter of UPQC-S perform voltage sag and swell compensation and sharing reactive power with shunt inverter.

V. Control Strategies of UPQC

Control strategy play very important role in system's performance. The control strategy of UPQC may be implemented in three stages:

i. Voltage and current signals are sensed Compensating commands in terms of voltage and current levels are derived.
ii. The gating signals for semiconductor Switches of UPQC are generatedusing PWM, hysteresis or fuzzy logic based control techniques
iii. In the first stage voltage signals are sensed using power transformer or voltage sensor and current signals are sensed using current transformer or current sensor.

In second stage derivation of compensating commands are mainly based on two types of domain methods: (1) Frequency domain methods, and (2) Time domain method. Frequency domain methods, which, is based on the Fast Fourier Transform (FFT) of distorted voltage or current signals to extract compensating commands. This FFT are not popular because of large computation, time and delay.

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Control methods of UPQC in time-domain are based on instantaneous derivation of compensating commands in the form of either voltage or current signals. There are mainly two widely used time domain control techniques of UPQC are:

- The instantaneous active and reactive power or p-q theory, and
- Synchronous reference frame method or d-q theory.

In *p-q* theory instantaneous active and reactive powers are computed, while, the *d-q* theory eals with the current independent of the supply voltage. Both methods transforms voltages and currents from abc frame to stationary reference frame (p-q theory) or synchronously rotating frame (d-q theory) to separate the fundamental and harmonic quantities.

In third stage the gating signals for semiconductor switches of UPQC based on derive compensating commands in terms of voltage or current. Then, these compensating commands are given to PWM, hysteresis or fuzzy logic based control techniques [25] [28].

VI. Technical and Economical Consideration

Technical literature on the APFs can be found since early 1970s [1]. However, the use of UPQC to enhance electric power system quality is reported since mid 1990s [3]. Among the various power quality enhancement devices, STATCOM and few others are commercially available [2]. The technology to develop commercial UPQC system is available today; however, the overall cost and complexity of such a system still imposes some limitations. A 250-kVA prototype developed at C-DAC, Thiruvananthapuram, India [17], is the most viable reported prototype.

The capacity of small and large-scale renewable energy systems based on wind energy, solar energy, etc., installed at distribution as well as transmission levels is increasing significantly. These newly emerging DG systems are imposing new challenges to electrical power industry to accommodate them without violating standard requirements (such as, IEEE 1547, IEEE 519). In terms of power quality, the excessive feeder voltage rise due to reverse power flow from DG system and power system stability is of significant importance. Moreover, most of the DG systems utilize power electronic converters as interfacing device to deliver the generated power to the grid. The switching operation of these systems is contributing as increased harmonic levels both in the grid voltages and currents.

In this paper, several UPQC configurations and topologies have been discussed. Among these configurations, UPQC-DG could be the most interesting topology for a renewable energy based power system. This configuration can offer multifunctional options, namely, active power delivery from DG system to grid (normal DG operation), voltage and current related power quality compensation (UPQC operation), and uninterruptible power supply operation. Commercial products have started to appear in the market to increase the renewable energy system connectivity by compensating some of these problems. As the penetration levels of DG system on the existing power system continue to increase, the utilization of active compensating technologies (such as, flexible ac transmission system devices and APFs) is expected to increase gradually.

VII. Conclusion

The power quality problems in distribution systems are not new but customer awareness of these problems increased recently. It is very difficult to maintain electric power quality at acceptable limits. One modern and very promising solution that deals with both load current and supply voltage imperfections is the Unified Power Quality Conditioner (UPQC). This paper presented a review on the UPQC as a tool to enhance the electric power quality at distribution level. The UPQC is able to compensate supply voltage power quality issues such as, sags, swells, unbalance, flicker, harmonics, and for load current power quality problems such as, harmonics, unbalance, reactive current and neutral current. Among all these configurations, UPQC-DG and UPQC-ML are the most vital topologies to achieve better reliability and power quality at higher power rating of the system. Therefore with the help of these topologies can meet required load demand in future, increase the production in industries and increase the economy of the country.

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- Two Column with Equal Column with of 3.38 and Gaping of .2
- First Character must be three lines Drop capped.
- Paragraph before Spacing of 1 pt and After of 0 pt.
- Line Spacing of 1 pt
- Large Images must be in One Column
- Numbering of First Main Headings (Heading 1) must be in Roman Letters, Capital Letter, and Font Size of 10.
- Numbering of Second Main Headings (Heading 2) must be in Alphabets, Italic, and Font Size of 10.

You can use your own standard format also.
Author Guidelines:

1. General,

2. Ethical Guidelines,

3. Submission of Manuscripts,

4. Manuscript's Category,

5. Structure and Format of Manuscript,

6. After Acceptance.

1. GENERAL

Before submitting your research paper, one is advised to go through the details as mentioned in following heads. It will be beneficial, while peer reviewer justify your paper for publication.

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Complete support for both authors and co-author is provided.

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Original research paper: Such papers are reports of high-level significant original research work.

Review papers: These are concise, significant but helpful and decisive topics for young researchers.

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Papers: These are reports of significant research (typically less than 7000 words equivalent, including tables, figures, references), and comprise:

(a)Title should be relevant and commensurate with the theme of the paper.

(b) A brief Summary, "Abstract" (less than 150 words) containing the major results and conclusions.

(c) Up to ten keywords, that precisely identifies the paper's subject, purpose, and focus.

(d) An Introduction, giving necessary background excluding subheadings; objectives must be clearly declared.

(e) Resources and techniques with sufficient complete experimental details (wherever possible by reference) to permit repetition; sources of information must be given and numerical methods must be specified by reference, unless non-standard.

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(h) Brief Acknowledgements.

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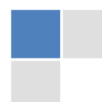

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Standard Usage, Abbreviations, and Units: Spelling and hyphenation should be conventional to The Concise Oxford English Dictionary. Statistics and measurements should at all times be given in figures, e.g. 16 min, except for when the number begins a sentence. When the number does not refer to a unit of measurement it should be spelt in full unless, it is 160 or greater.

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- One should avoid outdated words.

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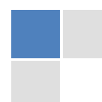

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1. Choosing the topic: In most cases, the topic is searched by the interest of author but it can be also suggested by the guides. You can have several topics and then you can judge that in which topic or subject you are finding yourself most comfortable. This can be done by asking several questions to yourself, like Will I be able to carry our search in this area? Will I find all necessary recourses to accomplish the search? Will I be able to find all information in this field area? If the answer of these types of questions will be "Yes" then you can choose that topic. In most of the cases, you may have to conduct the surveys and have to visit several places because this field is related to Computer Science and Information Technology. Also, you may have to do a lot of work to find all rise and falls regarding the various data of that subject. Sometimes, detailed information plays a vital role, instead of short information.

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24. Never copy others' work: Never copy others' work and give it your name because if evaluator has seen it anywhere you will be in trouble.

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26. Go for seminars: Attend seminars if the topic is relevant to your research area. Utilize all your resources.

27. Refresh your mind after intervals: Try to give rest to your mind by listening to soft music or by sleeping in intervals. This will also improve your memory.

28. Make colleagues: Always try to make colleagues. No matter how sharper or intelligent you are, if you make colleagues you can have several ideas, which will be helpful for your research.

29. Think technically: Always think technically. If anything happens, then search its reasons, its benefits, and demerits.

30. Think and then print: When you will go to print your paper, notice that tables are not be split, headings are not detached from their descriptions, and page sequence is maintained.

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33. Report concluded results: Use concluded results. From raw data, filter the results and then conclude your studies based on measurements and observations taken. Significant figures and appropriate number of decimal places should be used. Parenthetical remarks are prohibitive. Proofread carefully at final stage. In the end give outline to your arguments. Spot out perspectives of further study of this subject. Justify your conclusion by at the bottom of them with sufficient justifications and examples.

34. After conclusion: Once you have concluded your research, the next most important step is to present your findings. Presentation is extremely important as it is the definite medium though which your research is going to be in print to the rest of the crowd. Care should be taken to categorize your thoughts well and present them in a logical and neat manner. A good quality research paper format is essential because it serves to highlight your research paper and bring to light all necessary aspects in your research.

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- Write your paper in the form, which is presented in the guidelines using the template.
- Please note the criterion for grading the final paper by peer-reviewers.

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· Keep on paying attention on the research topic of the paper

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· Present your points in sound order

· Use present tense to report well accepted

· Use past tense to describe specific results

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- Fundamental goal
- To the point depiction of the research
- Consequences, including definite statistics - if the consequences are quantitative in nature, account quantitative data; results of any numerical analysis should be reported
- Significant conclusions or questions that track from the research(es)

Approach:

- Single section, and succinct
- As a outline of job done, it is always written in past tense
- A conceptual should situate on its own, and not submit to any other part of the paper such as a form or table
- Center on shortening results - bound background information to a verdict or two, if completely necessary
- What you account in an conceptual must be regular with what you reported in the manuscript
- Exact spelling, clearness of sentences and phrases, and appropriate reporting of quantities (proper units, important statistics) are just as significant in an abstract as they are anywhere else

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- Shield the model - why did you employ this particular system or method? What is its compensation? You strength remark on its appropriateness from a abstract point of vision as well as point out sensible reasons for using it.
- Present a justification. Status your particular theory (es) or aim(s), and describe the logic that led you to choose them.
- Very for a short time explain the tentative propose and how it skilled the declared objectives.

Approach:

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- Present surroundings information only as desirable in order hold up a situation. The reviewer does not desire to read the whole thing you know about a topic.
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- If use of a definite type of tools.
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- Report the method (not particulars of each process that engaged the same methodology)
- Describe the method entirely
- To be succinct, present methods under headings dedicated to specific dealings or groups of measures
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- If well known procedures were used, account the procedure by name, possibly with reference, and that's all.

Approach:

- It is embarrassed or not possible to use vigorous voice when documenting methods with no using first person, which would focus the reviewer's interest on the researcher rather than the job. As a result when script up the methods most authors use third person passive voice.
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Content

- Sum up your conclusion in text and demonstrate them, if suitable, with figures and tables.
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- Present a background, such as by describing the question that was addressed by creation an exacting study.
- Explain results of control experiments and comprise remarks that are not accessible in a prescribed figure or table, if appropriate.
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What to stay away from

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- Do not present the similar data more than once.
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- Never confuse figures with tables - there is a difference.

Approach

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- Recommendations for detailed papers will offer supplementary suggestions.

Approach:

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References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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