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# AC Characteristics of a Dual Gate Large Area Graphene MOSFET

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**Abstract-** This paper presents a detailed study of RF characteristics together with the high frequency performance of dual gate large area graphene MOSFET. A quasi analytical modeling approach is presented here. To know the RF characteristics of a graphene MOSFET, the transconductance is simulated using small signal equivalent model. Finally the intrinsic top and back gate gain of graphene MOSFET are also shown which are very important figure of merit for RF applications.

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## I. INTRODUCTION

Graphene is a flat monolayer of  $sp^2$  carbon atoms tightly packed into a two-dimensional (2D) honeycomb lattice including a linear energy dispersion relation [1]. Graphene offers many of the advantages such as high carrier mobilities up to  $10 \times 2^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  in substrate supported devices and high saturation velocity [2] [6]. The novel electronic properties of graphene lead to intense research into possible applications of this material in nano scale devices such as dual gate graphene MOSFETs.

There have been studies on designing and fabrication of dual gate graphene MOSFETs. However, the progress in designing and fabricating of G-MOSFETs is at initial stage. In order to fabricate high performance G-MOSFETs, understanding of detailed device modeling and performance evaluations is urgently required. The recent works have been concentrated mostly on the DC characteristics of large area graphene MOSFETs using different approaches. However, there have no significant works on AC characteristics although graphene is predicted to highly attracted material for nano-scale devices.

## II. DEVICE MODEL

A dual gated graphene MOSFET is considered for our work shown in Fig. 1. Graphene grown on metal and transferred to a  $SiO_2$  covered Si wafer is used as the

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channel of the MOSFET. The length and width of the graphene channel are  $5 \mu\text{m}$  and  $1 \text{ m}$  respectively. Here,  $HfO_2$  ( $k=9$ ) is used as top-gate oxide and  $SiO_2$  ( $k=3.9$ ) is used as back-gate oxide [5], [7].

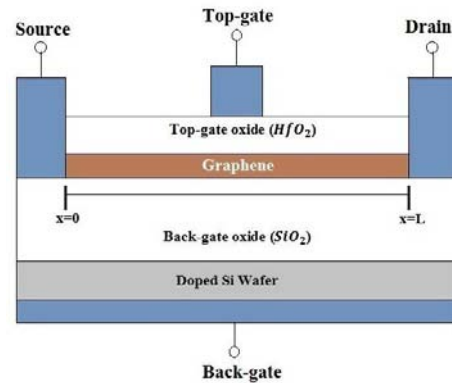


Figure 1 : Cross section of the modeled graphene MOSFET [8]

### a) Channel Charge Calculation

The goal of this work is to model the high-frequency characteristics of these devices. This will be done by calculating the elements of the small-signal equivalent circuit. Before we can deal with these elements we need to know how to calculate the channel charge, since this is essential in order to determine the gate-source and gate-drain capacitances. In general the channel charge  $Q_{ch}$  can be calculated by subtracting the amount of electrons from the amount of holes and multiplying the result by the elementary charge. This can be written as [09].

$$Q_{ch} = qW \int_0^L (p(x) - n(x)) dx \quad (01)$$

To obtain  $Q_{ch}$ , a simple numerical integration is performed using a trapezoidal approximation. The  $x$  dependence of the local hole and electron sheet densities can be translated into a dependence on the local voltage  $V(x)$ . By using this equation [09].

$$\frac{dx}{dV(x)} = \frac{qW_{real}(V(x))\mu}{I_d} + \frac{\mu}{v_{sat}(V(x))} \quad (02)$$

The overall net charge can be expressed using Eqn.01 and the necessary equation of  $Q_{ch}$

$$Q_{ch} = qW \int_0^{V_{ds-int}} [p(V(x)) - n(V(x))] \frac{dx}{dV(x)} dV(x) \quad (03)$$

$$Q_{ch} = \int_0^{V_{ds-int}} [\rho(V(x)) - nV(x)] \left( \frac{qW \rho_{real}(V(x)) \mu}{I_d} + \frac{\mu}{v_{sat}(V(x))} \right) dV(x) \quad (04)$$

It is important to distinguish between p, n and in  $\rho_{real}$  the formula above. If we neglect the minority charge carriers,  $p(V(x)) - n(V(x))$  is equal to  $\rho_{real}$  can be expressed as:

$$p(V(x)) - n(V(x)) \cong - (V_{gs-top} - V(x) - V_{gs-top,0}) \frac{\frac{1}{2} C_{ox-top} C_q}{C_{ox-top} + C_{ox-top} + \frac{1}{2} C_q} - (V_{gs-top} - V(x) - V_{gs-top,0}) \frac{\frac{1}{2} C_{ox-back} C_q}{C_{ox-top} + C_{ox-top} + \frac{1}{2} C_q} \quad (05)$$

The integral to determine  $Q_{ch}$  is solved numerically. We have used the MATLAB simulation. Note that to calculate channel charge as well as small signal parameters the internal voltages have to be used [09].

a) *Small-Signal Equivalent Circuit*

The high-frequency behavior of the transistor can be modeled with a small-signal equivalent circuit [10] as shown in Figure2. The intrinsic transistor is described by the transconductance  $g_m$ , the drain conductance  $g_{ds}$ , the gate-source capacitance  $C_{gs}$ , and the gate-drain capacitance  $C_{gd}$ . Thereby the whole behavior of the device is described by these four elements:  $g_m$ ,  $g_{ds}$ ,  $C_{gs}$  and  $C_{gd}$ . The reason why this is possible is the following. The high-frequency AC signal is thought to be superimposed onto a DC signal, which defines the DC operating point. If the amplitude of the AC signal is small, the nonlinear transistor characteristics can be linearized around the DC operating point. Thus all elements of Fig. 2 are explained in the following as mentioned [09].

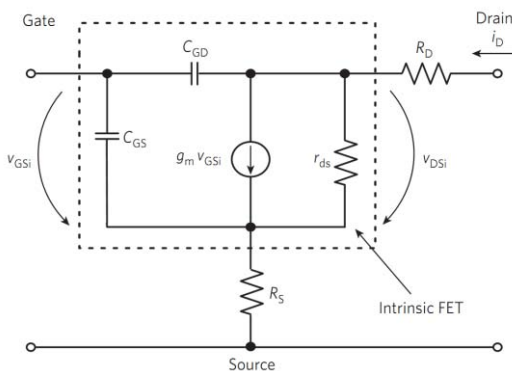


Figure 2 : The small-signal equivalent circuit of a graphene MOSFET

The intrinsic transconductance,  $g_m$ , is related to the internal small-signal gate source and drain– source voltages,  $V_{GSi}$  and  $V_{DSi}$ , whereas the terminal transconductance,  $g_{mt}$ , is related to the applied gate– source and drain–source voltages,  $V_{GS}$  and  $V_{DS}$  [10].

III. TRANSCONDUCTANCE CALCULATION

The transconductance calculation is very important to know the radio-frequency characteristics of a graphene MOSFET. The transconductance is defined as the variation in the drain current caused by a small variation in the gate voltage. They are two types: intrinsic transconductance and drain-conductance.

a) *Intrinsic Transconductance*

The intrinsic transconductance is defined as the change of the drain current  $I_d$  caused by small variations of the internal gate-source voltage  $V_{gs-top-int}$  at a fixed drain source voltage  $V_{ds-int-const}$ , denoted by  $g_m$  [09], [10].

$$g_{m-top} = \left. \frac{dI_d}{dV_{gs-top-int}} \right|_{V_{ds-int}=const} \quad (06)$$

$$g_{m-back} = \left. \frac{dI_d}{dV_{gs-back-int}} \right|_{V_{ds-int}=const} \quad (07)$$

The transconductance due to top-gate voltage ( $g_{m-top}$ ) and the transconductance due to back-gate voltage ( $g_{m-back}$ ) can be evaluated using Eqn. 06 and Eqn.07 clearly. It describes how the output signal (drain current) reacts on changes of the input signal (gate- source-voltage).

b) *Drain Conductance of GFET,  $g_{ds}$*

The drain-source conductance  $g_{ds}$  describes the resistance of the graphene channel, since it is the inverse of  $r_d$ . It is expressed by the variation of the drain current  $I_d$  caused by a change of the internal drain-source voltage  $V_{ds-int}$  at a fixed  $V_{gs-top-int}$ .

$$g_{ds-top} = \left. \frac{dI_d}{dV_{ds-int}} \right|_{V_{gs-top-int}=const} \quad (08)$$

$$g_{ds-back} = \left. \frac{dI_d}{dV_{ds-int}} \right|_{V_{gs-back-int}=const} \quad (09)$$

The drain conductance due to fixed value of top-gate voltage ( $g_{ds-top}$ ) and the drain conductance due to fixed value of back-gate voltage ( $g_{ds-back}$ ) can be evaluated using Eqn.08 and Eqn.09.

#### IV. INTRINSIC CAPACITANCE CALCULATION

The intrinsic capacitance is very necessary to calculate the cut-off frequency and other radiofrequency behaviour of a graphene MOSFET. The mobile channel charge depends on the top-gate voltage  $V_{gs-top-int}$ , the back-gate voltage  $V_{gs-back-int}$  and drain-source voltage  $V_{ds-int}$ . This dependence is modeled by the gate-source capacitance  $C_{gs}$  & the gate-drain capacitance  $C_{gd}$  [09].

##### a) Gate-Source Capacitance, $C_{gs}$

The gate-source capacitance  $C_{gs}$  is defined as the variation in the channel charge  $Q_{ch}$  caused by a small variation in the top-gate voltage  $V_{gs-top-int}$  with a fixed value of drain-source voltage  $V_{ds-int}$ .

$$C_{gs-top} = \left. \frac{dQ_{ch}}{dV_{gs-top-int}} \right|_{V_{ds-int}=const} \quad (10)$$

$$C_{gs-back} = \left. \frac{dQ_{ch}}{dV_{gs-back-int}} \right|_{V_{ds-int}=const} \quad (11)$$

The gate-source capacitance due to top-gate voltage ( $C_{gs-top}$ ) and the gate-source capacitance due to back-gate voltage ( $C_{gs-back}$ ) can be evaluated using Eqn.10 and Eqn.11 clearly.

##### b) Gate-Drain Capacitance, $C_{gd}$

The gate-drain conductance  $C_{gd}$  is defined as the variation in the channel charge  $Q_{ch}$  caused by a small variation in the drain-source voltage  $V_{ds-int}$  with a fixed value of top-gate voltage  $V_{gs-top-int}$ .

$$C_{gd-top} = \left. \frac{dQ_{ch}}{dV_{ds-int}} \right|_{V_{gs-top-int}=const} \quad (12)$$

$$C_{gd-back} = \left. \frac{dQ_{ch}}{dV_{ds-int}} \right|_{V_{gs-back-int}=const} \quad (13)$$

The gate-drain capacitance due to the fixed value of top-gate voltage ( $C_{gd-top}$ ) and the gate-drain capacitance due to the fixed value of back-gate voltage ( $C_{gd-back}$ ) can be evaluated using Eqn.12 and Eqn.13 also.

#### V. INTRINSIC GAIN CALCULATION

Finally, we show an example of projection of the intrinsic gain as a figure of merit commonly used in RF/analog applications. In small signal amplifiers, for instance, the transistor is operated in the ON-state and small RF signals that are to be amplified are

superimposed onto the DC gate-source voltage [41]. Instead, what is needed to push the limits of many analog/RF figures of merit, for instance the cut-off frequency or the intrinsic gain, is an operation region where high trans conductance together with a small output conductance is accomplished. Next, we will give an example on how to use our current-voltage DC model to project an important figure-of-merit (FOM) used in RF/analog applications, namely the intrinsic gain (G).

##### a) Intrinsic Top-Gate Gain, $G_{top}$

The intrinsic top-gate gain  $G_{top}$  which is defined as the ratio of the transconductance  $g_{m-top}$  to the drain-conductance  $g_{ds-top}$  expressed as: Intrinsic top-gate gain,

$$G_{top} = \frac{g_{m-top}}{g_{ds-top}} \quad (14)$$

The top-gate gain ( $G_{top}$ ) is very important in RF/analog applications as well as cut-off frequency.

##### b) Intrinsic Back-Gate Gain, $G_{back}$

The intrinsic back-gate gain  $G_{top}$ , which is defined as the ratio of the trans conductance ( $g_{m-top}$ ) to the drain-conductance ( $g_{ds-top}$ ) expressed as:

Intrinsic back-gate gain,

$$G_{back} = \frac{g_{m-back}}{g_{ds-back}} \quad (15)$$

#### VI. RESULTS AND DISCUSSION

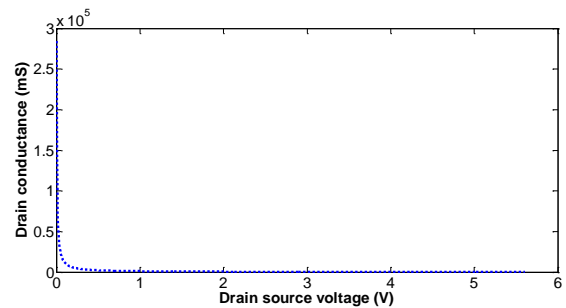


Figure 3 : Drain transconductance as a function of Drain Source voltage of a graphene MOSFET

Fig. 3. shows the variation of drain transconductance as a function of drain-source voltage of graphene MOSFET

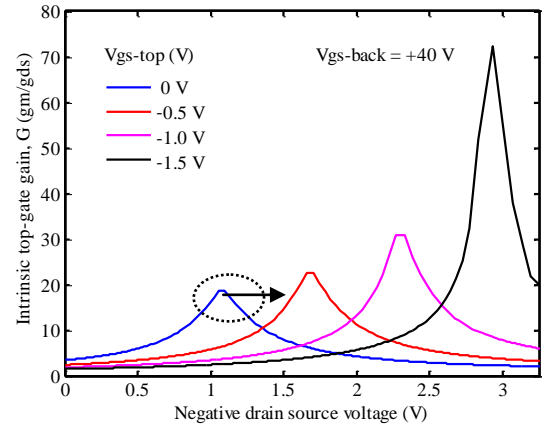
Figure 4(a) shows the intrinsic peak top-gate gain ( $G_{top}$ ) for different top-gate voltages. The intrinsic peak top-gate gain ( $G_{top}$ ) is increasing with the increase of top-gate voltages at  $V_{gs-back} = +40V$ . At a top-gate voltage, ( $G_{top}$ ) = 1.5V, the intrinsic peak top-gate gain is found. approximately 73 which is very important figure of merit for high speed devices. Also the peak

point of the top-gate gain ( $G_{top}$ ) shifts towards right with increasing  $V_{gs-top}$ .

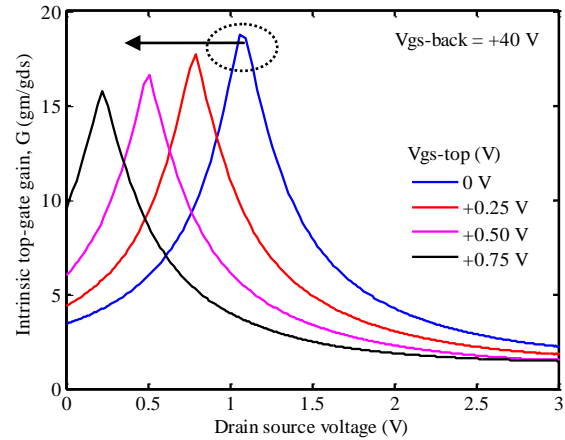
Figure 4(b) shows the intrinsic peak top-gate gain ( $G_{top}$ ) for different positive gate bias condition. We have found  $G_{top} \approx 15.79, 16.60, 17.69$  and  $18.77$  as a function of  $V_{ds}$  for top-gate voltages  $+0.75V, +0.50V, +0.25V$  and  $0.0V$  respectively with  $V_{gs-back} = +40V$ . There has no significant change of top-gate gain ( $G_{top}$ ) shown in Fig.4 (b) except the shifting of the peak point towards left.

The effect of both positive and negative gate bias on intrinsic peak top-gate gain ( $G_{top}$ ) is shown in Fig. 4(c) which shows the significant increase in intrinsic peak  $G_{top}$  in case of negative gate bias in comparison with positive gate bias.

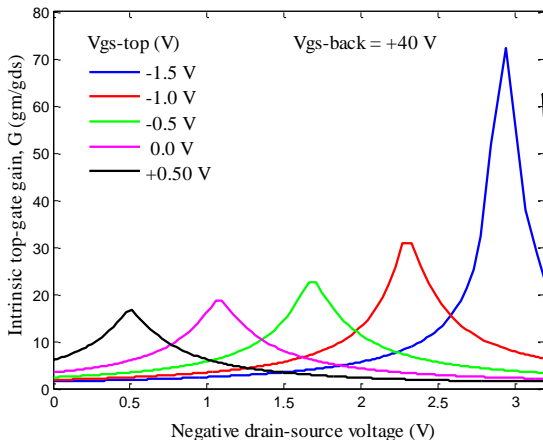
Fig. 4(d) shows the variation of intrinsic peak back-gate gain ( $G_{back}$ ) with drain-source voltage for different positive back-gate voltages. At a back-gate voltage,  $V_{gs-back} = +40V$ , the highest peak  $G_{back} \approx 73$  is obtained and shifts towards left with increasing  $V_{gs-back}$  positively.



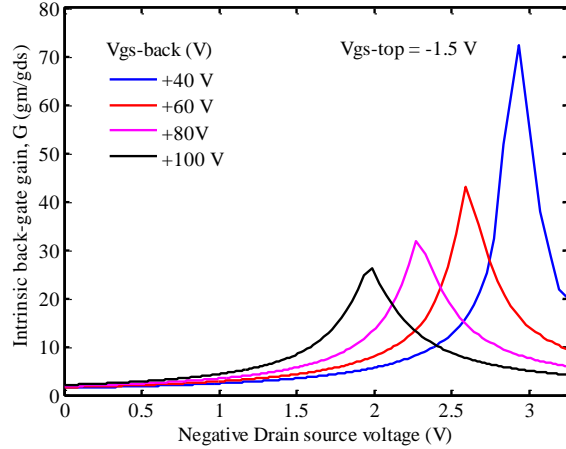
(a)



(b)



(c)



(d)

Figure 4 : (a) Intrinsic top-gate gain ( $G_{top} = gm/gds$ ) as a function of drain source voltage  $V_{ds}$  at  $V_{gs-top} = 0V, -0.50V, -1.0V$  and  $-1.5V$  with  $V_{gs-back} = +40V$ . (b) Intrinsic top-gate gain ( $G_{top} = gm/gds$ ) as a function of drain source voltage  $V_{ds}$  at  $V_{gs-top} = 0.0V, +0.25V, +0.50V$  and  $+0.75V$  with  $V_{gs-back} = +40V$ . (c) Intrinsic top-gate gain ( $G_{top} = gm/gds$ ) as a function of drain source voltage  $V_{ds}$  at  $V_{gs-top} = -1.50V, -1.0V, -0.5V, 0.0V$  and  $+0.50V$  with  $V_{gs-back} = +40V$ . (d) Intrinsic back-gate gain ( $G_{back} = gm/gds$ ) as a function of drain source voltage  $V_{ds}$  at  $V_{gs-back} = 40V, +60V, +80V$  and  $+100V$  with  $V_{gs-top} = -1.5V$ .

## VII. CONCLUSION

In this paper, the AC characteristics of a dual gated Graphene MOSFET are studied using analytical approach. The drain transconductance of the device is computed. We have simulated the top and back gate gain as a function of drain to source voltage. The resulting high intrinsic top gate gain 73 which is promising.

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