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Design of a Novel Low-Power SRAM Column

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I. Introduction

Static random access memory (SRAM) is widely used in present day logic LSIs. SRAM memory cell array normally occupies around 40% of the chip area and hence affects the operating speed, power, supply voltage, and chip size. Therefore, a good design of SRAM cell and SRAM cell array is essential. This paper present a novel SRAM column architecture using standard 7nm process technology provided by the predictive technology model (PTM) [9].Various kinds of SRAM memory cell have been proposed, developed, and used. To resolve the problem of switching capacitances at the word line clocked transmission gate adiabatic SRAM has been designed [1], this topology uses the bootstrapped NMOS transistors and CMOS latch structure to recover the charge of large switching capacitances on word-line, write bit line, and sense amplified lines and so on. Since this circuit uses clocked transmission gate logic as well as sampling of the input signals so it may be slower comparatively, also it has floating nodes for some period of time which may not be desired for the memory array, this design also uses sub array selection signal with some delays which is again not desirable; all these issues has been taken care for the presented design. Now the variations in the threshold voltage (Vt) for the transistors of the cell may create some undesired effects which are again resolved by controlling the memory cell-power line (MCPL) and word-line voltage [2],this design provide low current operation with negligible area penalty; in this design the word line voltage is changed stepwise which may effect in slower operation of the memory array; furthermore in these circuits, the memory cell power line voltage is almost equal to Vdd, which is not very effective for resolving the Vt variation problem. The MCPL cannot be decreased to ground because the data of the unselected word line (WL) vanish if the MCPL set to ground, here the data vanishes because the MCPL is shared with different loads. Also in the conventional six transistors (6-T) SRAM cell [6] there will be voltage drop problem at the word line access which increases the overall power dissipation of the cell; also there may be a short circuit current flowing through the circuit. All these problems have been taken care for this novel design.

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II. Proposed Sram Column

Fig.1 shows the design of a proposed SRAM column. It includes precharging circuit (mo & m1) from where the precharged voltage is generated and this equalizes the bit and bit-bar lines with equal potential, storage cell (m2 – m7) is used to store the data [either 0 or 1] in the memory cell, sense amplifier (m8 – m12) is used during reading operation of the required data from the memory array and column select circuit (m13 & m14) used to select the corresponding column from the memory array. Working of this design can be understood in the following mode viz. i) Read, ii) Write.

For the first case when a read control signal is given to the column, it first selects the respective column, then the precharging circuit is activated and the voltage Vp is transferred to the bit and bit-bar lines which makes both the lines at equal potential. After that the word lines (WL and WLB) are activated which enable the transfer of stored values on the memory cell (either 0 or 1) to the bit lines resulting in one of the bit line go high and the other bit lines go low. Finally the sense amplifier is enabled which senses the potential difference between bit and bit-bar lines and transmits the signals to the bi-directional input-output data lines.

For write operation a write signal is applied to select the respective column without activating the precharging circuit. The data (either 0 or 1) to be entered is supplied by bi-directional input-output data lines to the bit lines. The word line is then activated to store the required information into the cell. Note that for efficient read or write operation the transistor sizing should be appropriate otherwise it may leads to wrong data read or write. For the standby operation word line (WL) voltage is not applied to the cell hence the stored information remains latched and the inverters connected back to back reinforce each other and maintain the required data into the cell.

The proposed SRAM column includes two transmission gates (TG-1 and TG-2) in place of pass transistors for word line access transistors, the use of pass transistors as word line shows the voltage drop problem for the cell but in case of transmission gates there is negligible voltage drop. Also as there is a static current flow through the cell during memory cell operation (especially when writing the data to the cell), so to restrict the short circuit current the NMOS switch (m6) is used at the bottom of the cell which turns on during memory cell operation and shows high resistance to the current flow. The proposed SRAM column was simulated using HSPICE simulator. The design parameters (or process parameters) for the column was taken from PTM and the technology used here is standard 7nm. The Vdd was 0.8 V. The trapezoidal clock pulse was used for the word line access. The simulation results for reading and writing of the SRAM column are shown in fig.2 and fig.3 respectively.

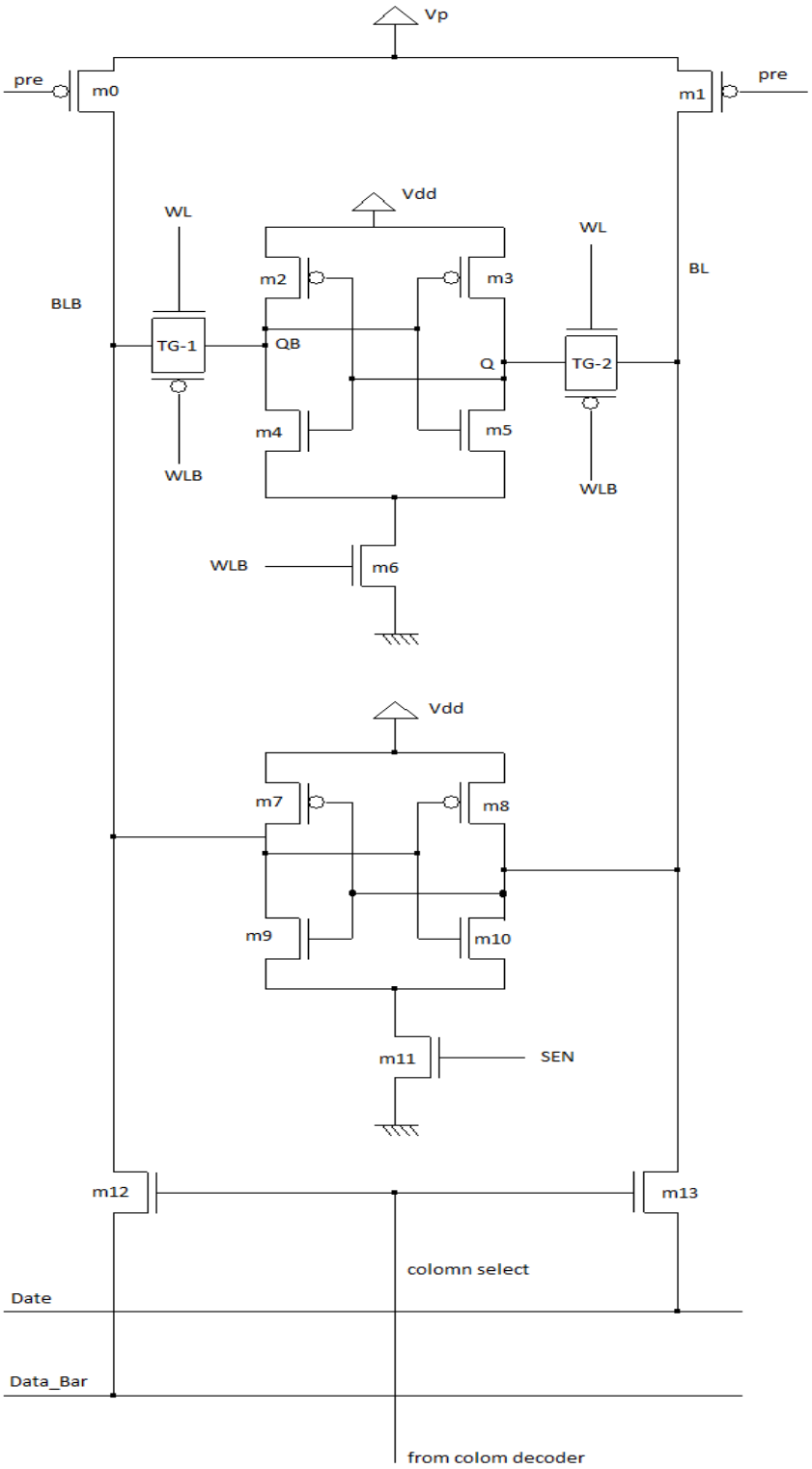

Figure 1 : Proposed SRAM Column

III. Simulation Results

Fig.2 shows the simulated waveforms of proposed SRAM column during read cycle; furthermore fig.2 (a) shows the waveform of precharge signal (Vp and pre) which is transferred in equalized manner to the bit and bit-bar (BL and BLB) lines of the column. Also fig.2 (b) shows the waveform of word line (WL and WLB) which is trapezoidal in nature, after the arrival of word line signal the stored data will be transferred to the bit lines which makes one bit line to go high and other to go low depending on the data stored, and then after column select (c_sel) and sense enable (sen) signals the values at the bit and bit-bar lines will be read out and can be seen at the bidirectional data and data-bar lines.

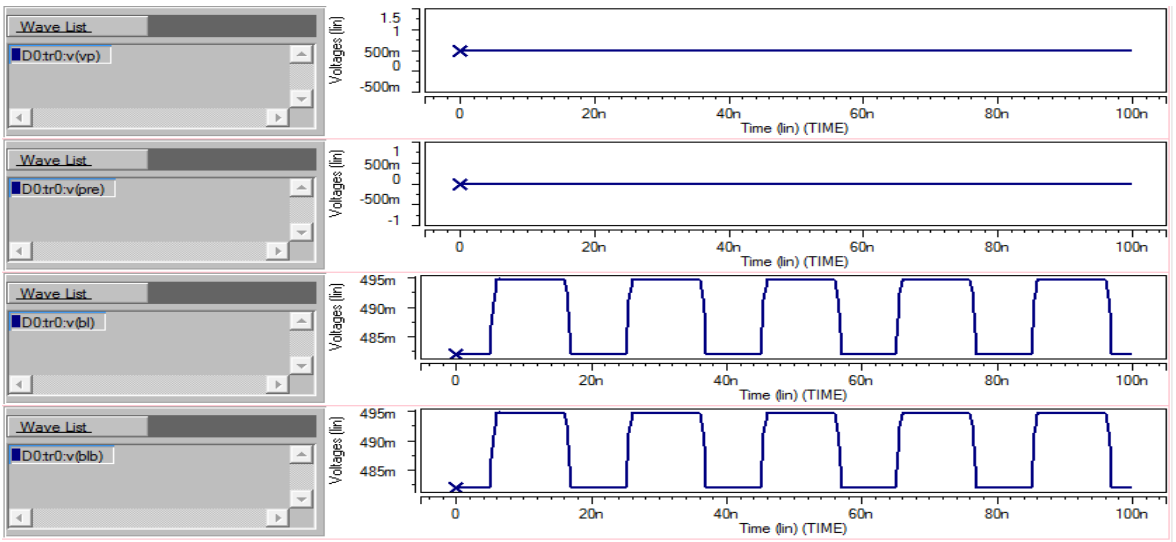

Figure 2 : (a)

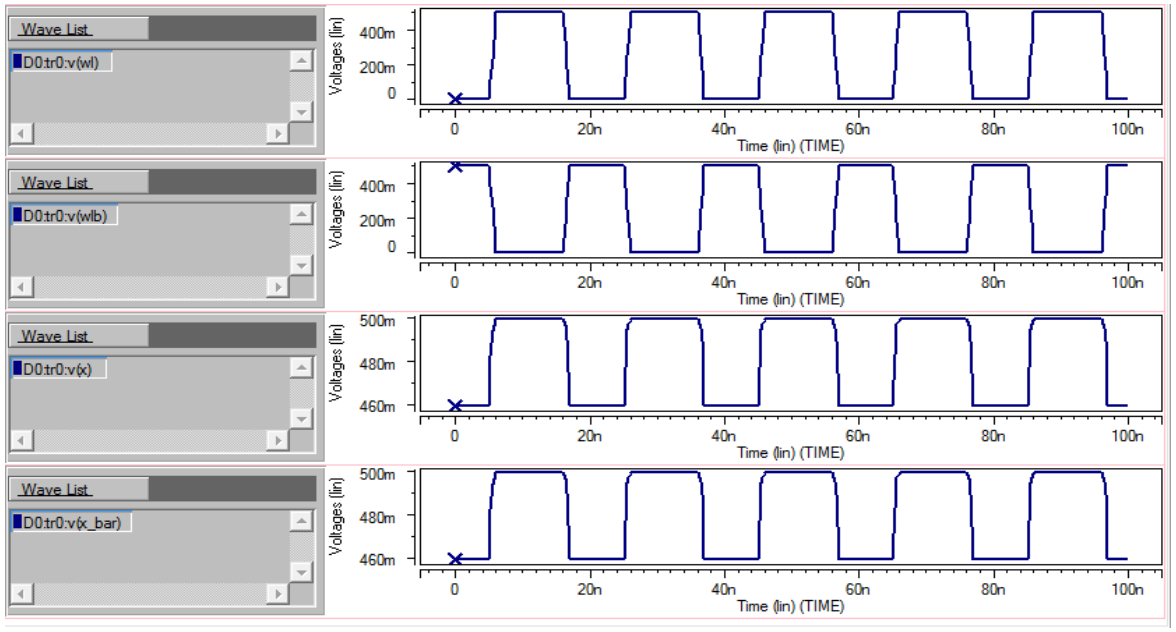

Figure 2 : (b)

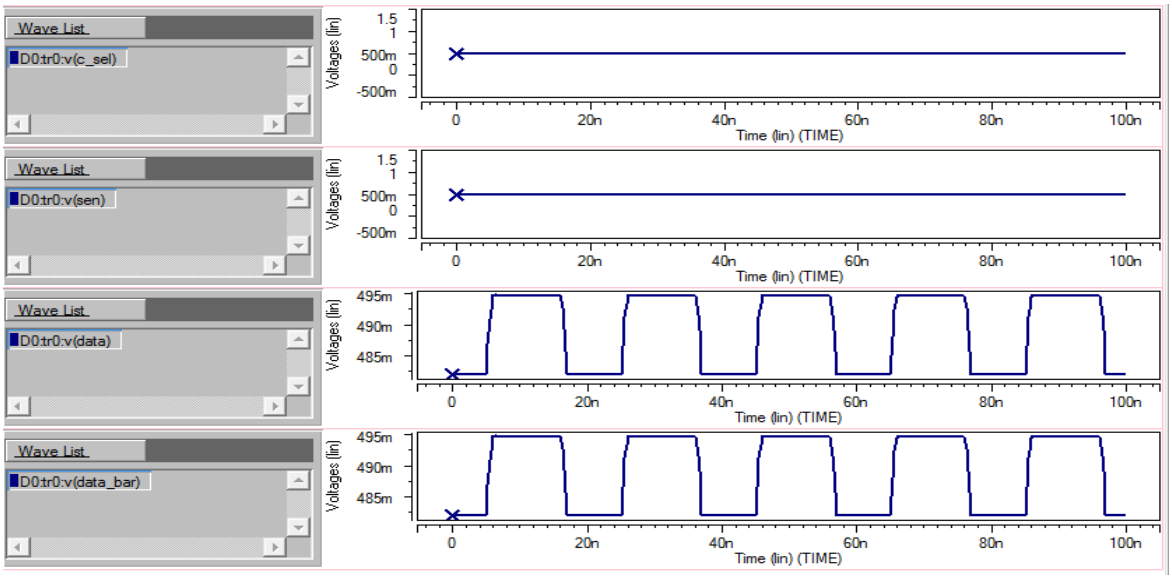

Figure 2 : (c)

Figure 2 : Simulated waveforms during read operation

Fig.3 shows the simulated waveforms of proposed SRAM column during write cycle; fig.3 (a) shows the required data which is to be stored into the cell and the respective column to be selected. Fig.3 (b) shows the bit and bit-bar potentials after transferring the data by selecting the desired column. The stored data (x and xb) can be easily seen after arrival of word line signal in fig.3 (c).

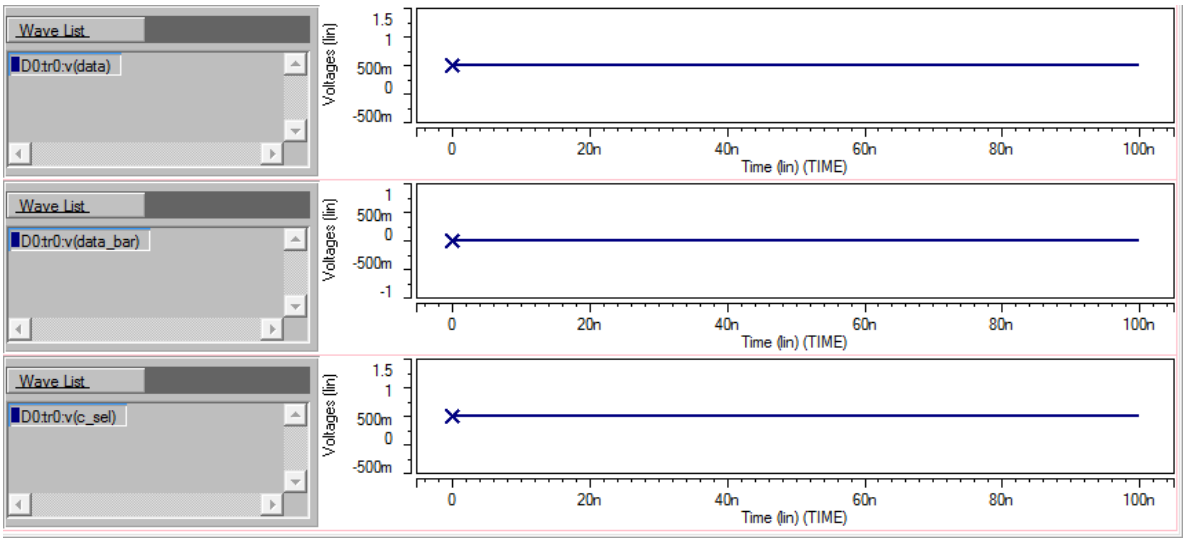

Figure 3 : (a)

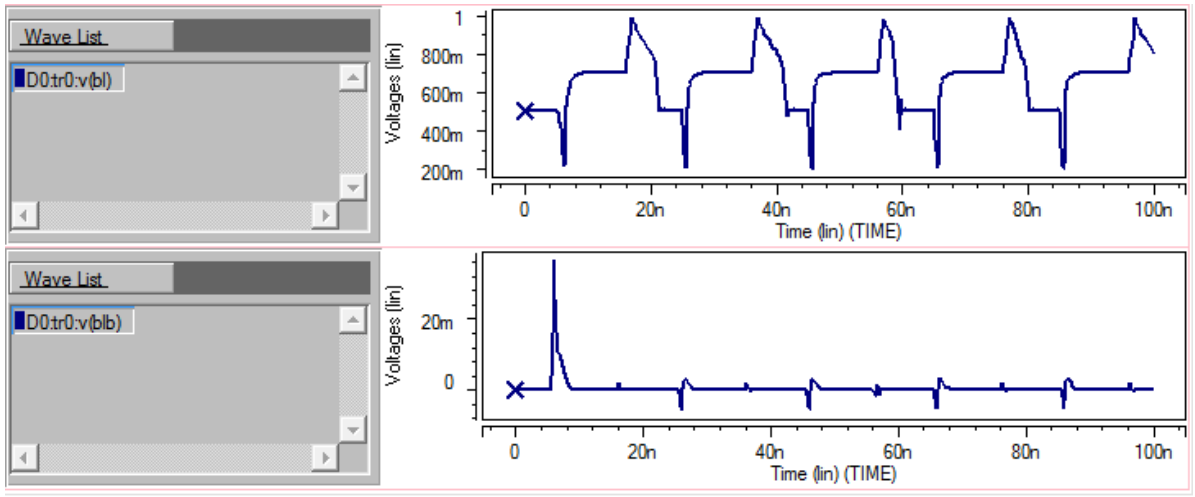

Figure 3 : (b)

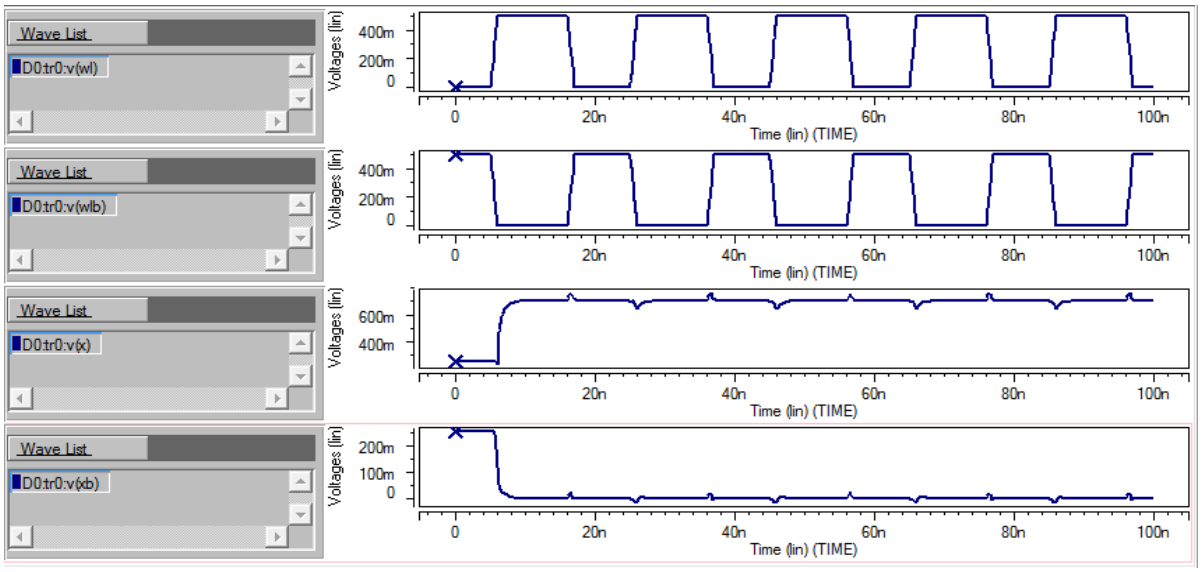

Figure 3 : (c)

Figure 3 : Simulated waveforms during write operation

The values of power dissipation during various operations of the proposed SRAM column are listed in table-1 as shown below.

Table 1

Proposed SRAM Column	Average Power Consumed
During Read Operation	$1.45 * 10^{-4}$ W
During Write Operation	$4.70 * 10^{-5}$ W

IV. Conclusion

In summary, a new SRAM column was designed by using standard 7nm process models from PTM. In the design transmission gates are used in place of pass transistors to rectify the voltage drop problem, an additional NMOS switch is also used at the bottom of the cell instead connecting the cell directly to the ground this helps in reducing the static current flow through the cell during memory operation especially during writing the data to the memory cell. Trapezoidal wave pulses are used at the word line access signal which helps in reducing the power of the memory cell. Finally, by observing the output files generated by HSPICE it was concluded that the proposed SRAM column consumes low power and functioning correctly.

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