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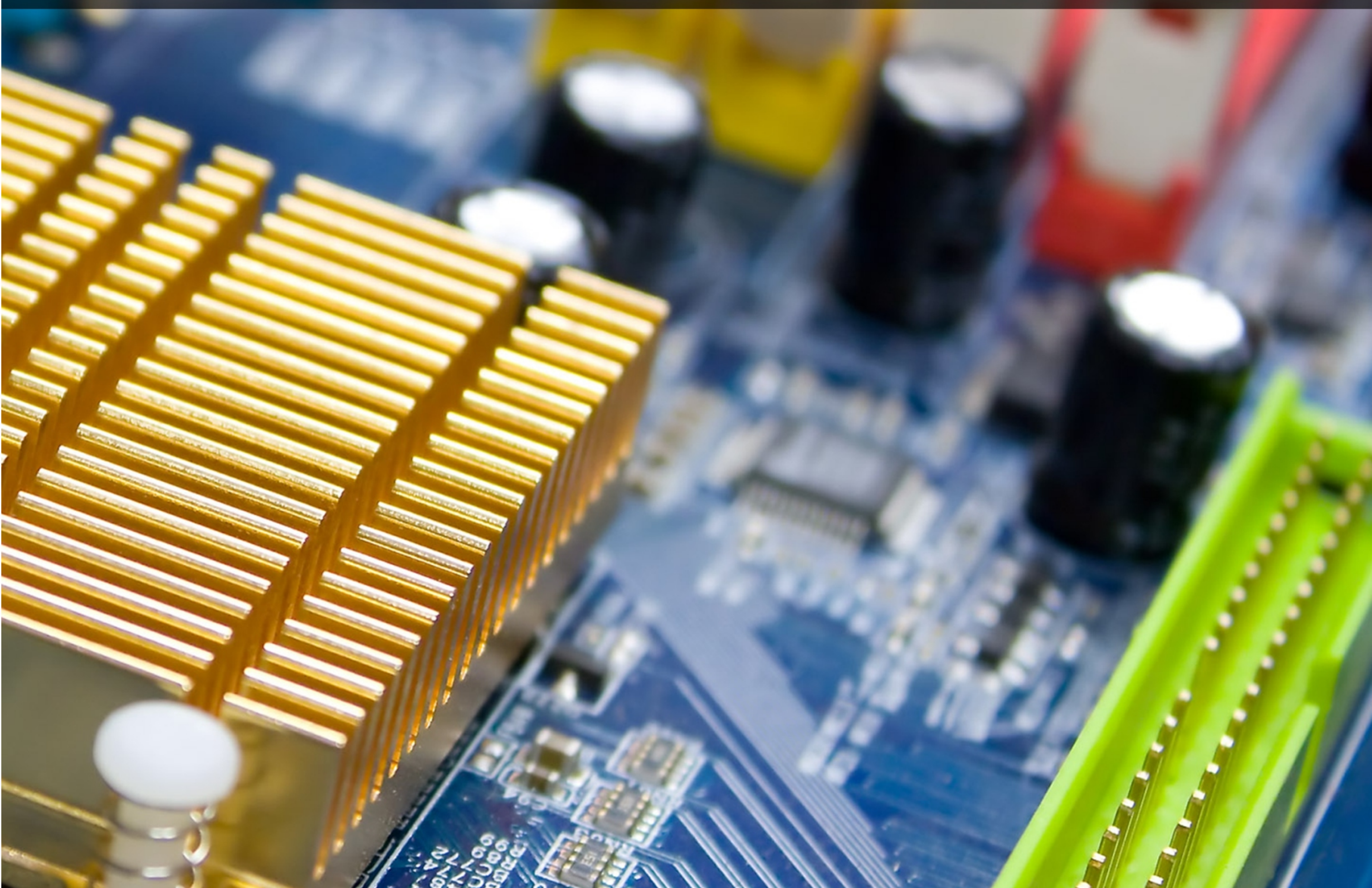

Power System Stability

Improvement of Power System

Highlights

FPGA based Solution

Cascade Proportional Integral

Discovering Thoughts, Inventing Future

VOLUME 14 ISSUE 2 VERSION 1.0

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Design of STATCOM for Power System Stability Improvement

By Sohel Hossain, Atiqur Rahman Khan & Jannat-E-Noor
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Abstract- This paper presents the model of a STATCOM which is controlled externally by a newly designed Power Oscillation Controller (POC) for the improvements of power system stability and damping effect of an on line power system. The proposed POC consists of two controllers (PID & POD). PID parameters has been optimized by Zigler Necles close loop tuning method. Machine excitation has been controller by using excitation controller as required. Both single phase and three phase faults has been considered in the research. In this paper, A power system network is considered which is simulated in the phasor simulation method & the network is simulated in three steps; without STATCOM, With STATCOM but no externally controlled, STATCOM with Power Oscillation Controller (POC). Simulation result shows that without STATCOM, the system parameters becomes unstable during faults. When STATCOM is imposed in the network, then system parameters becomes stable. Again, when STATCOM is controlled externally by POC controllers, then system voltage & power becomes stable in faster way then without controller. It has been observed that the STATCOM ratings are only 20 MVA with controllers and 200 MVA without controllers. So, STATCOM with POC controllers are more effective to enhance the voltage stability and increases power transmission capacity of a power system .So STATCOM with POC & excitation controllers, the system performance is greatly enhanced.

Keywords: STATCOM, voltage regulator, power system controller, PID, POD, power oscillation controller (POC), MATLAB simulink.

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Design of STATCOM for Power System Stability Improvement

Sohel Hossain [α], Atiqur Rahman Khan [σ] & Jannat-E-Noor [ρ]

Abstract- This paper presents the model of a STATCOM which is controlled externally by a newly designed Power Oscillation Controller (POC) for the improvements of power system stability and damping effect of an on line power system. The proposed POC consists of two controllers (PID & POD). PID parameters has been optimized by Zigler Necles close loop tuning method. Machine excitation has been controller by using excitation controller as required. Both single phase and three phase faults has been considered in the research. In this paper, A power system network is considered which is simulated in the phasor simulation method & the network is simulated in three steps; without STATCOM, With STATCOM but no externally controlled, STATCOM with Power Oscillation Controller (POC). Simulation result shows that without STATCOM, the system parameters becomes unstable during faults. When STATCOM is imposed in the network, then system parameters becomes stable. Again, when STATCOM is controlled externally by POC controllers, then system voltage & power becomes stable in faster way then without controller. It has been observed that the STATCOM ratings are only 20 MVA with controllers and 200 MVA without controllers. So, STATCOM with POC controllers are more effective to enhance the voltage stability and increases power transmission capacity of a power system .So STATCOM with POC & excitation controllers, the system performance is greatly enhanced.

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I. Introduction

Power system stability improvements is very important for large scale system. The AC power transmission system has diverse limits, classified as static limits and dynamic limits[1- 2].Traditionally, fixed or mechanically switched shunt and series capacitors, reactors and synchronous generators were being used to enhance same types of stability augmentation[3]. For many reasons desired performance was being unable to achieve effectively. A STATCOM is an electrical device for providing fast-acting reactive power compensation on high voltage transmission networks and it can contribute to improve the voltage profiles in the transient state and therefore, it can improve the qualities and performances of the electric services[3]. An STATCOM can be controlled externally by using properly designed different types of controllers which can improve voltage stability of a large scale power system. In previous study Authors has d signed a PID controller which has tuned by Triple Integral Differential (TID) tuning method [4]. However, in this study, With a view to get better performance, A new Power Oscillation Controller (POC) has been designed & proposed for STATCOM to injects Vqref externally for the improvement of power system stability. Therefore, thyristor based STATCOM with POC controllers has been used to improve the performance of power system.

II. Control Concept of STATCOM

A static synchronous compensator (STATCOM), also known as a "static synchronous condenser" ("STATCON"), is a regulating device used on alternating current electricity transmission networks. It is based on a power electronics voltage-source converter and can act as either a source or sink of reactive AC power to an electricity network. If connected to a source of power it can also provide active AC power. It is a member of the FACTS family of devices. Usually a STATCOM is installed to support electricity networks that have a poor power factor and often poor voltage regulation. A STATCOM is a voltage source converter (VSC)-based device, with the voltage source behind a reactor. The voltage source is created from a DC capacitor and therefore a STATCOM has very little active power capability. However, its active power capability can be increased if a suitable energy storage device is connected across the DC capacitor. The reactive power at the terminals of the STATCOM depends on the amplitude of the voltage source [5].diagram.

III. Power System Model

This example described in this section illustrates modeling of a simple transmission system containing 2- hydraulic power plants [Fig.1]. STATCOM has been used to improve transient stability and power system oscillations damping. The phasor simulation method can be used.

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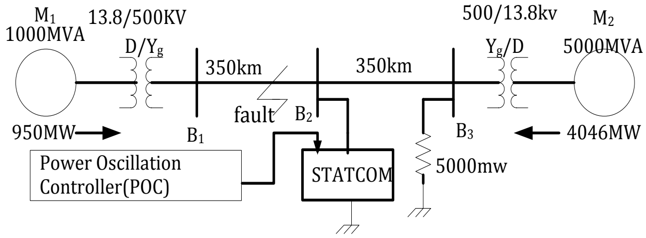

Figure 1 : Single line diagram of 2-machine power system

A single line diagram represents a simple 500 kV transmission system is shown in Fig.1 [6].In the proposed plan because resistor is low cost than potential transformer. A 1000 MW hydraulic generation plant (M1) is connected to a load centre through a long 500 kV, total 700km transmission line. A 5000 MW of resistive load is modelled as the load centre. The remote 1000 MVA plant and a local generation of 5000 MVA (plant M2) feed the load. A load flow has been performed on this system with plant M1 generating 950 MW so that plant M2 produces4046 MW. The line carries 944 MW which is close to its surge impedance loading (SIL = 977 MW). To maintain system stability after faults, the transmission line is shunt compensated at its centre by a 200MVAR STATCOM [Fig.2].The STATCOM does not have any controller unit. Machine & STATCOM parameters has been taken from reference [5].The complete simulink model of STATCOM with power system controller is shown in Fig.4. To maintain system stability after faults, the transmission line is shunt compensated at its centre by a 200MVAR STATCOM with power system controller. The two machines are equipped with a hydraulic turbine and governor (HTG) [Fig.2], excitation system. Any disturbances that occur in power systems due to fault, can result in inducing electromechanical oscillations of the electrical generators. Such oscillating swings must be effectively damped to maintain the system stability.

IV. Simulation Results

The load flow solution of the above system is calculated and the simulation results are shown below. Two types of faults: A. single line to ground fault & B. Three phase fault have been considered.

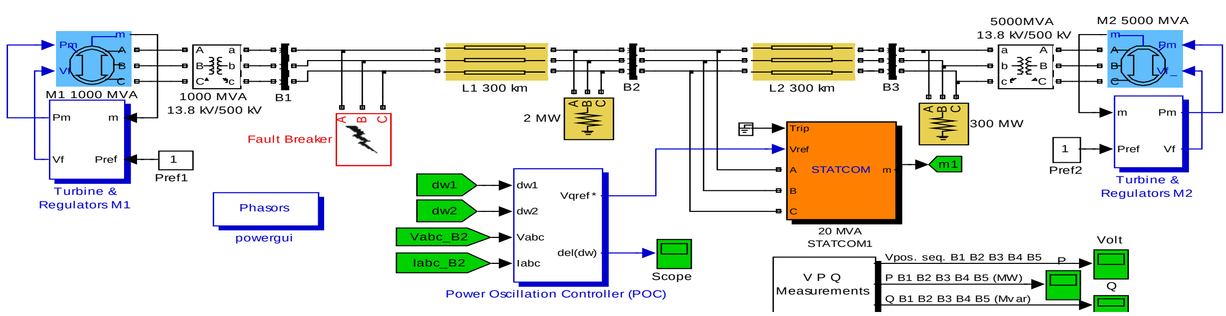

Figure 2 : Complete simulink model of 2-machine power system

a) Single line to ground fault

Consider a 1-phase fault occurred at 0.1s & circuit breaker is opened at 0.2s (4-cycle fault), Without STATCOM, the system voltage, power & machines oscillates goes on unstable [Fig. (3, 5)]. But if STATCOM (without controller) is applied then voltage becomes stable within 3s [Fig.4], power becomes within 3s [Fig.6]. All results has been summarized in table-I.

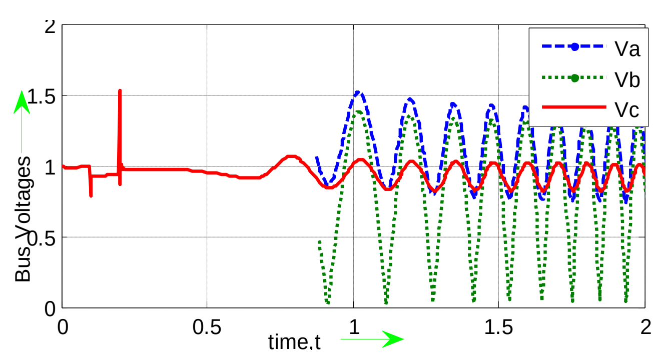

Figure 3 : Bus voltages for 1-phase fault (without STATCOM)

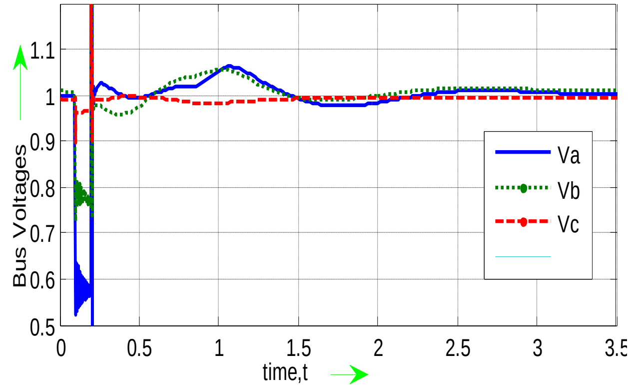

Figure 4 : Bus Voltages in p.u for 1-phase fault (with STATCOM)

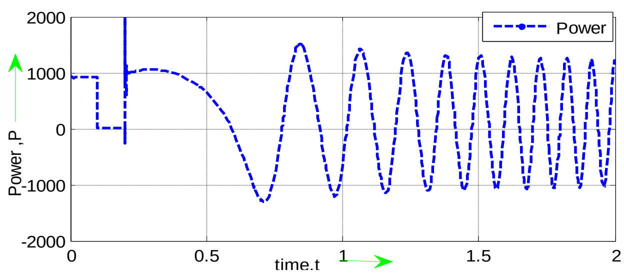

Figure 5 : Bus power, P in MW during fault (Without STATCOM)

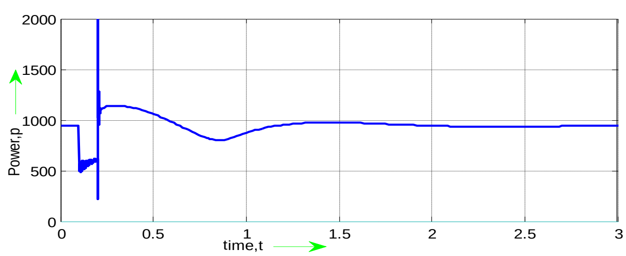

Figure 6 : Bus Power (P) in MW for 1-Ø faults (with STATCOM)

V. Design of Power Oscillation Controller (POC)

The proposed Power Oscillation controller consists of two parts, A. Proportional Integral Derivative (PID) controller which is tuned by Zieglar-Nicles method [4] & Power Oscillation Damping (POD) controller. PID controller takes input as machines angular speed deviation & get an error signal & POD controller takes input as line voltage & line current & after damp out the oscillation it also gives as error signal. Finally, the proposed power oscillation controller takes input as all parameters of power system network i.e. Vabc, Iabc, dω & it gives an error signal (Vqref) which injects STATCOM for improvement of power system stability.

a) Designed of PID Controller

The process of selecting the controller parameters to meet given performance specifications is called PID tuning. Most PID controllers are adjusted on-site, many different types of tuning rules have been proposed in the literature [4]. Using those tuning rules, delicate & fine tuning of PID controllers can be made on-site. Also automatic tuning methods have been developed and some of the PID controllers may possess on-line automatic tuning capabilities [4].
The PID controller has three term control signal[4],

$$u(t) = K_p e(t) + \frac{K_p}{T_i}\int e(t)dt + K_p T_d \frac{de(t)}{dt} \qquad (1)$$

In Laplace Form,

$$\frac{U(s)}{E(s)} = K_p\left(1 + \frac{1}{T_i} + T_d s\right)$$

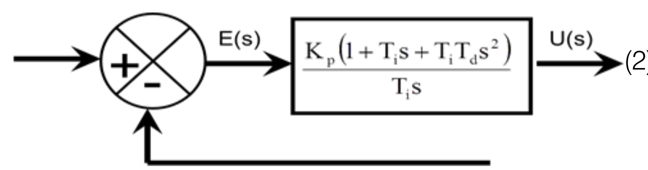

Figure 7 : Block diagram of PID controller parameters

For selecting the proper controller parameters, Ziegler-Nichols PID Tuning [4], Second Method is described below.

In the 2nd method, the parameter is selected as Ti= ∞ ,Td=0. Using the proportional controller action [Fig.4] only increase Kp from 0 to a critical value Kcr. At which the output first exhibits sustained oscillations [Fig.9].

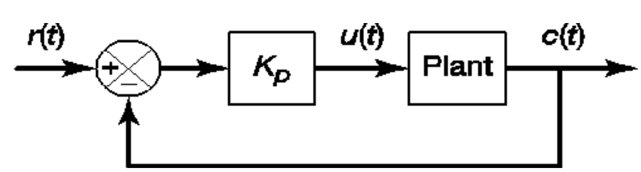

Figure 8 : PID controller is in proportional action

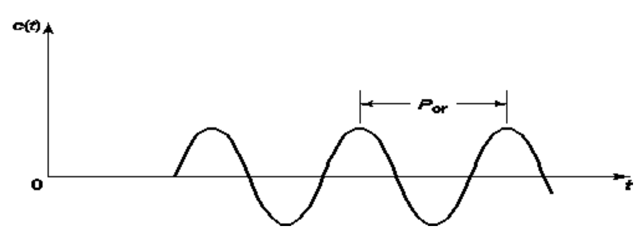

Figure 9 : Determination of sustained oscillation (Pcr)

Thus the critical gain Kcr & the corresponding period Pcr are experimentally determined. Ziegler and Nichols suggested that the values of the parameters Kp Ti Td should set according to the following formula.

Kp=0.6Kcr, Ti=0.5Pcr, Td=0.125Pcr

Notice that the PID controller tuned by the 2nd method of Ziegler-Nichols rules gives,

$$G_C(s) = K_p\left(1 + \frac{1}{T_i * S} + T_d S\right) \tag{3}$$

$$G_C(s) = 0.6K_{cr}\left(1 + \frac{1}{0.5P_{cr} * S} + 0.125P_{cr}S\right) \tag{4}$$

$$G_C(s) = 0.075K_{cr} * P_{cr}\frac{\left(S + \frac{4}{P_{cr}}\right)^2}{S} \tag{5}$$

Thus the PID controller has a pole at the origin and double Zeros at S= - 4/Pcr [Fig.10].

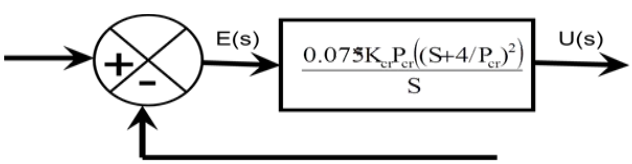

Figure 10 : PID controller with tuning parameters

The critical gain (Kcr) for which the plant output gives a sustained oscillation [Fig.9] is determined for this network (Kcr=200) & corresponding period of Pcr [Fig.9] is also determined from Fig.9 & found Pcr=0.2.Thus the transfer function or parameters of PID controller is determined based on Ziegler-Nichols tuning method [Eq. (1)] which is shown in fig.11 (a, c). During faults the machines angular speed deviation (dω) & mechanical power (Pm), line voltage, line current, power all are changed. So, dω & pm are taken as the input parameters of newly designed PID controller. The proposed PID controlled SVC simulink model is shown in the fig.11.

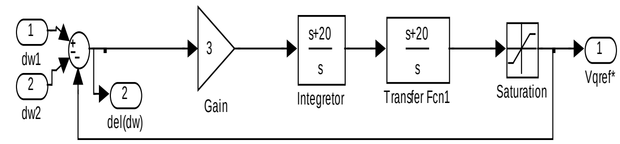

Figure 11 : Internal Structure of PID Controller

b) Designed of POD Controller

The Power Oscillation Damping Controller [Fig.12] takes input as Vabc, Iabc & it convert it as power. If no faults has occurred then switch remains open. But when fault occurred then switch becomes closed & after filtering or dampout oscillation, it also gives an error signal & finally two error signal has been added & this is Vqref.

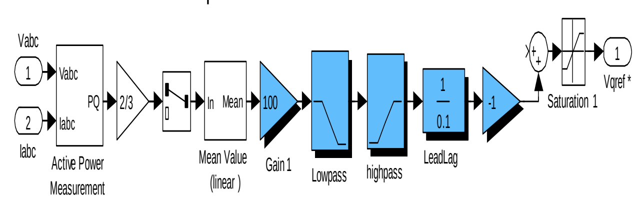

Figure 12 : Internal Structure of POD controller

c) Power Oscillation Controller (POC)

The proposed Power Oscillation Controller consists of both two controllers (PID & POD) [Fig.13] which injects Vqref in STATCOM further improve the power system stability.

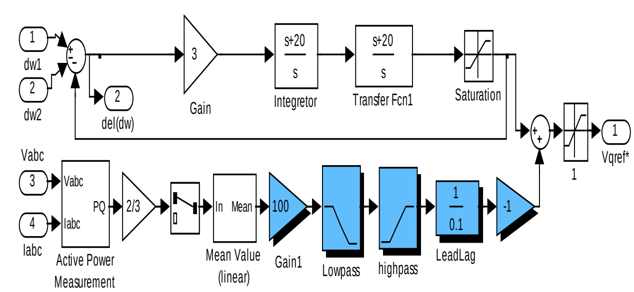

Figure 13 : Internal Structure of Power Oscillation Controller (POC)

VI. Design of Excitation Controller

Alternator prime mover consists of Hydraulic turbine governor (HTG) & Excitation block [Fig.14].

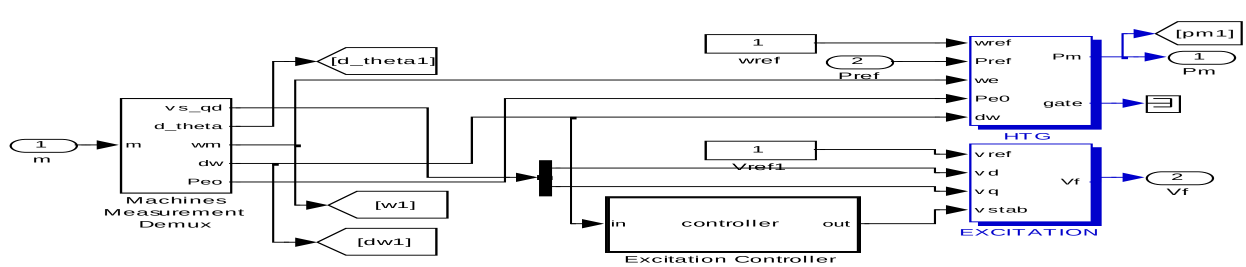

Figure 14 : HTG & Excitation block with controller

Alternator state can be sensed by a feedback. If any faults occur in network then HTG changes the speed of machine & Machine excitation can be changed by excitation controller. Inside the excitation controller, a MATLAB program has been sets so that machine excitation will change as required to regain system stability.

VII. Simulation Results with POC

The network remains same [Fig.2], just simple STATCOM is replaced by power system controlled STATCOM. During fault, machines speed deviation (dω) & Line voltage (Vabc), Line current (Iabc) are always monitored by power system controller & taking input of those oscillation, after processing as shown in Fig.13, it reduces damping of power system oscillation & helps STATCOM to improve stability. Two types of faults has been considered: A. Single line to ground fault and B. Three phase fault.

a) Single line to ground fault

During 1-phase faults, if POC is used as STATCOM controller then, the system voltage becomes stable within 0..25s with 0% damping [Fig.15] & Power (P,Q) becomes stable within 0.25s [Fig.16].

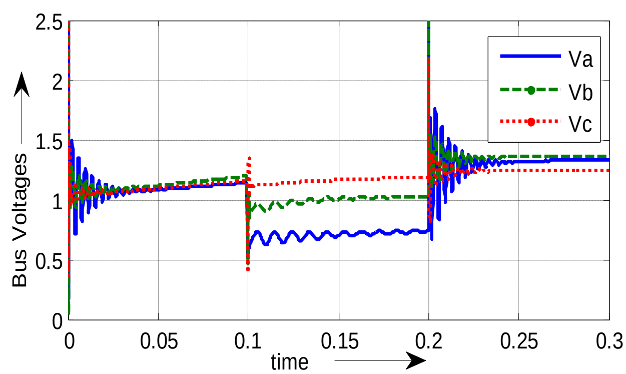

Figure 15 : Bus voltage in p.u for 1-Ø fault (with POC)

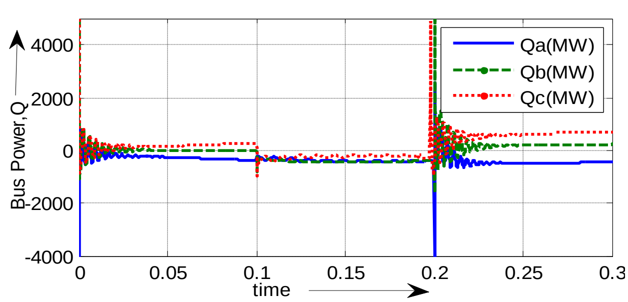

Figure 16 : Bus Power,Q for 1-Ø fault in MW (with POC)

b) Three phase fault

During 3-phase faults, If POC is used as STATCOM controller then, the system voltage becomes stable within 0.25s [Fig.17] & Both power, P becomes stable within 0.25s [Fig.18].

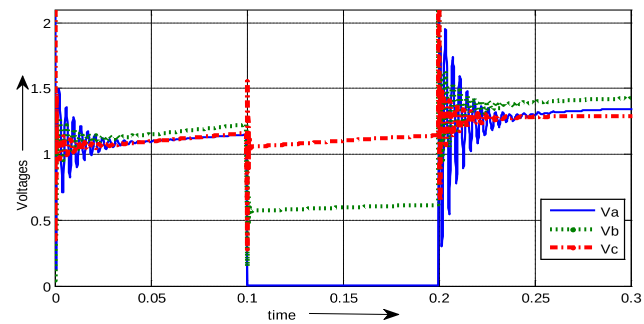

Figure 17 : Bus voltages in p.u for L-L fault (with POC)

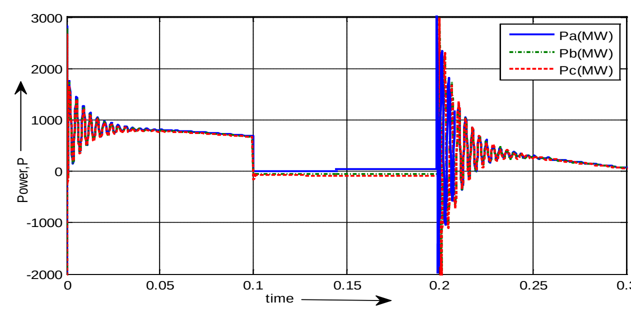

Figure 18 : Bus power, P in MW for L-L fault (with POC)

VIII. Results & Conclusion

The performance of the proposed Power Oscillation Controller with STATCOM has been summarized in the table-I. In table-I, α (infinite time) means the system is unstable, STATCOM rating in MVA. The network is simulated in three steps; without STATCOM, With STATCOM only, STATCOM with proposed Power Oscillation Controller (POC) & Excitation controller.

Table 1 : Performance of proposed Power Oscillation Controller

Controller Status		1-Ø fault (Stability time)		3-Ø fault (Stability time)	
Controller	STATCOM Rating	Volt	P,Q	Volt	P,Q
No STATCOM	0 MVA	α	α	α	α
STATCOM	200 MVA	3s	3s	5s	5s
STATCOM + POC	20 MVA	0..25s	0.25s	0.25s	0.25s

IX. Conclusion

This paper presents the power system stability improvement i.e. voltage level, machine oscillation damping, real power system model of STATCOM without or with proposed Power Oscillation Controller for different types of faulted conditions. POC is also a very efficient controller then others for STATCOM to enhance the power system stability. From above results, this proposed Zigler-Nicles close loop tuning method for selecting PID controller parameters & POD, In combine, Power Oscillation Controller may be highly suitable as a STATCOM controller because of shorter stability time, simple designed, low cost & highly efficient controller. Machines DC Excitation can also be controlled easily by using excitation controller. Rather that, If POC controller is used then only small rating of STATCOM becomes enough for stabilization of robust power system within very shortest possible time for both steady state & dynamic conditions. These proposed Power Oscillation Controller can be applied for any interconnected multi-machine power system network for stability improvement.

These controller can be applied to another FACTS devices namely SSSC, UPFC whose controllers may be controlled externally by designing different types of controllers which also may be tuned by using different algorithm i.e. Fazzy logic, ANN, Genetic algorithm, FSO etc. for both transient and steady state stability improvement of a power system.

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FPGA based Solution for the Identification of RADAR Pulse Sequences for Defense Applications

By J. Pandu, Dr. N. Balaji & Dr. C. D. Naidu

Sreyas Institute of Engineering and Technology, India

Abstract- The main objective of this paper is to design a generalized architecture for polyphase code identification used in RADAR signal processing applications. The proposed VLSI architecture will identify the type of a given polyphase code, amount of phase change and number of phase changes. RADAR signal processing applications require a set of sequences with individually peaky autocorrelation and pair wise cross correlation. Obtaining such sequences is a combinatorial problem. This paper aims at implementation of an efficient VLSI system for the design of polyphase codes identification useful for RADAR applications. The VLSI system is implemented on the field programmable gate array as it provides the flexibility of reconfigurability and reprogrammability and it is a real time signal processing solution which identifies the polyphase codes. The simulation results and the FPGA implementation shows the successful code identification, amount of phase, number of phase changes for a given input sequence.

Keywords: code identification, phase identification, frank codes, polyphase codes, RADAR, FPGA, VLSI, LPI.

GJRE-F Classification : FOR Code: 090609

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Strictly as per the compliance and regulations of :

FPGA based Solution for the Identification of RADAR Pulse Sequences for Defense Applications

J. Pandu [α], Dr. N. Balaji [σ] & Dr. C. D. Naidu [ρ]

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I. Introduction

Polyphase code identification and localization are basic and important problems in RADAR systems. Localizing the received code is an important task in the detection of polyphase codes. Localization of the received signal can leads to incorrect target range measurements. Pulse RADAR that uses pulses as the RADAR signal is being used in aviation control, weather forecasting, and ships. The strength of the received signal by the radar varies with the distance from radar to the target and is also dependent on the target RADAR cross section. The proposed architecture will identify the type of polyphase code, amount of phase change and number of phase changes among the polyphase codes which are present in the Low Probability of Intercept (LPI) RADAR. Identification of these parameters like code, phase, number of phase changes can reguide and retransmit to the transmitter without any effect to our electronic systems. With this system the unwanted signals are retransmitted to the transmitter.

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II. Polyphase Codes

The transmitted complex phase coded signal can be expressed in the following form

$$s(t)=Ae^{j(2\pi f_c t+\phi_i)} \tag{1}$$

where A is the amplitude, f_c is the carrier frequency and $\emptyset_i$ is the discrete phase sequence. Each phase has the same time duration. In the following, five different polyphase pulse compression codes are presented. The codes presented are the Frank, P1, P2, P3, and P4 codes.

a) *Frank Codes*

The Frank code is a step approximation to a linear frequency modulation (LFM) waveform using N frequency steps and N samples per frequency. Thus, the total number of samples in a Frank code is N^2. The phase of the i^{th} sample of the j^{th} frequency of a Frank code is given as

$$\Phi_{i,j}=\frac{2\pi}{N}(i-1)(j-1) \tag{2}$$

Where $i=1,2,\ldots N$ and. $j=1,2,\ldots N$ The pulse compression ratio of the Frank code is N^2. The Frank code has the highest phase increments from sample to sample in the center of the code, where the numbers represent multiplying coefficients of the basic phase angle $2\pi/N$.

b) *P1 Polyphase Codes*

The P1 code also consists of N^2 elements as Frank code, that way P1 code signal with $N=4$ produces a matrix of 16 different phases, if $N=8$ produces a matrix of 64 phases. In a p1 code, the phase of the i^{th} sample of the j^{th} frequency is given by

$$\Phi_{i,j}=\frac{-\pi}{N}[N-(2j-1)][(j-1)N+(i-1)] \tag{3}$$

where $i=1,2,\ldots N$ and $j=1,2,\ldots N$.

c) *P2 Polyphase Codes*

This code is essentially derived in the same way as the P1 code. The P2 code has the same phase increments within each group as the P1 code, except that the starting phase is different. The P2 code is valid for *N* even, and each group of the code is symmetric about 0 phases. In a p2 code, the phase of the i[th] sample of the j[th] frequency is given by

$$\Phi_{i,j}=\left\{\frac{\pi}{2}[(N-1)/N]-\left[\frac{\pi}{N}(i-1)\right]\right\}[N+1-2j] \quad (4)$$

where $i = 1,2,\ldots N$ and $j = 1,2,\ldots N$.

d) P3 Polyphase Codes

This code is derived by converting a linear frequency modulation waveform to baseband using a local oscillator on one end of the frequency sweep and sampling the In phase component I and Quadrature component Q at the Nyquist rate. If the waveform has a pulse length T and frequency $f=f_0+kT$, where k is a constant and the bandwidth of the signal will be approximately. $B=kT$ The bandwidth will support a compressed pulse length of about $t_c=1/BT$ and the waveform will provide a pulse compression ratio of. $pc=\frac{T}{t_c}=BT$ Assuming that the first sample of *I* and *Q* is taken at the leading edge of the waveform, the phases of successive samples taking t_c apart are

$$\Phi_i=2\pi\int_0^{(i-1)t_c}[(f_0+kt)-f_0]dt=\pi k(i-1)^2 t_c^2 \quad (5)$$

Where $i = 1,2,\ldots N$ Substituting $k = B/T$ and $t_c=1/B$, the equation can be written as

$$\Phi_i=\frac{\pi(i-1)^2}{BT}=\frac{\pi(i-1)^2}{N} \quad (6)$$

e) P4 Polyphase Codes

The P4 code consists of discrete phases of the linear chirp waveform taken at specific time intervals and exhibits the same range Doppler coupling associate with the chirp waveform. Phase code elements of the P4 code are given by

$$\Phi_i=\frac{\pi(i-1)^2}{N}-\pi(i-1) \quad (7)$$

where $i = 1$ to N.

f) Barker Codes

Barker sequence is a finite sequence of N values of '+1' and '-1'.The coding scheme used in direct sequence spread spectrum (DSSS) radio systems. Ai for i=1, 2, 3 ….N. such that the off peak autocorrelation coefficients

$$\sum_{i=1}^{i-k} a_i\, a_{i+k}\le 1 \quad (8)$$

For all $1\le k<i$. Barker codes are used for pulse compression of radar signals. There are Barker codes of lengths 2, 3, 4, 5, 7, 11, and 13, and it is conjectured that no longer Barker codes exist.

III. Proposed Architecture

Figure 1 show the block diagram for code identification, phase identification and number of phase changes identification. An input sequence of N bit length is applied to the proposed system. The first 3 MSB bits X_{N-1}, X_{N-2}, X_{N-3} are useful for code identification and the remaining bits from X_{N-4} to X_0 bits are used for phase identification. The input code word format is shown in table1.

Table 1 : Generalized Input Code Word

Code Identification Bits			Phase Identification Bits			
X_{N-1}	X_{N-2}	X_{N-3}	X_{N-4}	..	X_1	X_0

X_{N-4} phase identification bits will give the 2^{N-4} phase changes. The system will find which type of code it is by comparing the coefficients of those respective codes i.e. whether it is Frank, p1, p2, p3, p4 and Barker codes that are store in the memory.

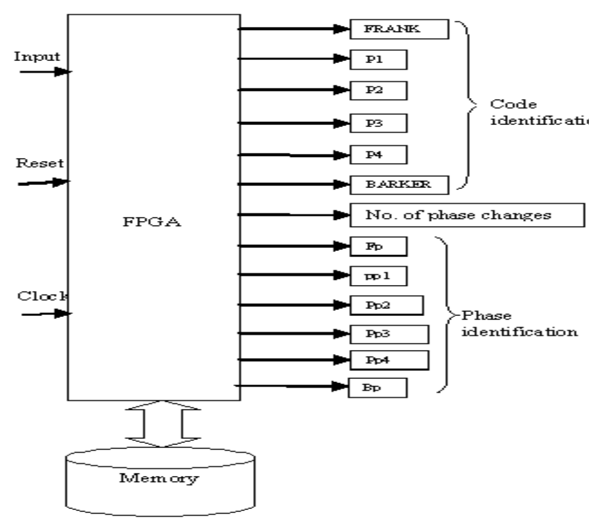

Figure 1 : Block Diagram for Code Identification, Phase Identification and Number of Phase changes Identification

The system has other inputs of clock and reset signal. The count block will give the number of phase changes in the respective code. The registers fp, pp1, pp2, pp3, pp4 are useful for storing the amount of phase change from the adjacent alphabets of the codes.

a) Code Identification

When an input code word shown in table 1 is given by the MSB bits X_{N-1}, X_{N-2}, X_{N-3} are used for code identification where the code identification bits X_{N-1}, X_{N-2}, X_{N-3} are given as inputs. The output is the corresponding identified (frank, p1, p2, p3, p4 and barker) code. Figure 2 shows the generalized block diagram for code identification.

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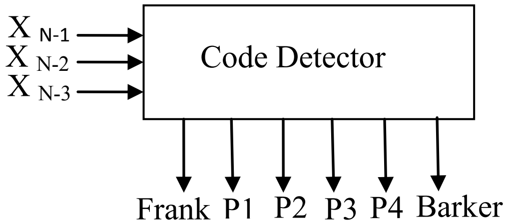

Figure 2 : Block Diagram for Code Identification

The code identification logic and its corresponding input output relationships are shown in the table 2. When the code identification bits are 000 then it will identify as frank code and similarly when the code identification bits are 001,010,011,100 and 101 they correspond to the p1, p2, p3, p4 and barker codes respectively.

b) Phase Identification

The remaining bits from X_0 to X_{N-4} are used for phase identification. Table 3 gives the phase change identification and amount of phase change from one phase to another phase among the polyphase codes. X_{N-4} phase identification bits will give the 2^{N-4} phase changes. The phases are given as from $\phi_0, \phi_1, \ldots\phi_{2^{N-5}}, \phi_{2^{N-4}}$.

Table 2 : Generalized Code Identification Logic

Code identification bits			Code
X_{N-1}	X_{N-2}	X_{N-3}	
0	0	0	Frank
0	0	1	P1
0	1	0	P2
0	1	1	P3
1	0	0	P4
1	0	1	Barker
1	1	0	Used for Future Expansion
1	1	1	

Table 3 : Generalized Phase Change Identification

X_{N-4}	X_{N-5}	………	X_1	X_0	Phase
0	0	………	0	0	ϕ_0
0	0	………	0	1	ϕ_1
0	0	………	1	0	ϕ_2
:	:	………	:	:	:
1	0	………	0	0	ϕ_{N-4}
1	0		0	1	ϕ_{N-3}
:	:	………	:	:	:
1	1	………	1	0	$\phi_{2^{N-5}}$
1	1	………	1	1	$\phi_{2^{N-4}}$

Figure 3 shows the generalized block diagram for the phase change identification. The phase identification unit comprises of state machine diagram as shown in the figure 4

Code identification output enables the corresponding phase identification units. Based on the identified code, the corresponding state machine will be activated. The counter will identify the number of phase changes in the given sequence. For the N-4 bits it will identify 2^{N-4} phase changes. The enable inputs are useful for activating the appropriate state machine for calculating the number of phase changes and amount of phase. The State machine consists of 2^{N-4} states and 2^{N-4+1} outputs and N-4 inputs. The figure 5 shows the N-4 inputs and N-4 next state outputs and corresponding complements. The reset and clock are given as the other inputs of the phase identification unit.

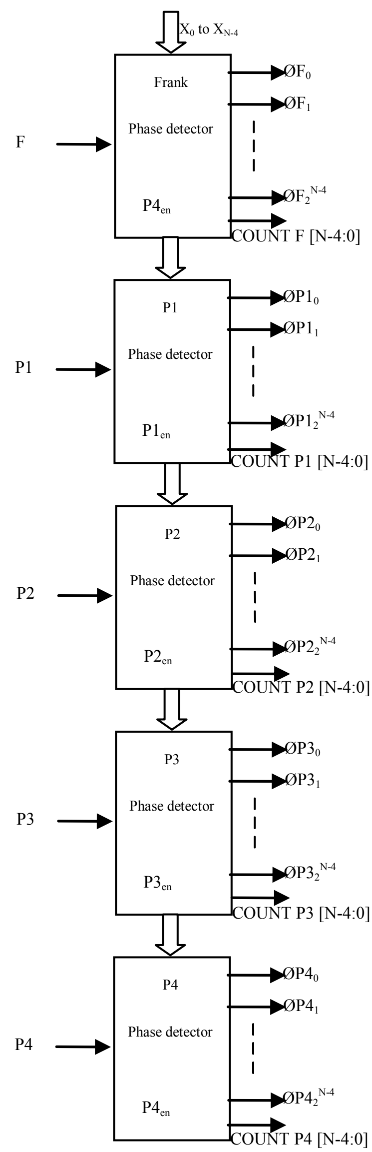

Figure 3 : Block Diagram for Phase Change Identification

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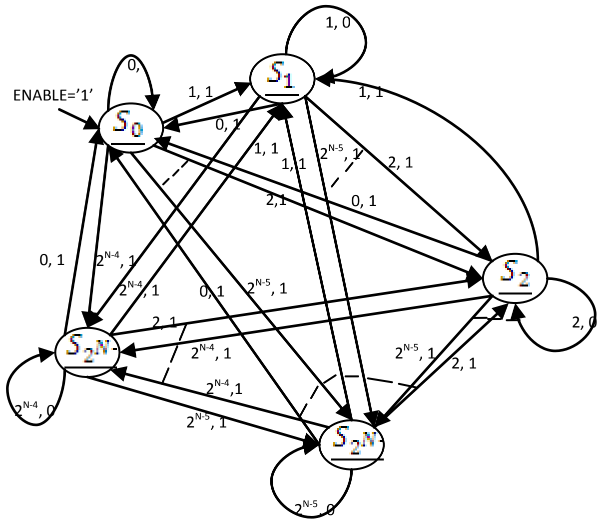

Figure 4 : State diagram for 2^{N-4} Phase Identification

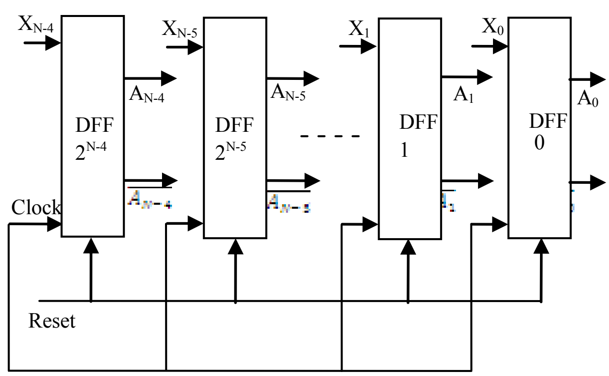

Figure 5 : Generalized Hardware Implementation for Phase Change Identification

From the table 3 the generalized phase changes equations are given below. The phase change can be calculated by using the given equations.

$$\left.\begin{aligned} \Phi_0 &= \overline{A_{N-4}}\,\overline{A_{N-5}}\cdots\cdots\cdots\overline{A_1}\,\overline{A_0} \\ \Phi_1 &= \overline{A_{N-4}}\,\overline{A_{N-5}}\cdots\cdots\cdots A_1\,\overline{A_0} \\ 2^{\Phi_{N-5}} &= A_{N-4}A_{N-5}\cdots\cdots\cdots A_1\,\overline{A_0} \\ 2^{\Phi_{N-4}} &= A_{N-4}A_{N-5}\cdots\cdots\cdots A_1 A_0 \end{aligned}\right\} \quad .\ (9)$$

The number of phase change identification can be identified by using the following equations

$$X(n)=\{X_{N-4}, X_{N-5},\ldots\ldots, X_1, X_0\} \quad (10)$$

$$X(n-1)=\{A_{N-4}, A_{N-5},\ldots\ldots, A_1, A_0\} \quad (11)$$

The phase change is given by

$$Z=X(n) \oplus X(n-1) \quad (12)$$

if Z=1 then count = count+1;
else
count = count;

The count value depends on the number of phases. The number of phases is equal to $\phi_2{}^{N-4}$ then the count value $2^{count} \geq \phi 2^{N-4}$.

IV. Example for Four Phase Identification

For a five input sequence the first three MSB bits are used for the code identification and the remaining two bits are used for the phase identification. The two phase identification bits will give four phases. The clock and reset signals are given to the buffer register. The buffer register is used to split the code identification bits and phase identification bits. The code identification block is used to identify which type of code whether frank, barker, and polyphase code i.e. p1, p2, p3, p4.The level detection unit will give the phases for the corresponding inputs bits. The z_{phase} will give the phase change among the phases. The phase display unit will give the phase angle corresponding to the four phases. The counter block will give the number of phase changes among the four phases. The internal block diagram of the system is given below figure 6.

Figure 7 shows the code identification unit for the five input sequences. The three MSB bits $X_{in}[4]$, $X_{in}[3]$, $X_{in}[2]$ are the code identification bits. These are the inputs given to the code identification unit. The corresponding codes frank, p1, p2, p3, p4 and barker are the outputs of the code identification unit. The clock and reset are the other inputs of the code identification unit.

The code identification logic is shown in table 4

Table 4 Code Identification Logic

Xin [4]	Xin [3]	Xin [2]	FRANK	P1	P2	P3	P4	BARKER
0	0	0	1	0	0	0	0	0
0	0	1	0	1	0	0	0	0
0	1	0	0	0	1	0	0	0
0	1	1	0	0	0	1	0	0
1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	1

If the three MSB bits shows 000 then it will identify the frank code similarly for 001,010,011,100.101 it will give p1, p2, p3, p4, barker codes and the bits 110, 111 are reserved for the future expansion. Figure 8 shows the level detection unit. $X_{in}[0]$, $X_{in}[1]$ are the inputs and Z1, Z2, Z3, Z4 and Z_{phase} are the outputs of the level detection unit. Clock and reset are given as the other inputs of the level detection unit.

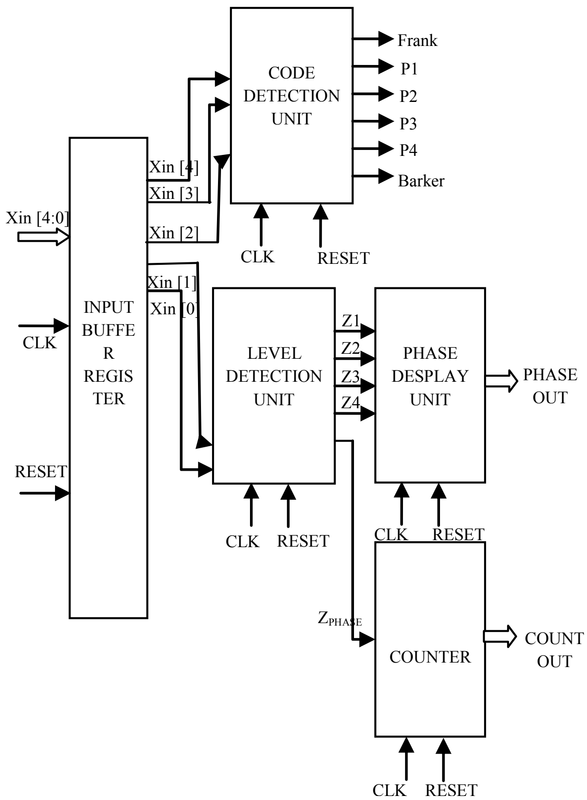

Figure 6 : Top Module of the system

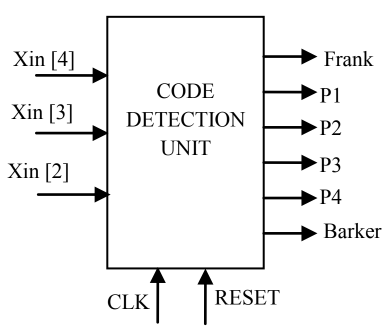

Figure 7 : Code Identification Unit

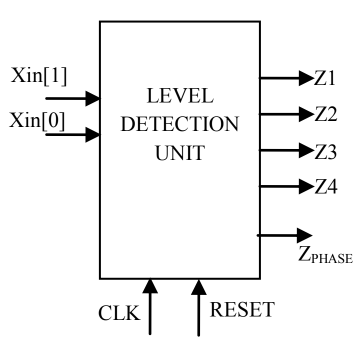

Figure 8 : Level Detection Unit

Table 5 shows the level detection. For the phase identification bits shows 00 then it will give the output z1 similarly for 01, 10, 11 it gives z2, z3, z4 respectively.

Table 5 : Level Detection Logic

Xin [1]	Xin [0]	Z1	Z2	Z3	Z4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Figure 9 shows the phase display unit where Z1, Z2, Z3 and Z4 are the inputs and phase out is the output of the phase display unit.

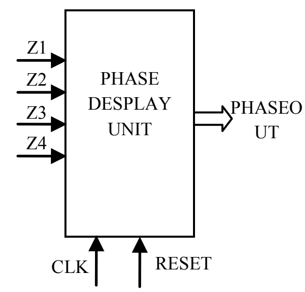

Figure 9 : Phase Display Unit

Table 6 will give the phase display for the corresponding to the level detection output. For the output z1 it will give 0 similarly for z2, z3, z4 it will give 90,180,270 respectively.

Table 6 : Phase Display Logic

Z1	Z2	Z3	Z4	Phase out
1	0	0	0	0
0	1	0	0	90
0	0	1	0	180
0	0	0	1	270

Figure 10 shows the counter unit. For the counter unit Z_{phase} is the input and the count out is the output. The counter unit will give the number of phase changes among the phases.

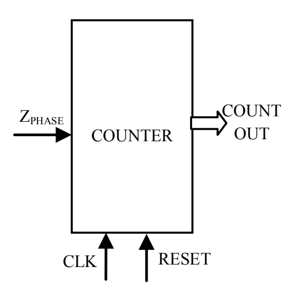

Figure 10 : Counter Unit

The below table shows the logic for identifying the number of phase changes.

$$Z_{PHASE}=Xin\ (n)\ +\ Xin(n\text{-}1) \tag{13}$$

Table 7 : Number of Phase Changes Logic

Z_{phase}	COUNT OUT
1	Count=count+1b'1
0	Count=count

If Z_{phase}=1 then Count=count+1

else

Z_{phase}=0 then Count=count.

V. Results and Discussions

Figure 11 gives the output for the code, amount of phase change and number of phase changes identification. The identified code enabled as logic '1'. It also gives the number of phase changes. The output will give the four phases 0^0, 90^0, 180^0, 270^0. The count block will give the number of phase changes among the codes. The code is identified as p2 code and it is represented in figure 11.the amount of phase change and numbers of phase changes are also shown in figure11.

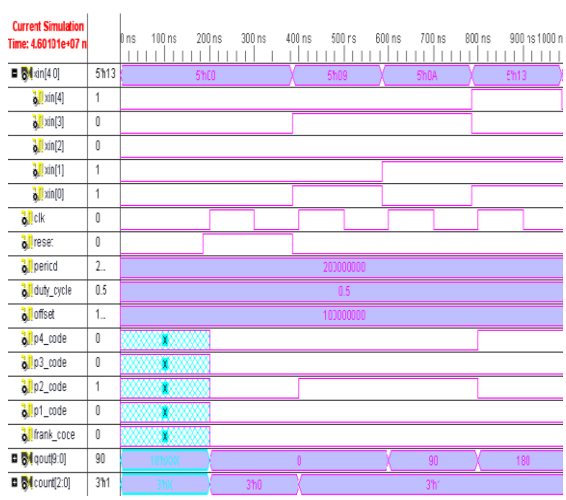

Figure 11 : Simulated output waveform showing the identified code, phase angle and number of phase changes

Figure 12 gives the photograph of the Field Programmable gate array (FPGA) results. The glowing LEDs show the logic '1'and the unglowing LEDs will give the logic'0'.the first three LED's are used for code identification and the remaining LED's are used for phase identification. The identified code is a four phase code.

Figure 12 : Photograph of FPGA Showing the Identified Fourphase Code along with the phase angle

VI. Conclusion and Future Scope

An algorithm is proposed for the identification of radar codes. The proposed algorithm is able to identify the code type, amount of phase and number of phase changes also the algorithm is implemented using FPGA. Using such a system in electromagnetic wave radar will lead to a reduction on the required microwave power supplied to the radar or extending the detection range of the radar. By knowing the coded signal parameters like code, phase, number of phase changes we can reguide and retransmit those signals to the transmitter without effecting our systems.

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Significance of Increasing the Receive Antenna Height in Reducing Path Loss for Hata Path Loss Model

By Md. Imran Hossain Jony, Md. Ibrahim Chowdhury, Ayesha Siddika & Md. Zahid Hasan

City University, Bangladesh

Abstract- This letter shows a significant improvement procedure to reduce the path loss for Hata Path Loss model. This can be applied for urban, suburban and open areas in different frequencies. This is completely a software based approach to determine a relation between the path loss and the height of the receive antenna. Here it is shown that if the height of receive antenna is increased then the path loss decreases significantly.

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GJRE-F Classification : *FOR Code: 291701, 290903*

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Abstract- This letter shows a significant improvement procedure to reduce the path loss for Hata Path Loss model. This can be applied for urban, suburban and open areas in different frequencies. This is completely a software based approach to determine a relation between the path loss and the height of the receive antenna. Here it is shown that if the height of receive antenna is increased then the path loss decreases significantly.

Keywords: hata-model, fading, correlation-coefficient, carrier-frequency, wireless-communication, path-loss.

I. Introduction

In wireless communication fading refers to a very unique characteristic. The variation of the signal amplitude over time and frequency is called fading. There are two types of fading, one is large scale fading and the other is small scale fading. Large scale fading comprises of path loss and shadowing. Hata model is one of the most adopted path loss models that can predict path loss in urban, suburban and open area. Here it is shown that if the height of receive antenna is increased then the path loss decreases significantly. Here the height of the transmit antenna is set to 30m and carrier frequencies used are 1500 MHz and 200 MHz.

a) Hata Model

Among many other radio propagation models, Hata model is currently the most popular path loss model. For the height of transmit antenna, h_{TX} [m], and the carrier frequency of f_c [MHz], the path loss at distance d [m] in an urban area is given by the Hata model as:

$$PL_{Hata,U}(d)[dB] = 69.55 + 26.16 \log f_c - 13.82 \log h_{TX} - C_{RX} + (44.9 + 6.55 \log h_{TX}) \log d.$$

Where, C_{RX} is the correlation coefficient of the receive antenna, which depends on the size of coverage. For small to medium-sized coverage, C_{RX} is given as

$$C_{RX} = 0.8 + (1.1 \log f_c - 0.7) h_{RX} - 1.56 \log f_c$$

Where, h_{RX} [m] is the height of transmit antenna. For large-sized coverage, C_{RX} depends on the range of the carrier frequency, for example,

$$C_{RX} = 8.29 (\log (1.54 h_{RX}))^2 - 1.1 \text{ if } f_c \text{ is in between } 150 \text{ MHz} - 200 \text{ MHz}$$

$$C_{RX} = 3.2 (\log (11.75 h_{RX}))^2 - 4.97 \text{ if } f_c \text{ is in between } 200 \text{ MHz} - 1500 \text{ MHz}$$

Meanwhile, the path loss at distance d in suburban and open areas are respectively given by the Hata model as

$$PL_{Hata,SU}(d)[dB] = PL_{Hata,U}(d) - 2 (\log f_c/28)^2 - 5.4$$

$$PL_{Hata,O}(d)[dB] = PL_{Hata,U}(d) - 4.78 (\log f_c)^2 + 18.33 \log f_c - 40.97$$

As in the urban area there are lots of obstructions like multistoried building or towers, therefore urban area possess more path loss than suburban and open area with the increase of distance between base station and mobile station. Open area have less obstructions and therefore less path loss than urban and suburban area.

Now it will be shown that if the height of the receive antenna is increased then the path loss decreases using MATLAB simulation.

II. Simulation

Several simulations are done to establish the concept which is proposed in this paper. At first the height of the transmit antenna is set to 30 [m] and carrier frequency is set to 1500 MHz. The height of the receive antenna will be varied from 2 [m] to 50 [m]. Now the generated output curves of path loss versus distance for urban, suburban and open area are shown in Fig. 1, Fig. 2, Fig. 3, Fig. 4, Fig. 5 and Fig. 6.

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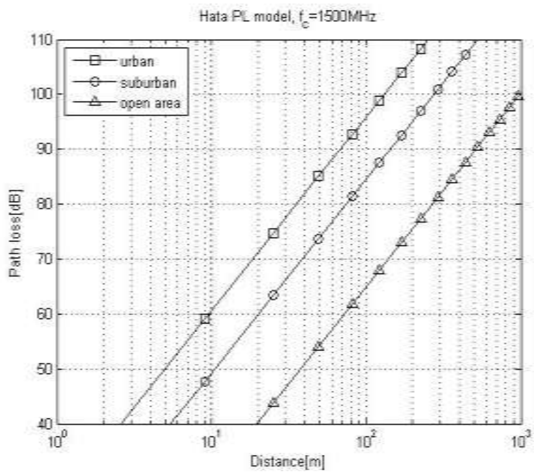

Figure 1 : Path loss vs. distance curves when receive antenna height is 2 [m]

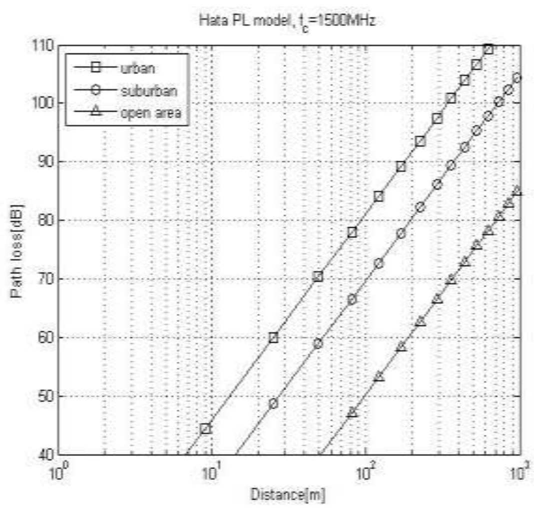

Figure 2 : Path loss vs. distance curves when receive antenna height is 30 [m]

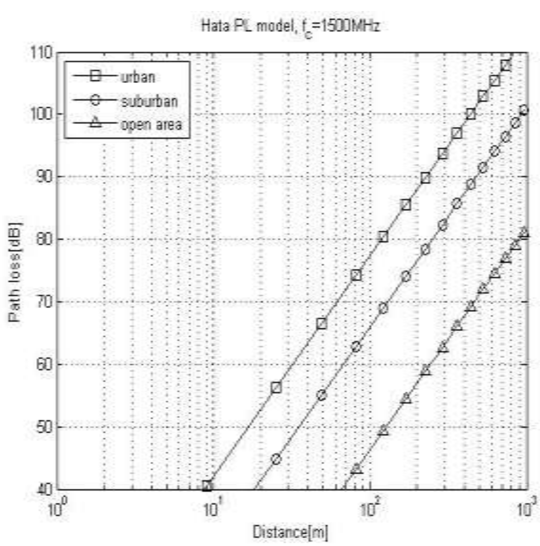

Figure 3 : Path loss vs. distance curves when receive antenna height is 50 [m]

Now the frequency is changed to 200 MHz keeping the transmit antenna height unchanged. Again for different heights of the receive antenna several path loss versus distance curves are generated.

The generated output curves are shown in Fig. 4, Fig. 5 and Fig. 6.

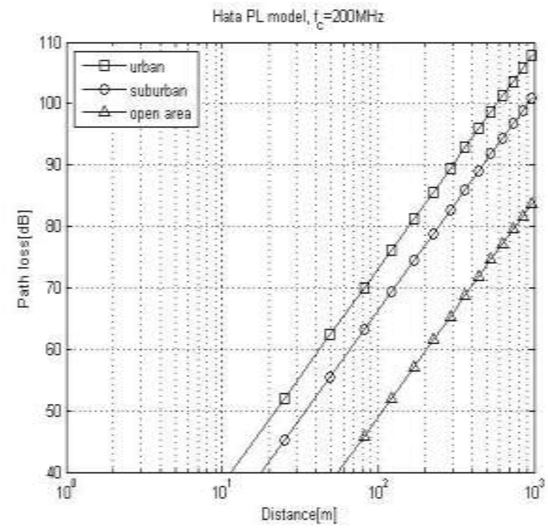

Figure 4 : Path loss vs. distance curves when receive antenna height is 2 [m]

It can also be said that for same value of transmit and receive antenna height, path loss decreases after reducing the value of carrier frequency.

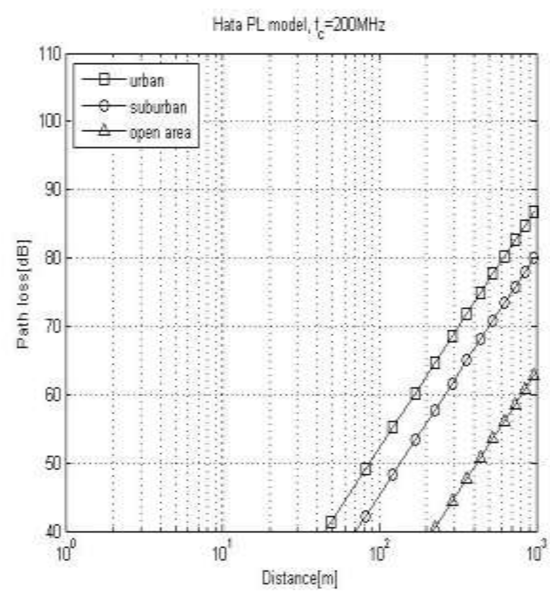

Figure 5 : Path loss vs. distance curves when receive antenna height is 30 [m]

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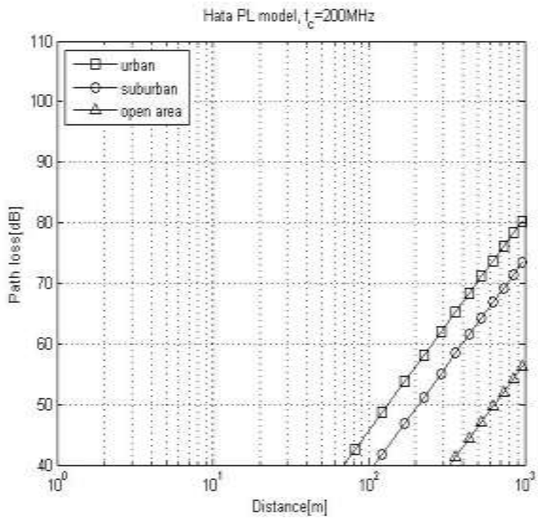

Figure 6 : Path loss vs. distance curves when receive antenna height is 50 [m]

III. Discussion

Simulation is done for different heights of receive antenna. Figure. 1, Fig. 2 and Fig. 3 are generated for a carrier frequency of 1500 MHz. We could see that path loss decreases with the increase of receive antenna height. Say for example, in Fig. 1, when distance is 100 [m] then path losses are around 97, 85 and 65 [dB] for urban, suburban and open area, respectively. But these values decrease in Fig. 2 and Fig. 3 for the same distance. In Fig. 3, path losses become around 78, 67, 47 [dB] for the same distance of 100 [m]. Figure. 4, Fig. 5 and Fig. 6 are generated for a carrier frequency of 200 MHz.

In Fig. 4, when distance is 100 [m] then path losses are around 72, 68 and 49 [dB] for urban, suburban and open area, respectively. But these values decrease in Fig. 5 and Fig. 6 for the same distance. In Fig. 6, path losses become around 47, 0, 0 [dB] for the same distance of 100 [m] which is a significant improvement.

IV. Conclusions

In this paper we tried to show the relation between the path loss and the height of receive antenna. It is evident that, path loss decreases with the increase of receive antenna's height. But in practice, this is not quite feasible enough in case of our cell phone. Because it is not possible to increase the height of its antenna to a significant amount as it will increase the cell size and weight. That is why sometimes external antennas are provided with the cell phones. So, the height of receive antenna should be increased to reduce the path loss to a significant amount.

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RGBtooth: RGB Color based Data Communication Protocol

By Md. Shiblee Nooman, Lutfeyara Begum Sweety, Silvia Shukla Karmokar & Kaiser Habib

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Abstract- At present time data communication is a keyword to our life. It's a time of IOT revolution. Lots of devices around us communicate with each other or they send data to internet. Some of the popular data communication protocols are like Bluetooth, Zigbee, Infrared, wifi, Wlan etc. In this project a similar type of wireless data communication system is designed. Some of the key factors of data communications systems are wireless, covered distance, data transfer speed, security or encryption etc. In this paper we have proposed a RGB color based data communication system. In this system each device is a transceiver. Each device contains of 16bit RGB color sensing module and RGB led. To transfer data from one device to another transmitting module encode raw data to a 16bit combination. This 16bit combination is transferred to RGB led and the color of this 16bit combination will glow. The receiving module will read this color and decode the color into 16bit data. This data is the raw data which we want to receive from the transmitter.

Keywords: color sensor, RGB led, data communication, protocol.

GJRE-F Classification : FOR Code: 090699

RGBtooth: RGB Color based Data Communication Protocol

Md. Shiblee Nooman [α], Lutfeyara Begum Sweety [σ], Silvia Shukla Karmokar [ρ] & Kaiser Habib [ω]

Abstract- At present time data communication is a keyword to our life. It's a time of IOT revolution. Lots of devices around us communicate with each other or they send data to internet. Some of the popular data communication protocols are like Bluetooth, Zigbee, Infrared, wifi, Wlan etc. In this project a similar type of wireless data communication system is designed. Some of the key factors of data communications systems are wireless, covered distance, data transfer speed, security or encryption etc. In this paper we have proposed a RGB color based data communication system. In this system each device is a transceiver. Each device contains of 16bit RGB color sensing module and RGB led. To transfer data from one device to another transmitting module encode raw data to a 16bit combination. This 16bit combination is transferred to RGB led and the color of this 16bit combination will glow. The receiving module will read this color and decode the color into 16bit data. This data is the raw data which we want to receive from the transmitter.

Keywords: color sensor, RGB led, data communication, protocol.

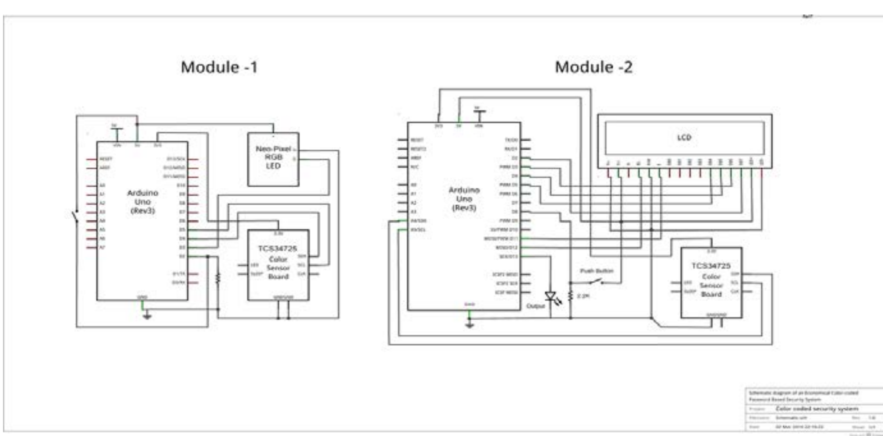
I. Introduction

Data communication plays a key role in our present life. Around us most of the devices uses different types of data communication technique. Some of them are designed for very long distance like DTMF communication[1]. Some are designed for short distance wireless communication like Bluetooth [2], infrared [3] etc. Infrared has lost its popularity due to lower data transfer rate. In this paper we have tried to design a protocol which works wireless but short distance communication. Infrared (IR) light is electromagnetic radiation with longer wavelengths than those of visible light, extending from the nominal red edge of the visible spectrum at 700 nanometers (nm) to 1 mm. Infrared transfer data by only red light. But if we can increase the number of color combination and bit depth then it is possible to increase the data transfer speed. In this paper to transfer data, combination of three types of color is used. Any combination of red, green and blue can make a unique color. But the range of this combination depends on the bit depth of the color. Usually 8bit color combination is used in different purpose but in this project 16bit depth RGB color combination is used to encode the raw data. This increases the range of data combination and the data transfer rate also.

II. Circuit Diagram

Circuit consists of two module. Both of them can be data transceiver. But in this project we used first module as data transmitter and the second one as data receiver. First module consists of arduino uno which is the heart of the module. Adafruit TCS34725 Color Sensors is used to receive the colors as data. Neopixel rgb led is connected with arduino.

Figure 1 : Circuit Diagram of RGB transmitter & Receiver



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5v Dc & ground pin of Arduino connected with vcc of rgb led & color sensor. Through I2C the color sensor communicates with arduino. SDA & SCL of arduino is connected with the color sensor respectively. SDA is on Digtital 20 and SCL is on digital 21. The LED pin can be pulled low to turn off the LED. By connecting wire directly to ground to turn it off completely. Connecting the LCD screen to Arduino through following pins:

- LCD RS pin to digital pin 12
- LCD Enable pin to digital pin 11
- LCD D4 pin to digital pin 5
- LCD D5 pin to digital pin 4
- LCD D6 pin to digital pin 3
- LCD D7 pin to digital pin 2

Additionally, wire a 10K pot to +5V and GND, with it's wiper (output) to LCD screens VO pin (pin3).

III. Circuit Diagram

- List of equipments:-

a) Arduino Uno

The Arduino Uno is a microcontroller board based on the ATmega328. It has 14 digital input/output pins, 6 analog inputs, a 16 MHz ceramic resonator, a USB connection. The Uno differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega16U2.

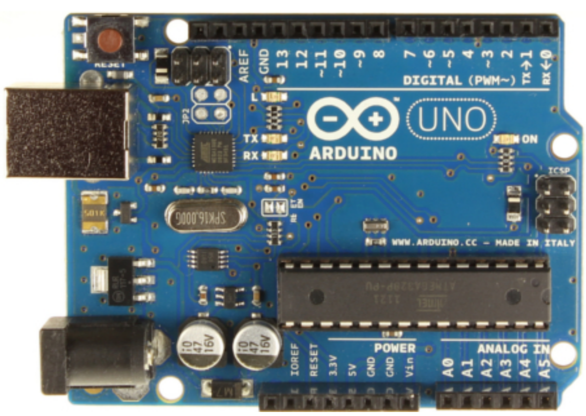

Figure 2 : Arduino Uno front side

Figure 3 : Arduino Uno rear side.

b) Liquid Crystal

The LiquidCrystal library allows you to control LCD displays that are compatible with the Hitachi HD44780 driver. There are many of them out there, and you can usually tell them by the 16-pin interface.

This example sketch prints "Hello World!" to the LCD and shows the time in seconds since the Arduino was reset.

Figure 4 : output of the sketch on a 2x16 LCD

The LCDs have a parallel interface, meaning that the microcontroller has to manipulate several interface pins at once to control the display. The interface consists of the following pins:

A register select (RS) pin that controls where in the LCD's memory you're writing data to. You can select either the data register, which holds what goes on the screen, or an instruction register, which is where the LCD's controller looks for instructions on what to do next. A Read/Write (R/W) pin that selects reading mode or writing mode An Enable pin that enables writing to the registers 8 data pins (D0 -D7). The states of these pins (high or low) are the bits that you're writing to a register when you write, or the values you're reading when you read.

There's also a display constrast pin (Vo), power supply pins (+5V and Gnd) and LED Backlight (Bklt+ and BKlt-) pins that you can use to power the LCD, control the display contrast, and turn on and off the LED backlight, respectively.

The process of controlling the display involves putting the data that form the image of what you want to display into the data registers, then putting instructions in the instruction register.

c) Flora RGB Smart newPixel

It runs at 'high speed' 800KHz communication. These pixels have full 24-bit color ability with PWM taken care of by the controller chip. Since the LED is so bright, you need less current/power to get the effects you want. The driver is constant current so its OK if your battery power changes or fluctuates a little.

Each pixel draws as much as 60mA (all three RGB LEDs on for full brightness white). In theory, the Flora can drive up to 500 pixels at 30 FPS (it will run out of RAM after that).

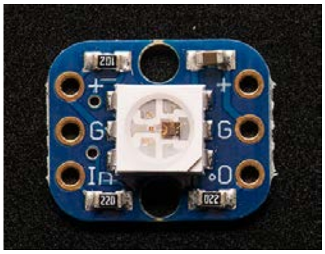

Figure 5 : Neopixel RGB Led

The TCS34725, which has RGB and Clear light sensing elements. An IR blocking filter, integrated on-chip and localized to the color sensing photodiodes, minimizes the IR spectral component of the incoming light and allows color measurements to be made accurately. The filter means getting much truer color, since humans don't see IR. The sensor also has an incredible 3,800,000:1 dynamic range with adjustable integration time and gain.

It has supporting circuitry as well, such as a 3.3V regulator so you can power the breakout with 3-5VDC safely and level shifting for the I2C pins so they can be used with 3.3V or 5V logic. Finally, it has a neutral 4150°K temperature LED with a MOSFET driver onboard to illuminate what you're trying to sense. The LED can be easily turned on or off by any logic level output.

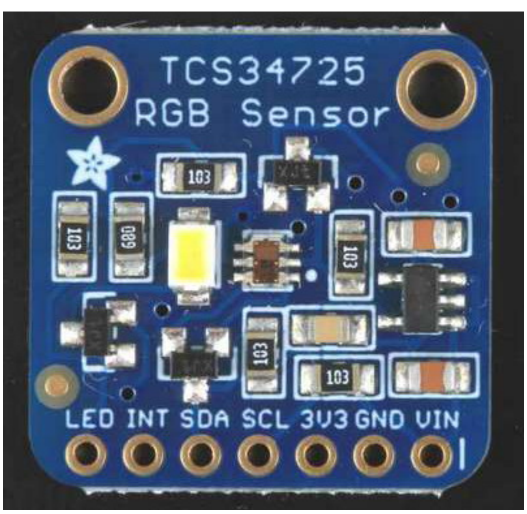

Figure 6 : TCS34725 RGB Color Sensor

IV. Hardware Implementation

In Transmitting module RGBtooth word is decoded and transmitted through rgb led. Here is some of the snap shots of encoded colors for the data RGBtooth.

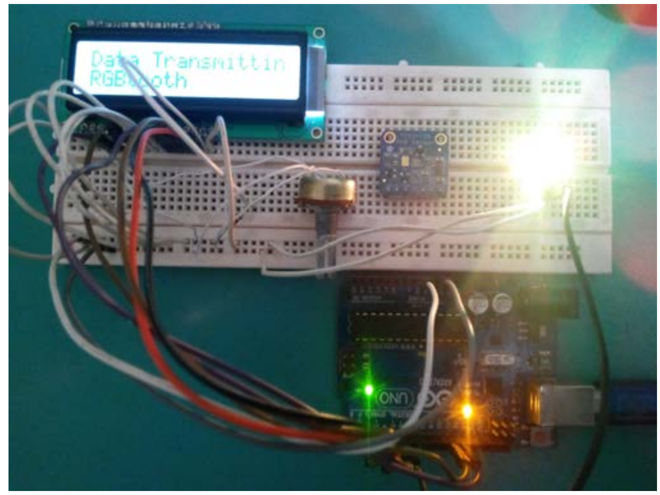

Figure 7 : Data Transmitting 1

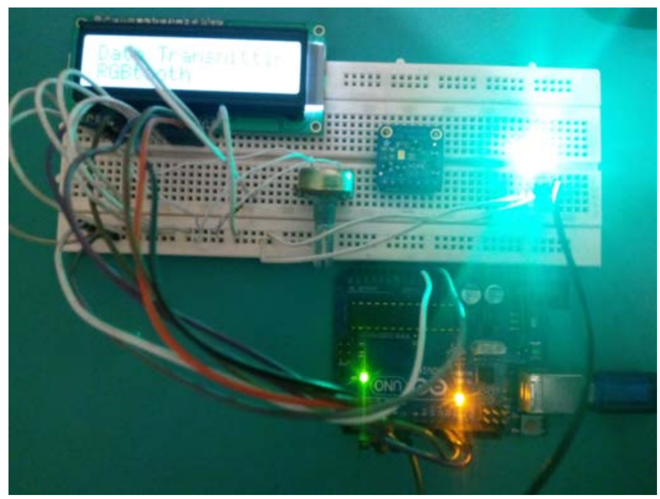

Figure 8 : Data Transmitting 2

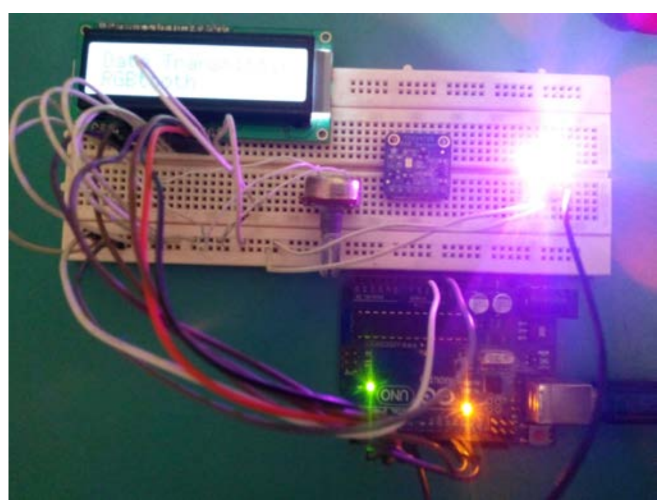

Figure 9 : Data Transmitting 3

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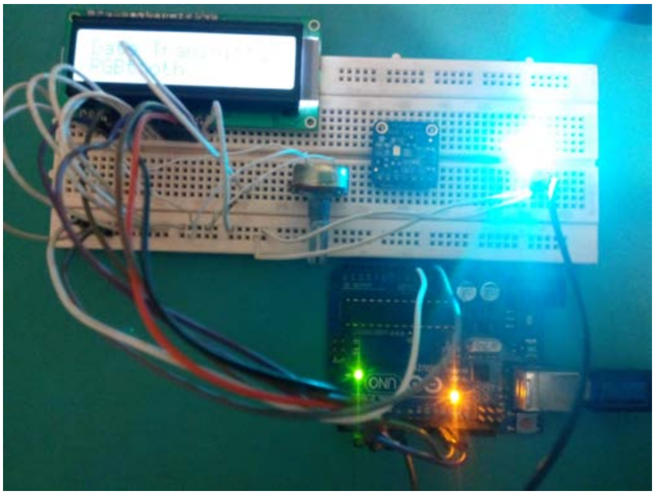

Figure 10 : Data Transmitting 4

Bellow the hardware implementation of data receiving is also shown.

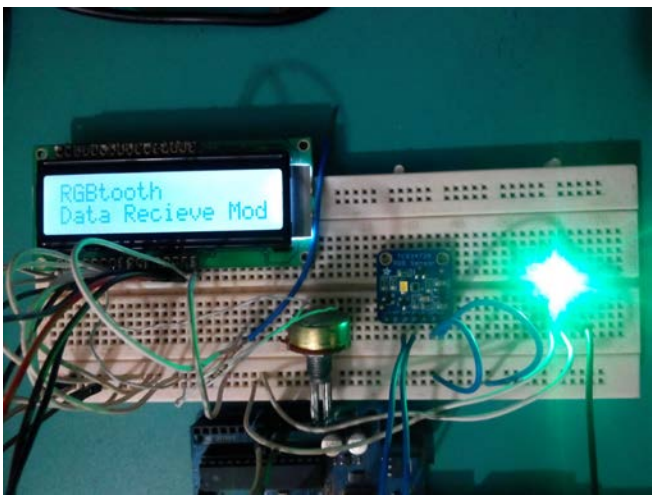

Figure 11 : Data Receiving Module

V. MAIN TECHNOLOGY USED

In the portion of the code we used arduino.cc lcd library, adafruit color sensor library & RGB led library. Bellow some of the important codes are shown.

```
#include <Adafruit_NeoPixel.h>
#define PIN 6 //RGB Led
#include <LiquidCrystal.h>
LiquidCrystal lcd(12, 11, 5, 4, 3, 2);
```

Here we have converted the text RGBtooth into different colors.

Text	R	G	B	t	o	o	t	h
Ascii	82	71	66	116	111	111	116	104

Each three digit combines and create a color to transmit those three digits.

```
colorWipe(strip.Color(82, 71, 66),50); // RGB
colorWipe(strip.Color(116, 111, 111), 50); // too
colorWipe(strip.Color(116, 104, 0), 50); // th
```

Here 50 means the light will be displayed for 50mili seconds. This time period is adjustable and it varies the data transmission speed. At best the RGB led is capable of transmitting data at 800khz speed and each time it combines 24bits of data. So approximately the highest amount of data transfer speed can be achieved in theory 24x800Khz=19200Khz. Which equals to 18.75Mhz. But in this experiment to get the data value accurately we have used much lower data transfer speed.

VI. FURTHER APPLICATIONS

- Color based password lock system.
- Secret Data communication.
- Inside Fiber optic cable.
- Cell phone for data communication.

VII. CONCLUSION

Although it is a very new concept about data communication but still it is possible to transfer higher rate of data through this process. The accuracy can be increase through encapsulating all the lights which emits. An encryption technique like start bits, stop bits, parity bits can make this communication more stable. This new communication technique can be used in many different fields.

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Improvement of Power System Stability by using UPFC with Cascade Proportional Integral Differential Controller

By Pranoy Kumar Singha Roy, MD Nasmus Sakib Khan Shabbir & Md Nazmul Hussain

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Abstract- In power system, one most crucial problem is maintaining system stability. The main reasons for occurring stability problem in the system is due to the fault occurs in the system. This paper presents the model of a Unified Power Flow Controller (UPFC) which is externally controlled by a cascade Proportional Integral Differential (PID) controller for the improvements of voltage stability on line power system. The cascade PID controller parameters has been selected by using Tyreus-Luyben settings method for primary loop controller and modified Ziegler-Nichols method for secondary loop controller. Cascade control is mainly used to achieve fast rejection of disturbance before it propagates to the other parts of the plant.PID controller in cascade architecture is the best choice compared to conventional single loop control system for controlling nonlinear processs. The primary controller is used to calculate the setpoint for the secondrary controller. Both single phase and three phase faults have been considered in the research. In this paper, A power system network is considered which is simulated in the phasor simulation method & the network is simulated in three steps; without UPFC, With UPFC but no externally controlled, UPFC with cascade PID.

Keywords: UPFC , voltage regulator, cascade propotional integral differential controller, matlab simulink.

GJRE-F Classification : FOR Code: 090607, 290901p

IMPROVEMENTOFPOWERSYSTEMSTABILITYBYUSINGUPFCWITHCASCADEPROPORTIONALINTEGRALDIFFERENTIALCONTROLLER

Improvement of Power System Stability by using UPFC with Cascade Proportional Integral Differential Controller

Pranoy Kumar Singha Roy [α], MD Nasmus Sakib Khan Shabbir [σ] & Md Nazmul Hussain [ρ]

Abstract- In power system, one most crucial problem is maintaining system stability. The main reasons for occurring stability problem in the system is due to the fault occurs in the system. This paper presents the model of a Unified Power Flow Controller (UPFC) which is externally controlled by a cascade Proportional Integral Differential (PID) controller for the improvements of voltage stability on line power system. The cascade PID controller parameters has been selected by using Tyreus-Luyben settings method for primary loop controller and modified Ziegler-Nichols method for secondary loop controller. Cascade control is mainly used to achieve fast rejection of disturbance before it propagates to the other parts of the plant.PID controller in cascade architecture is the best choice compared to conventional single loop control system for controlling nonlinear processs. The primary controller is used to calculate the setpoint for the secondray controller. Both single phase and three phase faults have been considered in the research. In this paper, A power system network is considered which is simulated in the phasor simulation method & the network is simulated in three steps; without UPFC, With UPFC but no externally controlled, UPFC with cascade PID. Simulation result shows that without UPFC, the system parameters becomes unstable during faults. When UPFC is imposed in the network, then system parameters becomes stable. Again, when UPFC is controlled externally by cascade PID controllers, then system parameters (V,P,Q) becomes stable in faster way then without controller. It has been observed that the UPFC ratings are only 10 MVA with controllers and 100 MVA without controllers. So, UPFC with cascade PID controllers are more effective to enhance the voltage stability and increases power transmission capacity of a power system. The power system oscillations is also reduced with controllers in compared to that of without controllers. So with cascade PID controllers the system performance is greatly enhanced.

Keywords: UPFC, voltage regulator, cascade propotional integral differential controller, matlab simulink.

I. Introduction

FACTS can convenience the power flow control, increases the power transfer capability, enhance the security and stability, decrease the generation cost of the power system [1]-[2]. UPFC is one kind of FACTs device which can be installed in series in the transmission lines [3]. It is used to control the power flow along the transmission line and thus to meet the needs of power transfer. UPFC consists of a series and shunt converter that is connected by a common DC link capacitor. UPFC performs simultaneously the function of transmission line real and reactive power flow control in addition to UPFC bus voltage shunt reactive power control. The parameters (voltage, impedence, and phase angle) affecting power flow in the transmission line which can be control by using of the UPFC [4]-[6]. The UPFC bus voltage/shunt reactive power and the dc link capacitor voltage is controlled by the shunt converter of the UPFC. The series converter of the UPFC injects a series voltage of adjustable magnitude and phase angle in the transmission line and controls real and reactive power flow in the transmission line [7]-[9]. The dynamic nature of the UPFC lies in the use of thyristor devices (e.g. GTO, IGCT).Therefore, this paper presents thyristor based UPFC controllers to improve the performance of multimachine power system.

II. Control Concept of UPFC

UPFC is a FACTS device used for improving power quality in power systems is shown in fig1.The UPFC consists of combination of series converter and shunt converter. The DC terminals of shunt device are connected to a common link DC capacitor. The shunt converter of the UPFC controls the UPFC bus voltage/shunt reactive power and the dc link capacitor voltage. In this case, the shunt converter voltage is decomposed into two components. One component is in phase and the other in quqdrature with the UPFC bus voltage. Decoupled control system has been employed to achive simultaneous control of the UPFC bus voltage and the DC link capacitor voltage. The series converter of the UPFC provides simultaneous control of real and reactive power flow in the transmission line. The series converter injected voltage is decomposed into two component. One component of the series injected voltage is in quadrature and the other in phase with the UPFC bus voltage. The quadrature injected component controls the transmission line real power flow. This strategy is similar to that of a phase shifter. The in phase component controls the transmission line reactive power flow. This strategy is similar to that of a tap changer.

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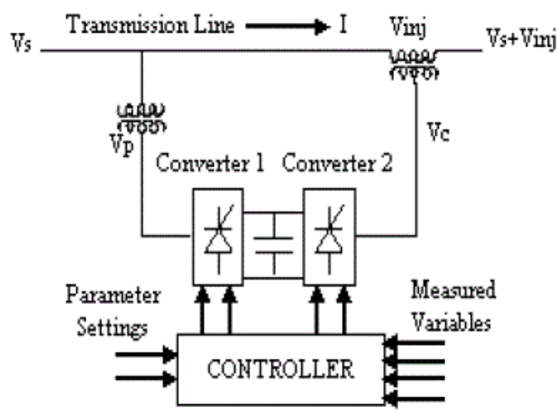

Figure 1 : UPFC based control system

III. Power System Model

This example described in this section illustrates modeling of a simple transmission system containing 2-hydraulic power plants in Fig.2. The power grid consists of two power generation substations[10]. Complete simulink model is shown in Fig.3.

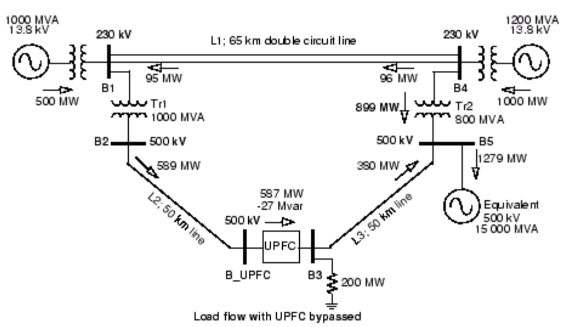

Figure 2 : Single line diagram of 2-machine power system

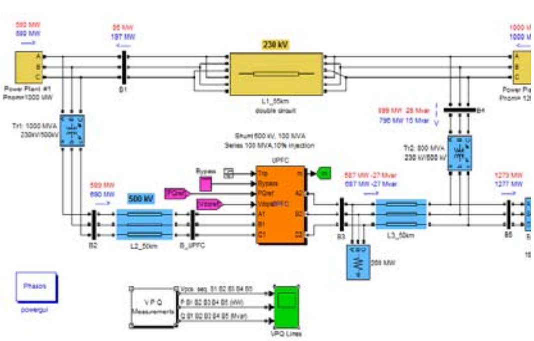

Figure 3 : Complete simulink model of 2-machine power system[10]

A UPFC is used to control the power flow in a 500 kV /230 kV transmission system. The system, connected in a loop configuration, consists essentially of five buses (B1 to B5) interconnected through three transmission lines (L1, L2, L3) and two 500 kV/230 kV transformer banks Tr1 and Tr2. Two power plants located on the 230 kV system generate a total of 1500 MW which is transmitted to a 500 kV, 15000 MVA equivalent and to a 200 MW load connected at bus B3. Each plant model includes a speed regulator, an excitation system as well as a power system stabilizer (PSS). In normal operation, most of the 1200 MW generation capacity of power plant #2 is exported to the 500 kV equivalent through two 400 MVA transformers connected between buses B4 and B5. For this demo we are considering a contingency case where only two transformers out of three are available (Tr2= 2*400 MVA = 800 MVA). The load flow shows that most of the power generated by plant #2 is transmitted through the 800 MVA transformer bank (899 MW out of 1000 MW) and that 96 MW is circulating in the loop. Transformer Tr2 is therefore overloaded by 99 MVA. The demonstration illustrates how the UPFC can relieve this power congestion. The UPFC located at the right end of line L2 is used to control the active and reactive powers at the 500Kv bus B3, as well as the voltage at bus B_UPFC. It consists of a phasor model of two 100-MVA, IGBT-based, converters (one connected in shunt and one connected in series and both interconnected through a DC bus on the DC side and to the AC power system, through coupling reactors and transformers). Parameters of the UPFC power components are given in the dialog box. The series converter can inject a maximum of 10% of nominal line to-ground voltage (28.87 kV) in series with line L2. The blue numbers on the diagram show the power flow with the UPFC in service and controlling the B3 active and reactive powers respectively at 687 MW and -27 Mvar. Machines, UPFC parameters value was taken from reference[10]. Complete Simulink model has shown in Fig.3.

IV. Simulation Results

The load flow solution of the above system is calculated and the simulation results are shown below. Two types of faults: A. single line to ground fault &B. Three phase fault have been considered.

a) Single line to ground fault

Consider a 1-phase fault occurred at 0.1s & circuit breaker is opened at 0.2s (4-cycle fault), Without UPFC, the system voltage, power goes on unstable[Fig.(4,6)]. But if UPFC(without controller) is applied then voltage becomes stable within 1s [Fig.5],power(P,Q) becomes within 1.4s[Fig.(7,8)] . All results has been summarized in table-III.

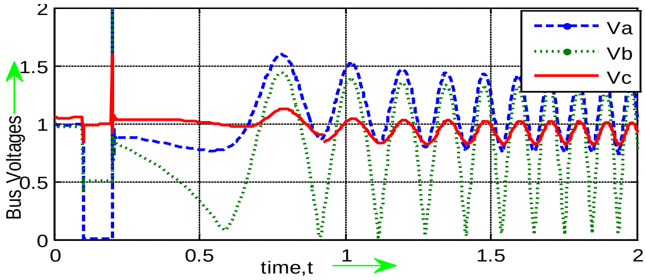

Figure 4 : Bus voltages in p.u for 1-phase fault (without UPFC)

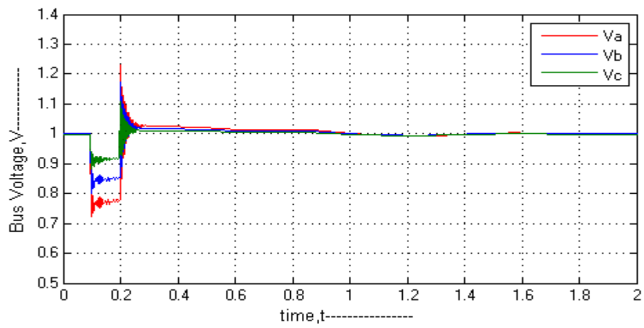

Figure 5 : Bus Voltages in p.u for 1-phase fault (with UPFC)

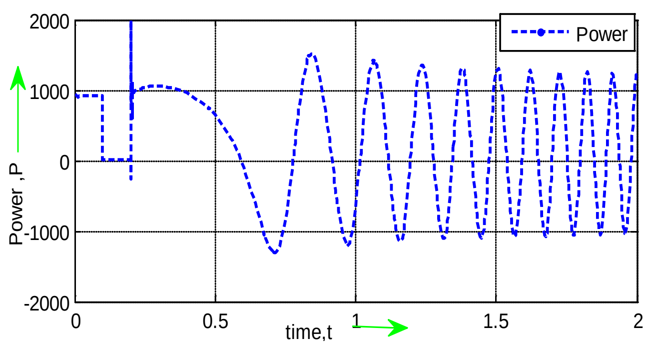

Figure 6 : Bus power, P in MW during fault (Without UPFC)

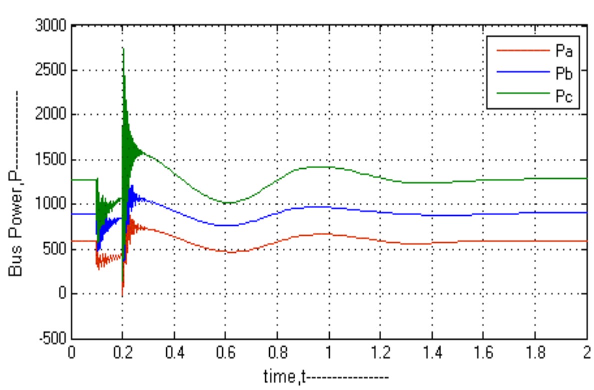

Figure 7 : Bus Power(P)in MW for 1-Ø faults (with UPFC)

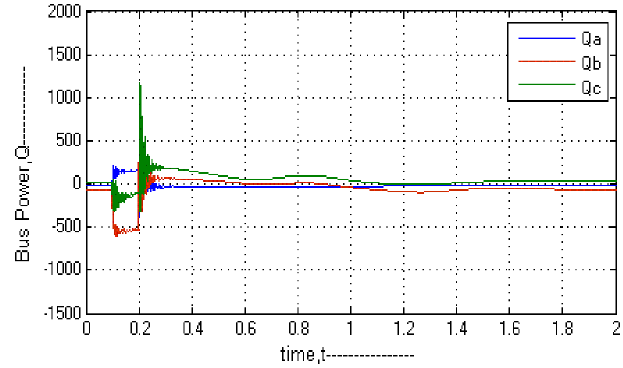

Figure 8 : Bus Power (Q) in MVAR for 1- phase fault (with UPFC)

b) Three phase fault

During 3-phase faults, If UPFC is applied then system voltage becomes stable at t=1.2s [Fig.9] &Power becomes stable at t=1.6s [Fig.(10,11)].

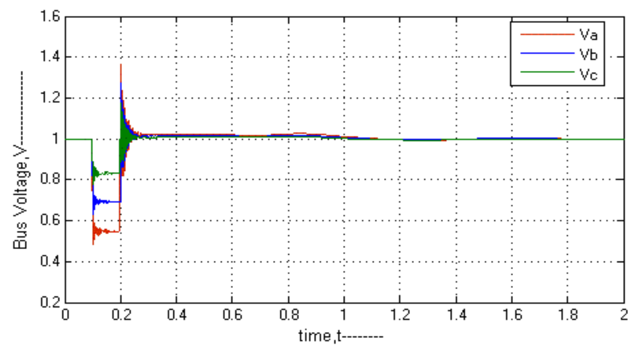

Figure 9 : Bus Voltages in p.u for 3-phase fault (with UPFC)

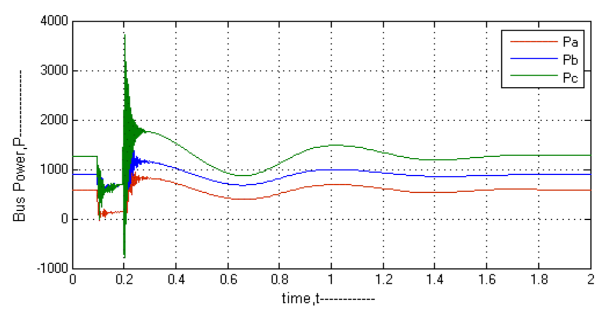

Figure 10 : Bus Power, P in MW for 3-phase fault (with UPFC)

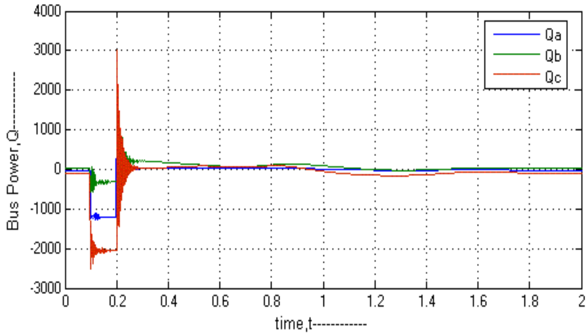

Figure 11 : Bus Power,Q in MVAR for 3-phase fault (with UPFC)

V. Designe of Cascade Propotional Integral Differtional Controller (PID)

The Tyreus- Luyben [10] procedure is quite similar to the Ziegler–Nichols method but the final controller settings are different. Tyreus-Luyben PID Controller, the values of delay time, rise time, and settling time are better in comparison with Modified Ziegler-Nichols method. Also this method only proposes settings for PI and PID controllers. These settings that are based on ultimate gain and period are given in table 1.

Table 1 : Tyreus-Luyben settings

Controller	Kp	Ti	Td
PI	Kcr/3.2	2.2Pcr	
PID	Kcr/3.2	2.2Pcr	Pcr/6.3

For some control loops the measure of oscillation, provide by ¼ decay ratio and the corresponding large overshoots for set point changes are undesirable therefore more conservative methods are often preferable such as modified Z-N settings.

Table 2 : Modified Ziegler-Nichols settings

Controller	Kp	Ti	Td
PI	0.2Kcr	Pcr/2	
PID	0.2Kcr	Pcr/2	Pcr/3

a) Designed of PID Controller

PID controller is tuned by the proposed Tyreus-Luyben tuning methods.The PID controller has three term control signal

$$u(t) = K_p e(t) + \frac{K_p}{T_i}\int e(t)dt + K_p T_d \frac{de(t)}{dt}$$

$$Gc(s)=Kp(1+\frac{1}{T_i S}+T_d S)$$

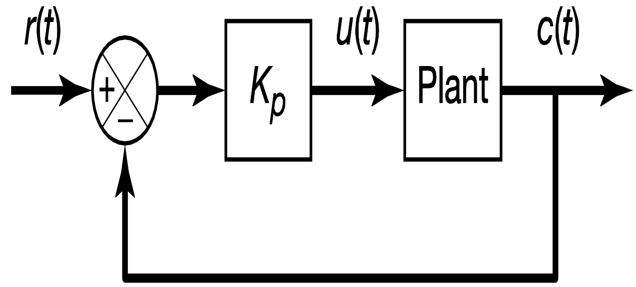

Figure 12 : PID controller is in proportional action

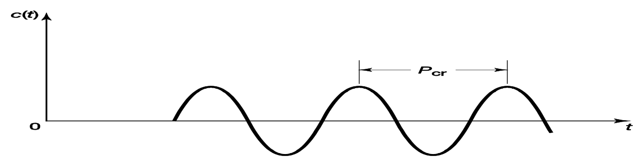

Figure 13 : Determination of sustained oscillation (P_{cr})

For selecting the proper controller parameters, Tyreus-Luyben Tuning Method is described below.

In this method, the parameter is selected as $T_i=\infty, T_d=0$. Using the proportional controller action [Fig.12]only increase K_p from 0 to a critical value $K_{cr.}$ At which the output first exhibits sustained oscillations [Fig.13]. Thus the critical gain K_{cr}& the corresponding period P_{cr} are experimentally determined.It is suggested that the values of the parameters K_p T_i T_d should set according to the following formula same as Zieglar-Nicles methods.

$$K_p=0.3125K_{cr}\ ,\ T_i=2.2P_{cr}\ ,\ T_d=0.159P_{cr}$$

Notice that the PID controller tuned by proposed Tyreus-Luyben tuning methods rules as follows,

$$Gc(s)=Kp(1+\frac{1}{T_i S}+T_d S)$$

$$Gc(s)=0.3125Kcr(1+\frac{1}{2.2PcrS}+0.159PcrS)$$

It's found that, $P_{cr}=0.2s$ & $K_{cr}=200$ [Fig.4]. So,

$$Gc(s)=\frac{1.98}{S} * (S^2+31.5S+71.6)$$

For selecting the proper controller parameters,Modified Ziegler-Nichols Tuning Method is described below.

In this method, the parameter is selected as $T_i=\infty, T_d=0$. Using the proportional controller action[Fig.14]only increase K_p from 0 to a critical value $K_{cr.}$ At which the output first exhibits sustained oscillations [Fig.14]. Thus the critical gain K_{cr} & the corresponding period P_{cr} are experimentally determined.It is suggested that the values of the parameters K_p T_i T_d should set according to the following formula .

$K_p=0.2K_{cr}$, $T_i=0.5P_{cr}$, $T_d=0.33P_{cr}$

Notice that the PID controller tuned by proposed Ziegler-Nichols tuning methods rules as follows,

$$Gc(s)=Kp\left(1+\frac{1}{T_i S}+T_d S\right)$$

$$Gc(s)=0.2Kcr\left(1+\frac{1}{0.5PcrS}+0.33PcrS\right)$$

It's found that, P_{cr}=0.2s & K_{cr}=200[Fig.4]. So,

$$Gc(s)=\frac{2.67}{S}*(S^2+15S+150)$$

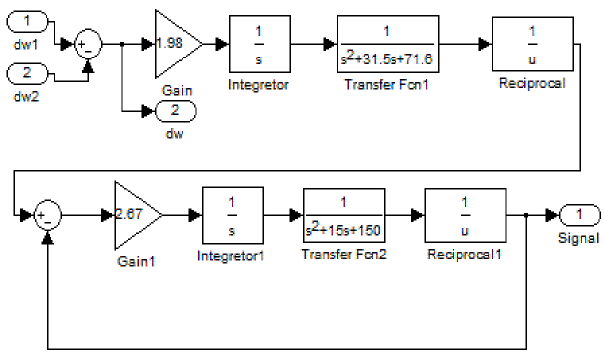

Figure 14 : Internal Structure of cascade PID controller with dω input

VI. Simulation Results

The network remains same [Fig.3], just simple UPFC is replaced by cascade PID controlled UPFC. It reduces damping of the power system oscillation & helps UPFC to improve stability. Two types of faults has been considered: A. Single line to ground fault and B. Three phase L-L fault.

a) Single line to ground fault

During 1-phase faults, if cascade PID is used as UPFC controller then, the system voltage becomes stable within 0.38s with 0% damping [Fig.15] & Power (P,Q) becomes stable within 1.2s&0.38s [Fig.16,17].

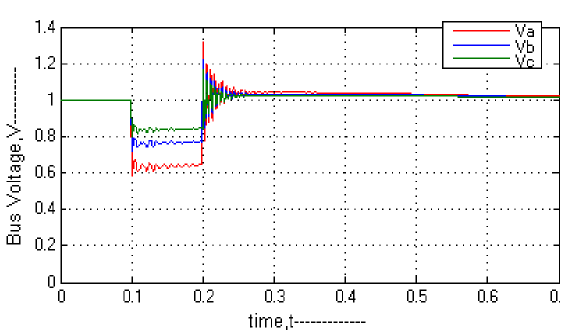

Figure 15 : Bus voltage in p.u for 1-Ø fault (with PID)

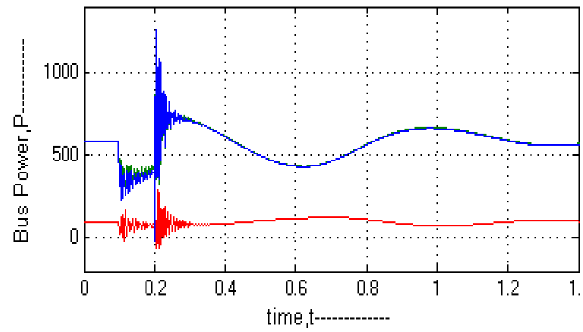

Figure 16 : Bus power, P in MW for 1-Ø fault (with PID)

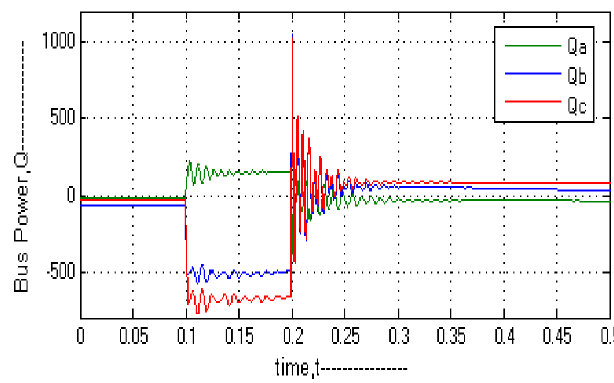

Figure17 : Bus Power, Q for 1-Ø fault in MW(with PID)

b) Three phase fault

During 3-phase faults, If cascade PID is used as UPFC controller then, the system voltage becomes stable within 0.4s [Fig.18] & Both power (P, Q) becomes stable within 1.3s& 0.4s [Fig.19, 20].

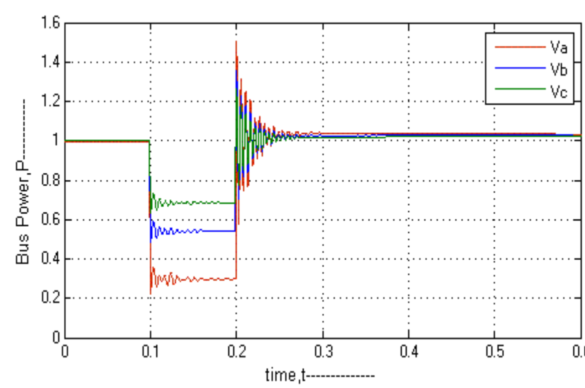

Figure 18 : Bus voltages in p.u for L-L fault (with PID)

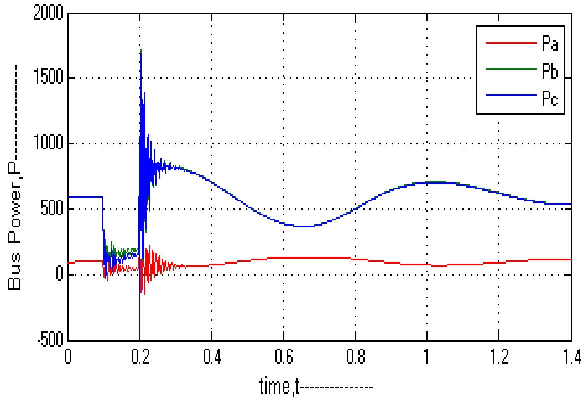

Figure 19 : Bus power, P in MW for L-L fault (with PID)

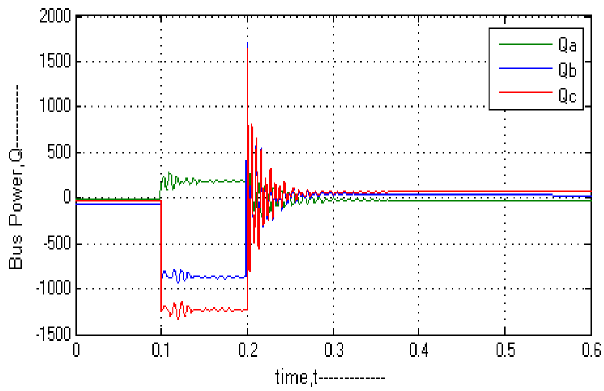

Figure 20 : Bus power, Q in MVAR for L-L fault (with PID)

VII. Results & Discussions

The performance of the proposed PID Controller with UPFC has been summarized in the table-II. In table-II, α (infinite time) means the system is unstable, UPFC rating in MVA. The network is simulated in three steps; without UPFC, With UPFC, UPFC with proposed PID Controller.

Table 2 : Performance of Proposed PID Controller

		Stability Time			
		1-Ø fault		3-Ø fault	
Status	UPFC Ratins	Volt	P, Q	Volt	P, Q
No UPFC	No	α	α	α	α
UPFC	100 MVA	1s	1.4s	1.2s	1.6s
UPFC+cascade PID	10 MVA	0.38s	1.2s,0.38s	0.4s	1.3s,0.4s

VIII. Conclusion

This paper presents the power system stability improvement i.e. voltage level, machine oscillation damping, real & reactive power in a power system model of UPFC without or with proposed cascade PID Controller for different types of faulted conditions. Cascade PID is also a very efficient controller then others for UPFC to enhance the power system stability. From above results, this proposed Tyreus-Luyben setting method for selecting for primary PID controller parameters and modified Ziegler-Nichols method for Secondary PID controller. In cascade PID Controller may be highly suitable as a UPFC controller because of shorter stability time, simple designed, low cost & highly efficient controller. Rather that, If cascade PID controller is used then only small rating of UPFC becomes enough for stabilization of robust power system within very shortest possible time for both steady state & dynamic conditions. These proposed cascade PID Controller can be applied for any interconnected multi-machine power system network for stability improvement. These controller can be applied to another FACTS devices namely SSSC, STATCOM, SVC whose controllers may be controlled externally by designing different types of controllers which also may be tuned by using different algorithm i.e. Fazzy logic,ANN, Genetic algorithm, FSO etc. for both transient and steady state stability improvement of a power system.

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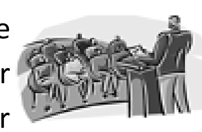

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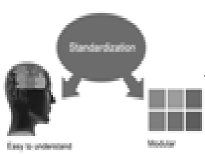

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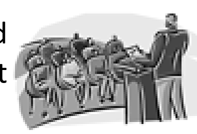

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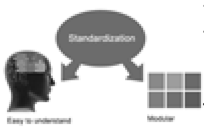

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Key points to remember:

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A purpose of organizing a research paper is to let people to interpret your effort selectively. The journal requires the following sections, submitted in the order listed, each section to start on a new page.

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What to keep away from

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The page length of this segment is set by the sum and types of data to be reported. Carry on to be to the point, by means of statistics and tables, if suitable, to present consequences most efficiently.You must obviously differentiate material that would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matter should not be submitted at all except requested by the instructor.

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- Explain results of control experiments and comprise remarks that are not accessible in a prescribed figure or table, if appropriate.
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- Not at all, take in raw data or intermediate calculations in a research manuscript.
- Do not present the similar data more than once.
- Manuscript should complement any figures or tables, not duplicate the identical information.
- Never confuse figures with tables - there is a difference.

Approach

- As forever, use past tense when you submit to your results, and put the whole thing in a reasonable order.
- Put figures and tables, appropriately numbered, in order at the end of the report
- If you desire, you may place your figures and tables properly within the text of your results part.

Figures and tables

- If you put figures and tables at the end of the details, make certain that they are visibly distinguished from any attach appendix materials, such as raw facts
- Despite of position, each figure must be numbered one after the other and complete with subtitle
- In spite of position, each table must be titled, numbered one after the other and complete with heading
- All figure and table must be adequately complete that it could situate on its own, divide from text

Discussion:

The Discussion is expected the trickiest segment to write and describe. A lot of papers submitted for journal are discarded based on problems with the Discussion. There is no head of state for how long a argument should be. Position your understanding of the outcome visibly to lead the reviewer through your conclusions, and then finish the paper with a summing up of the implication of the study. The purpose here is to offer an understanding of your results and hold up for all of your conclusions, using facts from your research and generally accepted information, if suitable. The implication of result should be visibly described. Infer your data in the conversation in suitable depth. This means that when you clarify an observable fact you must explain mechanisms that may account for the observation. If your results vary from your prospect, make clear why that may have happened. If your results agree, then explain the theory that the proof supported. It is never suitable to just state that the data approved with prospect, and let it drop at that.

- Make a decision if each premise is supported, discarded, or if you cannot make a conclusion with assurance. Do not just dismiss a study or part of a study as "uncertain."
- Research papers are not acknowledged if the work is imperfect. Draw what conclusions you can based upon the results that you have, and take care of the study as a finished work
- You may propose future guidelines, such as how the experiment might be personalized to accomplish a new idea.
- Give details all of your remarks as much as possible, focus on mechanisms.
- Make a decision if the tentative design sufficiently addressed the theory, and whether or not it was correctly restricted.
- Try to present substitute explanations if sensible alternatives be present.
- One research will not counter an overall question, so maintain the large picture in mind, where do you go next? The best studies unlock new avenues of study. What questions remain?
- Recommendations for detailed papers will offer supplementary suggestions.

Approach:

- When you refer to information, differentiate data generated by your own studies from available information
- Submit to work done by specific persons (including you) in past tense.
- Submit to generally acknowledged facts and main beliefs in present tense.

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	A-B	**C-D**	**E-F**
Abstract	Clear and concise with appropriate content, Correct format. 200 words or below	Unclear summary and no specific data, Incorrect form Above 200 words	No specific data with ambiguous information Above 250 words
Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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