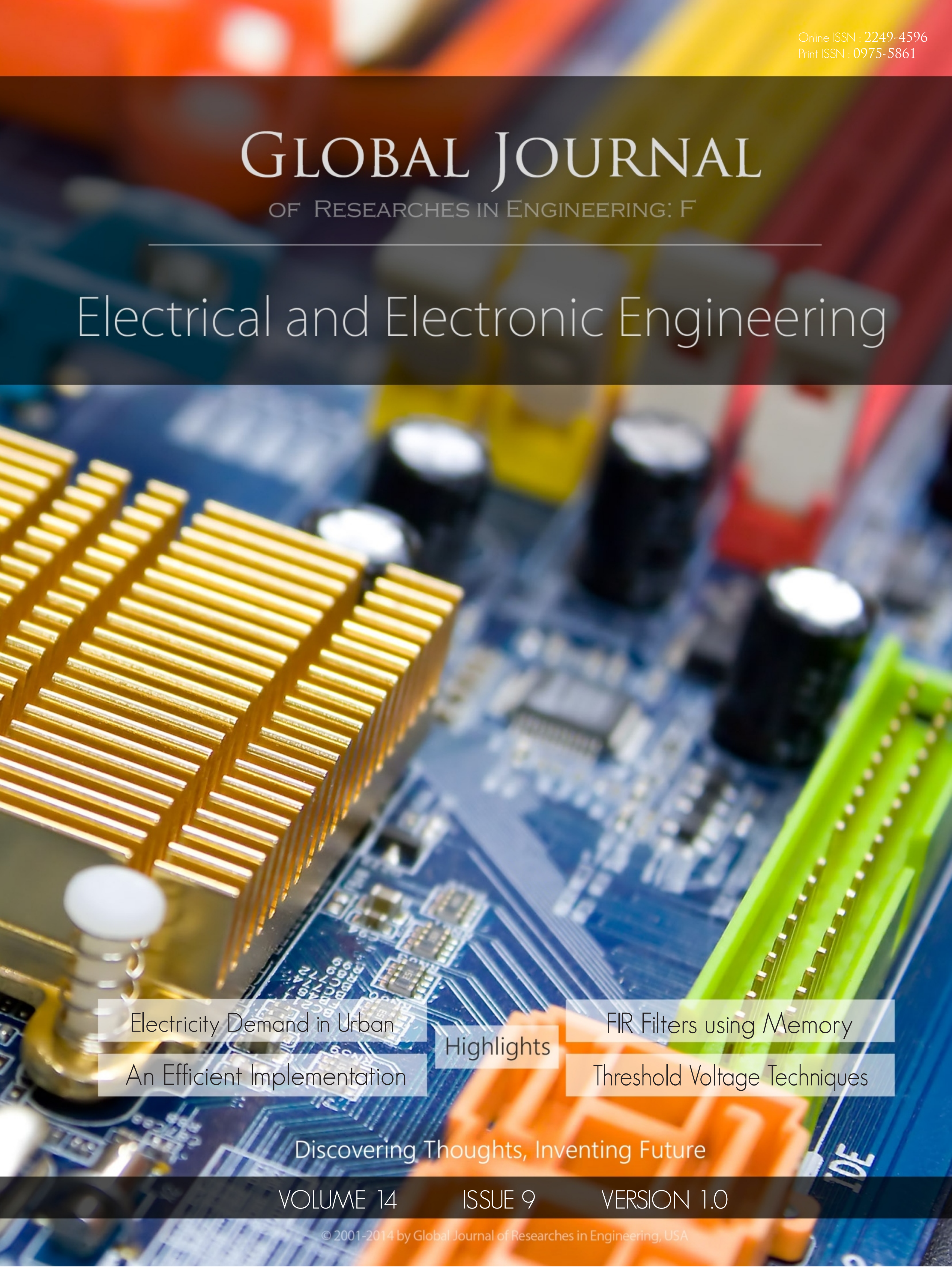

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Performance Analysis of Zero Forcing Equalizer in 2×2 and 3×3 MIMO Wireless Channel

By Tanvir Ahmed, Nezam Uddin & Motiur Rahaman
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Abstract- Wireless transmission is affected by fading and interference effects which can be combated with equalizer. The use of MIMO system promises good improvement in terms of spectral efficiency, link reliability and Signal to Noise Ratio (SNR). The effect of fading and interference always causes an issue for signal recovery in wireless communication. Equalization compensates for Inter-Symbol Interference (ISI) created by multipath within time dispersive channels. This paper analyzes the performance of Zero forcing method for MIMO wireless channels. The simulation results are obtained using MATLAB. The Bit Error Rate (BER) characteristics for the various transmitting and receiving antenna simulates in MATLAB and describes many advantages and disadvantages of the system. The simulation results show that the equalizer based zero forcing receivers is good for noise free channel and is successful in removing ISI.

Index Terms : *MIMO system, zero forcing equalizer, 2×2 MIMO channel, 3×3 MIMO channel, inter symbol interference (ISI), bit error rate (BER).*

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PERFORMANCEANALYSISOFZEROFORCINGEQUALIZERIN22AND33MIMOWIRELESSCHANNEL

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Performance Analysis of Zero Forcing Equalizer in 2×2 and 3×3 MIMO Wireless Channel

Tanvir Ahmed [α], Nezam Uddin [σ] & Motiur Rahaman [ρ]

Abstract- Wireless transmission is affected by fading and interference effects which can be combated with equalizer. The use of MIMO system promises good improvement in terms of spectral efficiency, link reliability and Signal to Noise Ratio (SNR). The effect of fading and interference always causes an issue for signal recovery in wireless communication. Equalization compensates for Inter-Symbol Interference (ISI) created by multipath within time dispersive channels. This paper analyzes the performance of Zero forcing method for MIMO wireless channels. The simulation results are obtained using MATLAB. The Bit Error Rate (BER) characteristics for the various transmitting and receiving antenna simulates in MATLAB and describes many advantages and disadvantages of the system. The simulation results show that the equalizer based zero forcing receivers is good for noise free channel and is successful in removing ISI.

Index Terms: MIMO system, zero forcing equalizer, 2×2 MIMO channel, 3×3 MIMO channel, inter symbol interference (ISI), bit error rate (BER).

I. Introduction

During the past there has been an explosion in wireless technology. This growth has opened a new dimension to future wireless communication whose ultimate goal is to provide universal personal and multimedia communication without regard to mobility or location with high data rates. To achieve such an objective, the next generation personal communication network will need to be support a wide range of services which will include high quality voice, data, facsimile, still pictures and streaming video. These future services are likely to include applications which require high transmission rates of several Mega bit per seconds (Mbps). The data rate and spectrum efficiency of wireless mobile communications have been improved over the last decade [1].

In mobile communication systems, data transmission at high bit rates is essential for many services such as video, high quality audio and mobile integrated service digital network. When the data is transmitted at high bit rates, over mobile radio channels, the channel impulse response can extend over many symbol periods, which lead to inter-symbol interference (ISI). This paper discuss the performances of equalization techniques by considering 2 transmitting and 2 receiving antenna case (resulting in a 2×2 MIMO channel) and 3 transmitting and 3 receiving antenna case (resulting in a 3x3 MIMO channel). Assume that the channel is a flat fading Rayleigh multipath channel and the modulation is BPSK. The ultimate goal is to provide universal personal and multimedia communication without regard to mobility or location with high data rates. To achieve such an objective we need a strong equalization technique to compensate ISI. Hence, there is need for the development of novel practical, low complexity equalization techniques and for understanding their potentials and limitations when used in wireless communication system characterized by very high rates, high mobility and the presence of multiple antennas [2].

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II. System Overview

a) *MIMO Systems Basics*

Multiple-Input Multiple-Output (MIMO) [5, 8] technology is a wireless technology that uses multiple transmitters and receivers to transfer more data at the same time shown inFig.1. MIMO technology takes advantage of a radio-wave phenomenon called multipath where transmitted information bounces off walls, ceilings, and other objects, reaching the receiving antenna multiple times via different angles and at slightly different times.

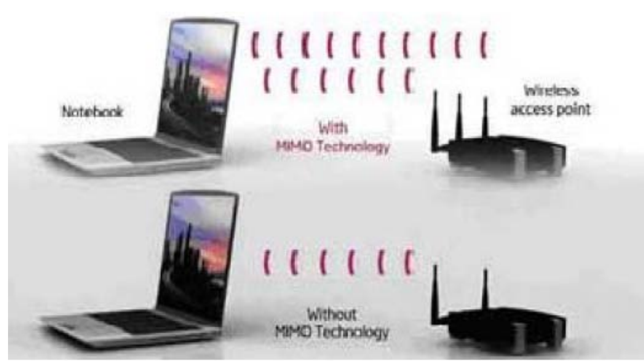

Fig. 1 : MIMO technology uses multiple radios to transfer more data at the same time

MIMO technology leverages multipath behaviour by using multiple, "smart" transmitters and receivers with an added "spatial" dimension to dramatically increase performance and range. MIMO allows multiple antennas to send and receive multiple spatial streams at the same time. MIMO makes antennas work smarter by enabling them to combine data streams arriving from different paths and at different times to effectively increase receiver signal-capturing power. Smart antennas use spatial diversity technology, which puts surplus antennas to good use. If there are more antennas than spatial streams, the additional antennas can add receiver diversity and increase range.

MIMO (multiple-in, multiple-out) takes advantage of multiplexing to increase wireless bandwidth and range. MIMO algorithms send information out over two or more antennas and the information is received via multiple antennas as well. On normal radio, multiplexing would cause interference, but MIMO uses the additional pathways to transmit more information and then recombines the signal on the receiving end. MIMO systems provide a significant capacity gain over conventional single antenna systems, along with more reliable communication. The benefits of MIMO lead many to believe it is the most promising of emerging wireless technologies.

MIMO system is represented by

$$Y=HX+N \qquad (1)$$

Hence,

X= Transmitting signal

Y= Received signal

H=Channel matrix

N= Noise vector.

i. *2×2 MIMO Channel*

In a 2×2 MIMO channel shown in Fig. 2, probable usage of the available 2 transmitting antennas can be as follows:

- Consider that we have a transmission sequence, for example$\{x_1, x_2, x_3 \ldots x_n\}$.
- In normal transmission, we will be sending x_1 in the first time slot, x_2 in the second time slot, x_3 and so on.
- However, as we now have 2 transmitting antennas, we may group the symbols into groups of two. In the first time slot, send x_1 and x_2 from the first and second antenna. In second time slot, send x_3 and x_4 from the first and second antenna send x_5 and x_6 in the third time slot and so on.
- Notice that as we are grouping two symbols and sending them in one time slot, we need only n/2 time slots to complete the transmission. Hence the data rate is doubled.
- This forms the simple explanation of a probable MIMO transmission scheme with 2 transmitting antennas and 2 receiving antennas. The two transmitted symbols interfered with each other and we will use zero forcing equalizer to minimize the interference.

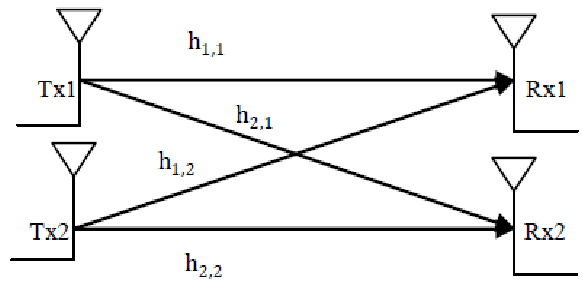

Fig. 2 : 2 transmit 2 receive (2 x 2) MIMO channel

b) *Other Assumptions*

- The channel is flat fading. In simple terms, it means that the multipath channel has only one tap. So, the convolution operation reduces to a simple multiplication [4].
- The channel experienced by each transmitting antenna is independent from the channel experienced by other transmitting antennas.
- For i^{th} the transmitting antenna to j^{th} receiving antenna, each transmitted symbol gets multiplied by a randomly varying complex number $h_{j,i}$. As the channel under consideration is a Rayleigh channel, the real and imaginary parts of hj, i are Gaussian n distributed having mean $\mu_{hj,i}$ =0and variance σ^2 $h_{j,i}$ =1/2 .
- The channel experienced between each transmitter to the receiving antenna is independent and randomly varying in time.
- On the receive antenna, the noise has the Gaussian probability density function with

$$p(n) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(n-\mu)^2}{2\sigma^2}}$$

With $\mu = 0$ and $\sigma^2 = \frac{N_o}{2}$

- The channel $h_{j,i}$ is known at the receiver.

i. *3×3 MIMO Channel*

In a 3×3 MIMO channel shown in Fig. 3, probable usage of the available 3 transmitting antennas can be as follows:

- Consider that we have a transmission sequence, for example$\{x_1, x_2, x_3 \ldots x_n\}$.
- In normal transmission, we will be sending x_1 in the first time slot, x_2 in the second time slot, x_3 and so on.
- However, as we now have 3 transmitting antennas, we may group the symbols into three groups. In the first time slot, send x_1, x_2 and x_3 from the first, second and third antenna. In second time slot, send x_4, x_5 and x_6 from the first, second and third antenna, send x_7, x_8 and x_9 in the third time slot and so on.4.

Notice that as we are grouping three symbols and sending them in one time slot, we need only n/3 time slots to complete the transmission. Hence the data rate is tripled.

- This forms the simple explanation of a probable MIMO transmission scheme with 3 transmitting antennas and 3receiving antennas. The three transmitted symbols interfered with each other and we will use zero forcing equalizer to minimize the interference.

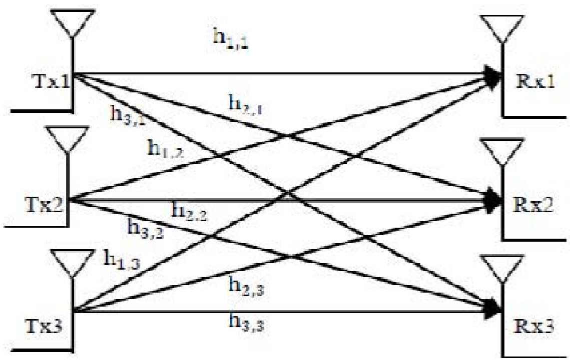

Fig. 3 : 3 transmit 3 receive (3 x 3) MIMO channel

Zero Forcing Equalizer [7] refers to a form of linear equalization algorithm used in communication systems which applies the inverse of the frequency response of the channel. This form of equalizer was first proposed by Robert Lucky. The Zero-Forcing Equalizer applies the inverse of the channel frequency response to the received signal, to restore the signal after the channel. It has many useful applications. For example, it is studied heavily for IEEE 802.11n (MIMO) where knowing the channel allows recovery of the two or more streams which will be received on top of each other on each antenna. The name Zero Forcing corresponds to bringing down the inter-symbol interference (ISI) to zero in a noise free case. This will be useful when ISI is significant compared to noise [3].

For a channel with frequency response (f) the zero forcing equalizer (f) is constructed by $(f) = 1/F(f)$. Thus the combination of channel and equalizer gives a flat frequency response and linear phase $F(f)\ C(f) = 1$. In reality, zero-forcing equalization does not work in most applications, for the following reasons: 1. Even though the channel impulse response has finite length, the impulse response of the equalizer needs to be infinitely long. 2. At some frequencies the received signal may be weak. To compensate, the magnitude of the zero-forcing filter ("gain") grows very large. As a consequence, any noise added after the channel gets boosted by a large factor and destroys the overall signal-to-noise ratio. Furthermore, the channel may have zeroes in its frequency response that cannot be inverted at all. (Gain * 0still equals 0). This second problem is often the more limiting condition. These problems can be addressed by making as mall modification to the denominator of (f): $(f) = 1/(F(f) + k)$ where k is related to the channel response and the signal SNR[6].If the channel response (or channel transfer function) for a particular channel is (s) then the input signal is multiplied by the reciprocal of it. This is intended to remove the effect of channel from the received signal, in particular the inter-symbol interference (ISI).

The zero-forcing equalizer removes all ISI, and is ideal when the channel is noiseless. However, when the channel is noisy, the zero-forcing equalizer will amplify the noise greatly at frequencies f where the channel response $(j2\pi f)$ has a small magnitude (i.e. near zeroes of the channel) in the attempt to invert the channel completely. A more balanced linear equalizer in this case is the minimum mean-square error equalizer, which does not usually eliminate ISI completely but instead minimizes the total power of the noise and ISI components in the output.

Let us now try to understand the math for extracting the two symbols which interfered with each other. In the first time slot, the received signal on the first receive antenna is,

$$y_1 = h_{1,1}x_1 + h_{1,2}x_2 + n_1 = [h_{1,1} \quad h_{1,2}]\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + n_1 \qquad (2)$$

The received signal on the second receive antenna is,

$$y_1 = h_{2,1}x_1 + h_{2,2}x_2 + n_2 = [h_{2,1} \quad h_{2,2}]\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + n_2 \qquad (3)$$

where

y_1, y_2 are the received symbol on the first and second antenna respectively,

$h_{1,1}$ is the channel from 1st transmit antenna to 1st receive antenna,

$h_{1,2}$ is the channel from 2nd transmit antenna to 1streceive antenna,

$h_{2,1}$ is the channel from 1st transmit antenna to 2nd receiveantenna,

$h_{2,2}$ is the channel from 2nd transmit antenna to 2nd receive antenna,

x_1, x_2 are the transmitted symbols and

n_1, n_2 is the noise on 1st, 2nd receive antennas.

We assume that the receiver knows $h_{1,1}$, $h_{1,2}$, $h_{2,1}$ and$h_{1,2}$. The receiver also knows $y_1$and y_2. The unknowns arex1and x_2. With two equations and two unknowns we cansolve it.

For convenience, the above equation can be represented in matrix notation as follows:

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} h_{1,1} & h_{1,2} \\ h_{2,1} & h_{2,2} \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} n_1 \\ n_2 \end{bmatrix} \qquad (4)$$

Equivalently,

$$y = Hx + n \qquad (5)$$

To solve for, we know that we need to find a matrix Wwhich satisfies WH + I.

The Zero Forcing (ZF) linear detector for meeting this constraint is given by,

$$W = (H^H H)^{-1} H^H \quad (6)$$

This matrix is also known as the pseudo inverse for a general m x n matrix. The term,

$$\begin{bmatrix} h_{1,1}^* & h_{2,1}^* \\ h_{1,2}^* & h_{2,2}^* \end{bmatrix} \begin{bmatrix} h_{1,1} & h_{1,2} \\ h_{2,1} & h_{2,2} \end{bmatrix} = \begin{bmatrix} |h_{1,1}|^2 + |h_{2,1}|^2 & h_{1,1}^* h_{1,2} + h_{2,1}^* h_{2,2} \\ h_{1,2}^* h_{1,1} + h_{2,2}^* h_{2,1} & |h_{1,2}|^2 + |h_{2,2}|^2 \end{bmatrix} \quad (7)$$

ii. *Zero forcing (ZF) equalizer for 3×3 MIMO channel*

Let us now try to understand the math for extracting the two symbols which interfered with Each other for 3×3 MIMO channel. In the first time slot, the received signal on the first receive antenna is,

$$y_1 = h_{1,1}x_1 + h_{1,2}x_2 + h_{1,3}x_3 + n_1 = [h_{1,1}\ h_{1,2}\ h_{1,3}] \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + n_1 \quad (8)$$

The received signals on the second and third receive antenna are,

$$y_2 = h_{2,1}x_1 + h_{2,2}x_2 + h_{2,3}x_3 + n_2 = [h_{2,1}\ h_{2,2}\ h_{2,3}] \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + n_2 \quad (9)$$

$$y_3 = h_{3,1}x_1 + h_{3,2}x_2 + h_{3,3}x_3 + n_3 = [h_{3,1}\ h_{3,2}\ h_{3,3}] \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + n_3 \quad (10)$$

where

y_1, y_2 and y_3 are the received symbol on the first, second and third antenna respectively,

$h_{1,1}$ is the channel from 1st transmit antenna to 1st receive antenna,

$h_{1,2}$ is the channel from 2nd transmit antenna to 1st receive antenna,

$h_{1,3}$ is the channel from 3rd transmit antenna to 1st receive antenna,

$h_{2,1}$ is the channel from 1st transmit antenna to 2nd receive antenna,

$h_{2,2}$ is the channel from 2nd transmit antenna to 2nd receive antenna,

$h_{2,3}$ is the channel from 3rd transmit antenna to 2nd receive antenna,

$h_{3,1}$ is the channel from 1st transmit antenna to 3rd receive antenna,

$h_{3,2}$ is the channel from 2nd transmit antenna to 3rd receive antenna,

$h_{3,3}$ is the channel from 3rd transmit antenna to 3rd receive antenna,

x_1, x_3 and x_3 are the transmitted symbols and n_1, n_2 and n_3 are the noise on 1st, 2nd and 3rd receive antennas respectfully.

We assume that the receiver knows $h_{1,1}$, $h_{1,2}$, $h_{1,3}$, $h_{2,1}$, $h_{2,2}$, $h_{2,3}$, $h_{3,1}$, $h_{3,2}$, and $h_{3,3}$. The receiver also knows y_1, y_2 and y_3. The unknowns are x_1, x_3 and x_3. With three equations and three unknowns we can solve it.

For convenience, the above equation can be represented in matrix notation as follows:

$$\begin{bmatrix} y_1 \\ y_2 \\ y_3 \end{bmatrix} = \begin{bmatrix} h_{1,1} & h_{1,2} & h_{1,3} \\ h_{2,1} & h_{2,2} & h_{2,3} \\ h_{3,1} & h_{3,2} & h_{3,3} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}$$

Equivalently,

$$y = Hx + n \quad (11)$$

To solve for x, we know that we need to find a matrix which satisfies WH +I.

The Zero Forcing (ZF) linear detector for meeting this constraint is given by,

$$W = (H^H H)^{-1} H^H \quad (12)$$

iii. *BER with ZF equalizer with 2×2and 3×3 MIMO*

Note that the off diagonal terms in the matrix HHH are not zero. Because the off diagonal terms are not zero, the zero forcing equalizer tries to null out the interfering terms when performing the equalization, i.e. when solving for x_1 the interference from x_2 is tried to be nulled and vice versa While doing so, there can be amplification of noise. Hence Zero Forcing equalizer is not the best possible equalizer to do the job. However, it is simple and reasonably easy to implement. Further, it can be seen that, following zero forcing equalization, the channel for symbol transmitted from each spatial dimension (space is antenna) is a like a 1×1 Rayleigh fading channel. Hence the BER for 2×2 and 3×3MIMO channel in Rayleigh fading with Zero Forcing equalization is same as the BER derived for a 1×1 channel in Rayleigh fading [4].

For BPSK modulation in Rayleigh fading channel, the bit error rate is derived as,

$$P_b = \sqrt{\frac{\left(\frac{E_b}{N_0}\right)}{\left(\frac{E_b}{N_0}\right)+1}} \quad (13)$$

III. Result and Discussion

As expected, the simulated results with a 2×2 MIMO system using BPSK modulation in Rayleigh channel is showing matching results as obtained in for a 1×1 system for BPSK modulation in Rayleigh channel shown in Fig. 4. The ZF equalizer helps us to achieve the data rate gain, but not take advantage of diversity gain (as we have two receiving antennas). We might not be able to achieve the two fold data rate improvement in all channel conditions. It can so happen that channels are correlated (the coefficients are almost the same).

BER for BPSK modulation with 2x2 MIMO and ZF equalizer (Rayleigh channel)

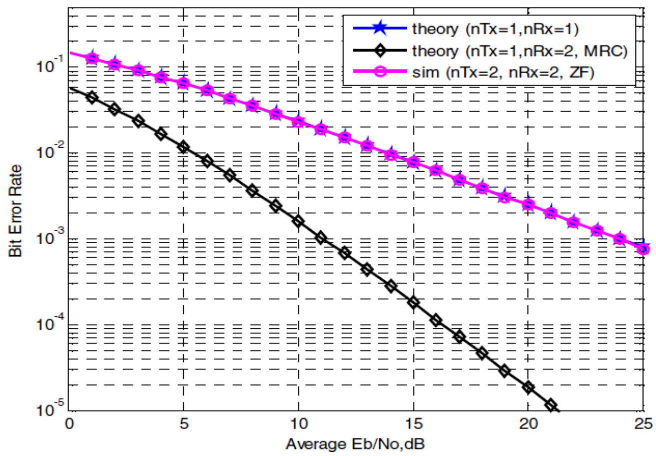

Fig. 4 : BER plot for 2x2 MIMO channel with ZF equalizer (BPSK modulation in Rayleigh channel)

Hence we might not be able to solve for the two unknown transmitted symbols even if we have two received symbols. In case of 3x3 MIMO shown in Fig. 5 has some discontinuity due to interference effect.

BER for BPSK modulation with 3x3 MIMO and ZF equalizer (Rayleigh channel)

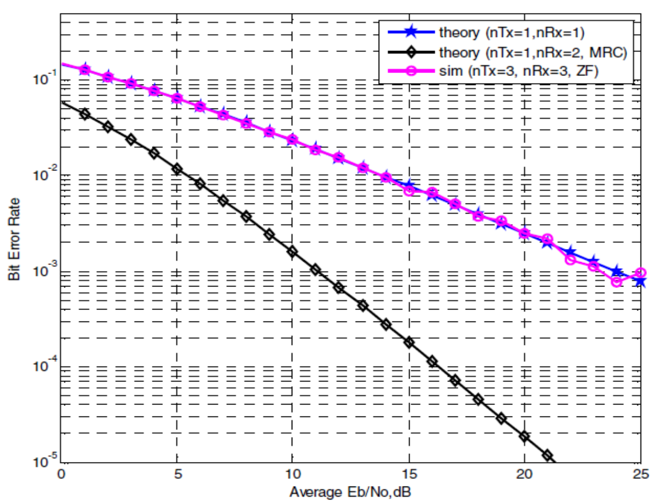

Fig. 5 : BER plot for 3x3 MIMO channel with ZF equalizer(BPSK modulation in Rayleigh channel)

IV. Conclusions

This paper presents a simulation study on the performance analysis of ZF equalizer based MIMO receiver. The simulation result shows the BER characteristics for the ZF equalizer. From the simulation result we can summarize that, ZF equalization in addition of noise gets boosted up and thus spoils the overall signal to noise ratio. Hence it is considered good to a receiver under noise free conditions. The multiple antennas are used to increase data rates through multiplexing or to improve performance through diversity. This technique offers higher capacity to wireless systems and the capacity increases linearly with the number of antennas and link range without additional bandwidth and power requirements.

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An Efficient Implementation of Digit FIR Filters using Memory based Realization

By Maloth Santhoshi, Mrs. E. P. Vanetha & P. Srikanth
Vardhaman College of Engineering, India

Abstract- The main contribution of this paper is an exact common sub expression elimination algorithm for the optimum sharing of partial terms in multiple constant multiplications (MCMs).Although many efficient high-level algorithms have been proposed for the realization of Multiple Constant Multiplications (MCM) using the fewest number of addition and subtraction operations, they do not consider the low-level implementation issues that directly affect the area, delay, and power dissipation of the MCM design. It is found that the proposed LUT-based multiplier involves comparable area and time complexity for a word size of 8 bits, but for higher word sizes, it involves significantly less area and less multiplication time than the canonical-signed-digit (CSD)-based multipliers we have proposed the anti symmetric product coding (APC) and odd-multiple-storage (OMS) techniques for lookup-table (LUT) design for memory-based multipliers to be used in digital signal processing applications. It was observed that the proposed algorithm obtains better solutions in terms of area than the algorithms designed for the MCM problem and the optimization of area problem in a digit-serial MCM operation at gate-level.

Keywords: digital signal processing (DSP), finite impulse response (FIR) filter, multiple constant multiplication, lut-based computing, VLSI design.

GJRE-F Classification : FOR Code: 090699

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An Efficient Implementation of Digit FIR Filters using Memory based Realization

Maloth Santhoshi [α], Mrs. E. P. Vanetha [σ] & P. Srikanth [ρ]

Abstract- The main contribution of this paper is an exact common sub expression elimination algorithm for the optimum sharing of partial terms in multiple constant multiplications (MCMs).Although many efficient high-level algorithms have been proposed for the realization of Multiple Constant Multiplications (MCM) using the fewest number of addition and subtraction operations, they do not consider the low-level implementation issues that directly affect the area, delay, and power dissipation of the MCM design. It is found that the proposed LUT-based multiplier involves comparable area and time complexity for a word size of 8 bits, but for higher word sizes, it involves significantly less area and less multiplication time than the canonical-signed-digit (CSD)-based multipliers we have proposed the anti symmetric product coding (APC) and odd-multiple-storage (OMS) techniques for lookup-table (LUT) design for memory-based multipliers to be used in digital signal processing applications. It was observed that the proposed algorithm obtains better solutions in terms of area than the algorithms designed for the MCM problem and the optimization of area problem in a digit-serial MCM operation at gate-level.

Keywords: digital signal processing (DSP), finite impulse response (FIR) filter, multiple constant multiplication, lut-based computing, VLSI design.

I. Introduction

There are many hand-held products that include digital signal processing (DSP), for example, cellular phones and hearing aids. For this type of portable equipment a long battery life time and low battery weight is desirable.

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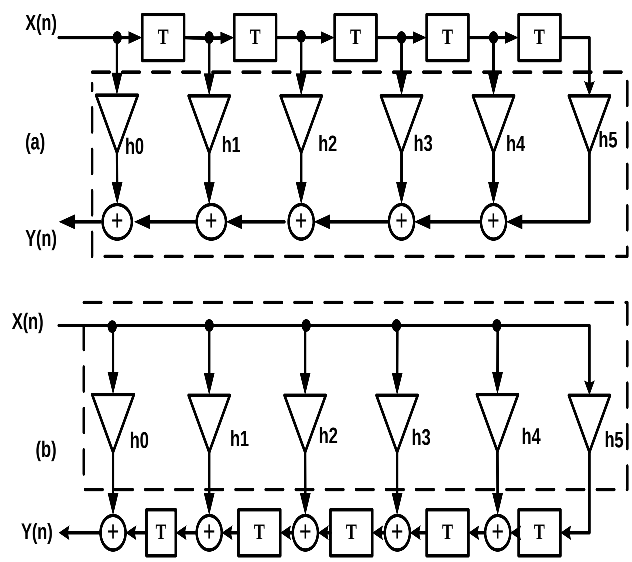

Fig. 1. (a) Direct and (b) Transposed direct form

To obtain this the circuit must have low power consumption. The main issue in this thesis is to minimize the energy consumption per operation for the arithmetic parts of DSP circuits, such as digital filters. More specific, the focus will be on single and multiple-constant multiplication using serial arithmetic.

a) Fir Filter Design

If the impulse response becomes zero after a finite number of samples it is a finite-length impulse response (FIR) filter.

For a given specification the filter order, N, is usually much higher for an FIR filter than for an IIR filter. However, FIR filters can be guaranteed to be stable and to have a linear phase response, which corresponds to constant group delay.

Different realizations of a fifth-order (five tap) FIR filter. (a) Direct form and (b) transposed direct form. It is not recommended to use recursive algorithms to realize FIR filters because of stability problems. Hence, here all coefficients bk in (1.1) is assumed to be zero. If an impulse is applied at the input each output sample will be equal to the corresponding coefficient ak, i.e., the impulse response is the same as the coefficients. The transfer function of an Nth-order FIR filter can then be written as

$$H(z) = \sum_{k=n}^{N} h(k)\, z^{-k}$$

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A direct realization for N = 5 is shown in Fig. 1(a). This filter structure is referred to as a direct form FIR filter. If the signal flow graph is transposed the filter structure in Fig. 1.1 (b) is obtained, referred to as transposed direct form [2]. The dashed boxes in Figs. 1 (a) and (b) mark a sum-of-product block and a multiplier block, respectively. In both cases, the part that is not included in the dashed box is referred to as the delay section and the adders in Fig.1 (b) are called structural adders.

b) Bit-Serial Multiplier

In bit-serial arithmetic, the numbers are commonly processed with the least significant bit first. In bit-serial addition the two's complement numbers are added sequentially bit-by-bit by a full adder controlled by the clock clk as shown in Fig. 2.a. The full adder produces a sum bit and a carry bit. The carry has to be saved by the D flip-flop in order to be added to the input words on the next higher significant level in the next clock cycle. At the start of the computation, the input carry bit should be cleared, which is controlled by the signal. This circuit is called Carry-Save Adder (CSA) since there is no carry propagation. Hence the circuit can be used at high clock rates compared to parallel adders. The sum will be available after the propagation time of the full adder t add 0, hence this adder is of latency model order 0. An adder with LM 1 is realized by pipelining with a D flip-flop at the sum output shown in Fig.2.b. The minimum clock period is determined by the delay of the full adder and the propagation delay of the D flip-flop, t add 1.

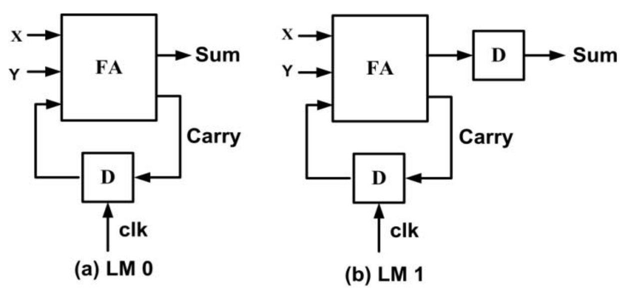

Fig. 2 : Bit-serial adders with LM 0 and LM 1

The algorithms designed for the MCM problem can be categorized in two classes: common sub expression elimination (CSE) algorithms [1]–[4] and graph-based (GB) techniques [2]–[4]. The CSE algorithms initially extract all possible sub expressions from the representations of the constants when they are defined under binary, canonical signed digit (CSD) [7], or minimal signed digit (MSD) [8]. Then, they find the "best" sub expression, generally the most common, to be shared among the constant multiplications. The GB methods are not limited to any particular number representation and consider a larger number of alternative implementations of a constant, yielding better solutions than the CSE algorithms. There is a disadvantage by implementing these algorithm the circuit complicity increases.

In order to avoid costly multipliers, most prior hardware implementations of digital FIR filters can be divided into two categories: multiplier less based and memory based. Multiplier less-based designs realize MCM with shift-and add operations and share the common sub operations using canonical signed digit (CSD) recoding and common sub expression elimination (CSE) to minimize the Adder cost of MCM.

In [8] and [9], more area savings are achieved by jointly considering the optimization of coefficient quantization and CSE. Most multiplier less MCM-based FIR filter designs use the transposed structure to allow for cross-coefficient sharing and tend to be faster, particularly when the filter order is large. However, the area of delay elements is larger compared with that of the direct form due to the range expansion of the constant multiplications and the subsequent additions in the SAs. Memory-based FIR designs consist of two types of approaches: lookup table (LUT) methods and distributed arithmetic (DA) methods [4]–[5]. The LUT-based design stores in ROMs odd multiples of the input signal to realize the constant multiplications in MCM [11].The DA-based approaches recursively accumulate the bit-level partial results for the inner product computation in FIR filtering [4], [5].

The remainder of the paper is organized as follows. In Section II, we have presented the proposed design of Architecture. In Section III, We have described the modules used in the proposed design for LUT Based multiplier in Section IV, Simulation results and FIR filter are evaluated and compared Conclusions are presented in Section V.

II. Proposed Architecture

A conventional lookup-table (LUT)-based multiplier is shown in Fig.4, where *A* is a fixed coefficient, and *X* is an input word to be multiplied with *A*. Assuming *X* to be a positive binary number of word length L, there can be 2^L possible values of *X* , and accordingly, there can be 2^L possible values of product $C = A \cdot X$. Therefore, for memory-based Multiplication, an LUT of 2L words, consisting of precomputed product values corresponding to all possible values of X,

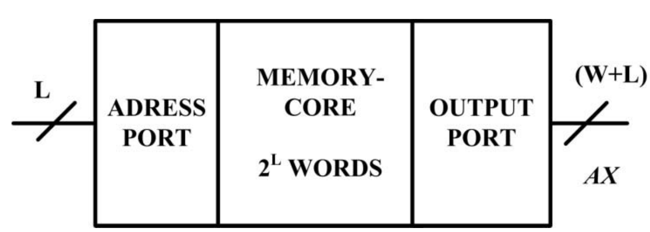

Fig. 3 : Conventional LUT-based multiplier

is The product word $A \cdot X_l$ is stored at the location X_l for $0 \le X_l \le 2^L - 1$, such that if an L-bit binary value of X_l is used as the address for the LUT, then the corresponding product value *A · Xl* is available as its output.

Memory based Computing: A class of dedicated systems, where the computational functions are performed by lookup tables (LUTs) instead of actual calculations .It close to human-like computing. Simple to design, and more regular compared with the multiply-accumulate structures. Involve less dynamic power consumption due to minimization of switching activities. It has potential for high-throughput and reduced latency implementation.

Memory-based computations examples Inner-product computation using the distributed arithmetic (DA) direct implementation of constant multiplications implementation of fixed and adaptive FIR filters and transforms well-suited for digital filtering and orthogonal. Transformations for digital signal processing and other applications: evaluation of trigonometric functions, sigmoid and other nonlinear function. The disadvantage of DA is filter with N coefficients the LUT has 2 N values. For higher order filter LUT size will increase, it required more memory space. The significant work on LUT optimization for memory-based multiplication, recently we have presented a new approach to LUT design, where only the odd multiples of the fixed coefficient are required to be stored [9], which we have referred to as the *odd-multiple-storage* (OMS).

The multiplication of any binary word *X* of size *L,* with a fixed coefficient A, instead of storing all the 2*L* possible values of $C = A \cdot X$, only (2^L /2) words corresponding to the odd multiples of A may be stored in the LUT, while all the even multiples of A could be derived by left-shift operations of one of those odd multiples. Based on the above assumptions, the LUT for the multiplication of an L-bit input with a W–bit coefficient could be designed by the Following strategy.

a) A memory unit of [(2^L/2) +1] words of (W+L) –bit width is used to store the product values, where the first (2^L/2) words are odd multiples of A, and the last word is zero.

b) A barrel shifter for producing a maximum of (L-1) left shifts is used to derive all the even multiples of A.

Table 1 : Look up table to multiples a 4-bit word word*with a constant

Address Word, X	Product word	Address Word, X	Product word
0000	0	1000	8A
0001	A	1001	9A
0010	2A	1010	10A
0011	3A	1011	11A
0100	4A	1100	12A
0101	5A	1101	13A
0110	6A	1110	14A
0111	7A	1111	15A

c) The L-bit input word is mapped to the (L-1) bit address of the LUT by an address encoder, and control bits for the barrel shifter are derived by a control circuit.

III. Modules used in the Proposed Design for LUT based Multiplier

a) Address Generator and Control Circuit

The address generation and control circuit used to produce the address d0d1d2d3. This address is given as the input to LUT component. The address generation circuit is generally used in conjunction with the control circuit which is used to produce the control signals s0and s1. The control signals are used in the subsequent blocks as can be seen from Fig. 3., for the multiplication of any binary word of size L, with a fixed coefficient A, instead of storing all the 2L possible values of C=A*X, only (2L/2) words corresponding to the odd multiples of A may be stored in the LUT, while all the even multiples of A could be derived by left-shift operations of one of those odd multiples. This can be achieved with of one of the modules i.e. Barrel Shifter.

b) Barrel Shifter Module

In Table 1, at eight memory locations, the eight odd multiples, A × (2i + 1), are stored. The even multiples 2A, 4A and 8A are derived by left-shift operations of A. 6A and 12A are derived by left shifting operation of 3A. 10A and 14A are derived by left shifting 5A and 7A, respectively. Three left-shift operations can be produced by a barrel shifter to derive all the multiplier.

c) LUT Component Module

The LUT component for multiplication of a 4-bit unsigned input consists of a set of eight odd multiple values of a fixed coefficient, say 4, i.e. 4, 12, 20, 28, and so on. Also, for 8-bit signed input, the LUT component has the above values as well as another set of odd multiple stored values such as 196, 200, and so on till 256. As a result, LUT size is considerably reduced. The design of hardware efficient and high throughput FIR filter has become much more demanding. In conventional design, however, the multipliers in the structure require a large portion of chip-area, and accordingly, the delay of the structure is large due to the large time required in multiplication. Multiplier less memory-based techniques [3]-[10] has been widely used in many applications, in recent years, for their high throughput processing and cost-effective structures.

Memory based multiplier implementation of multiplications can be performed by using CAD tools computing. In this paper, a new approach to LUT implementation for memory-based multiplication was proposed [11]. Though the approach proposed in [11] is efficient in implementation, the approach can be improved further. For example, it is noticed that there was an address encoder and a control circuit in the architecture [11, Fig. 5], which may increase the chip area. Therefore, if we could improve the memory-based technique, we may get a hardware efficient structure for implementation. In this paper, we aim at presenting a new memory-based technique to replace the conventional direct LUT for hardware-efficient implementation. In FIR filtering, one of the convolving sequences is the input samples while the other is the fixed coefficients of the filter. This behavior of the FIR filter makes it possible for memory-based multiplication realization. It yields faster output compared with the multiplier-based designs because it stores the pre-computed results in the memory units, which can be read out and accumulated to obtain the result. This memory based technique has two major features. *First,* it suits well for any number of input word lengths. And any N number of coefficients can be multiplied and stored in a specified address location and it shows shifting operation of given variables. *Second,* the whole structure can be decomposed into a number of small units, which can be extended further to obtain a high-throughput structure for FIR filter implementation. Multiplication of an 8-bit input with a W-bit fixed coefficient can be performed through a pair of multiplications using a dual-port memory of 8 words (or two single-port memory units) along with a pair of decoders, encoders, NOR cells and barrel shifters as shown in Fig. 5. The shift-adder performs left-shift operation of the output of the barrel-shifter corresponding to more significant half of input by eight bit-locations, and adds that to the output of the other barrel-shifter.

The proposed system technique is it multiples the N no. of variables with N no. of coefficient and reduces the memory size and stores it in a specified location by performing the conditional operations of the given code instruction. For an 8-bit input variable in this system initially we have to initiate the input 8-bit input variable and 4-bit filter coefficient. The input variable and filter coefficient multiples and gives the product output. The product output stored address location and shifting operation can be seen in the simulation results.

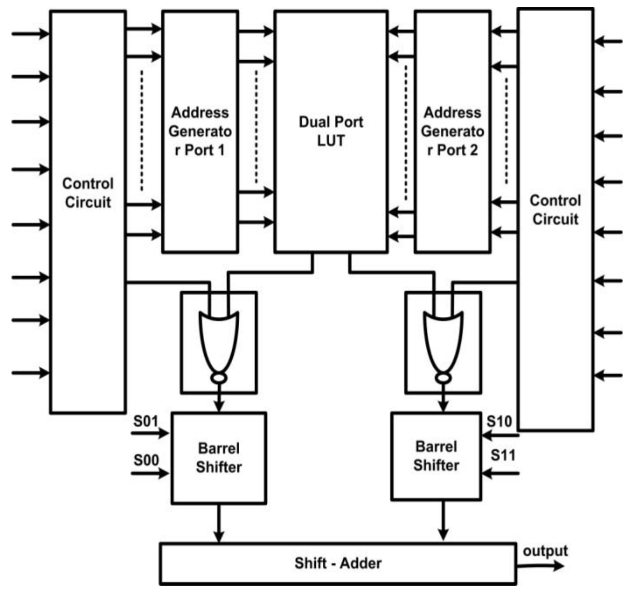

Fig. 5 : The shift-adder performs left-shift Operation of the output of the barrel-shifter

The hardware operation is reduces the partial products, so the area is reduces and the speed or performance of the designs increase Similar for a 16-bit variable function it performs same operation. Additionally by using the clock performs of the circuit is having potential for high-throughput and reduced latency implementation Low complexity in the circuit design. A modified hardware-efficient approach for Memory based multiplication is proposed. The proposed approach is less hardware complexity than the existing memory less-based design for multiplication. Then the proposed approach is applied in the FIR filter. Thus it can be readily used as an IP core in a number of environments, especially for those high-order filters. Further work may concern about the more efficient design for multiplication.

IV. Simulations Results

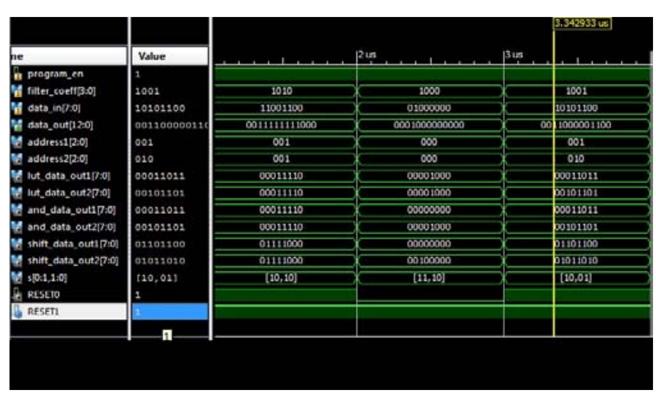

Fig. 6 : Simulation result of 8 bit LUT based FIR filter

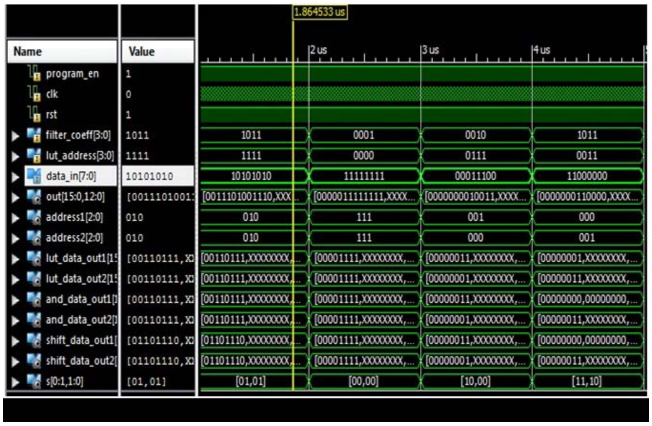

Fig. 7 : Simulation result of 16-bit LUT

Table 2 : Summary report of LUT

FIR filter design	No. of slices utilization out of 2448	No. of 4 input LUT out of 4896	Number of bonded IOBs out of 92
6-bit LUT based	6%	6	28
Proposed 8-bit memory based LUT	3%	3	28
16- bit memory based LUT	42%	36	39

V. Conclutions

In this paper, we have shown the possibility of using LUT based multipliers to implement the constant multiplication for DSP applications. It was observed that the proposed algorithm obtains better solutions in terms of area than the algorithms designed for the MCM problem and the optimization of area problem in a digit-serial MCM operation at gate-level. It was also shown that the realization of digit-serial FIR filters under the shift-adds architectures yields significant area and power reductions when compared to those whose multiplier blocks are implemented using digit-serial constant multipliers.

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Electricity from Municipal Waste: A Potential Way to Meet up the Electricity Demand in Urban Bangladesh

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Abstract- Electricity is much more important for the development of a country & its countryman. Electricity is the key to development. Most of the people in Bangladesh are migrating from rural areas to urban areas in search of a better life. As a result the demand of electricity in urban areas in Bangladesh is increasing day by day. But the Govt. has less alternative to meet up the huge demand of electricity in urban areas. In this paper a comparative study is taken to generate electricity from municipal waste which is also in an increasing rate in urban areas because of over population. By sorting out the municipal solid waste and through anaerobic process we can generate biogas which will lead to generate electricity. In this paper, this electricity generation process is described along with annual municipal waste data in different urban areas in Bangladesh to give a road map to the proper authority so that they may find it helpful to meet up the increasing demand of electricity in urban Bangladesh.

Keywords: municipal solid waste, waste management process, bio degradable waste, bio gas, gas generator.

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ELECTRICITYFROMMUNICIPALWASTEAPOTENTIALWAYTOMEETUPTHEELECTRICITYDEMANDINURBANBANGLADESH

Electricity from Municipal Waste: A Potential Way to Meet up the Electricity Demand in Urban Bangladesh

Md. Risat Abedin [α], Ajwad Muhtasim [σ] & Faysal Alam [ρ]

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Keywords: municipal solid waste, waste management process, bio degradable waste, bio gas, gas generator.

I. Introduction

Bangladesh is a densely populated country having a population of approximately 150 million [1]. It is one of the most promising developing countries in the world. The economic development of a country largely depends on the establishment of new industries. The availability of electricity gives pace to the establishment of new industries. Again in search of job and better life, a large number of people are migrating from rural to urban areas in Bangladesh. This makes a huge pressure of electricity demand – supply ratio in urban areas. For the shifted citizens and the newly established industries, Govt. has to arrange more electricity. But unfortunately the sources of electricity generation are very much limited. Moreover the conventional sources of electricity generation like coal; gases etc. are decreasing day by day. So, govt. has to find out better alternatives to supply the huge electricity demand in urban areas to continue the development process.

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II. Current Urbanization Process & Electricity Situation in Bangladesh

In search of living, a great many people are shifting from rural areas to urban areas in Bangladesh. A survey indicates that in 1990 Bangladesh has a rural population of 92736985.1 where in 2010 it is 106909642.2 and the population growth rate in rural area is 0.5 % in 2010 [2]. On the other hand in 1990 Bangladesh has a urban population of 22895165.9 where in 2010 it is 41782488.8 and the annual growth rate in urban area is 2.9 % in 2010 [2] . So it is clearly indicating that the population is increasing much more rapidly in urban areas than the rural areas. Figure 1 shows the urban population situation in Bangladesh. [2]

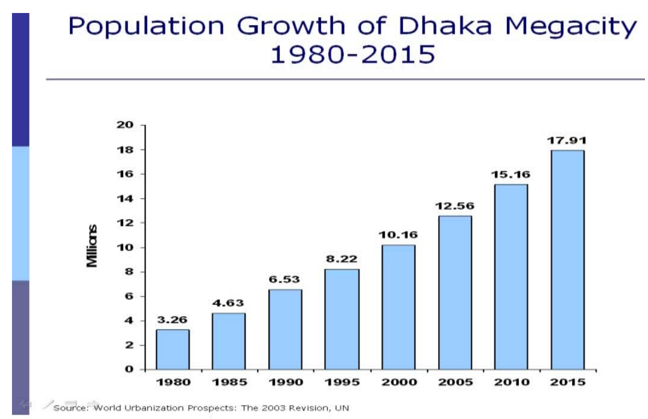

Figure 1 : Urban Population (Dhaka City) in Bangladesh

On the other hand though Bangladesh govt. is trying its best, but the demand – supply ratio of electricity is not satisfactory here. According to Bangladesh Power Development Board (BPDB) report, on 9 Sep -2014, maximum demand (substation end) at evening peak hour was 6356 MW whereas the maximum generation at evening peak hour was 6133 MW [3]. Table 1 shows a comparative study of demand and load shedding behaviour in different areas in Bangladesh [4].

Table I : Demand & Load Shed in Different Areas in Bangladesh as on 10/09/2014 [4]

AREA	Demand (MW)	Load Shed (MW)
Dhaka	2590	249
Chittagong	682	99
Khulna	730	112
Rajshahi	715	103
Comilla	440	70
Mymensing	370	45
Sylhet	320	28
Barisal	140	16
Rangpur	365	53
Total	6352	775

III. Definition of Wastes

Waste is termed as unwanted material. Waste and wastes can be various types like municipal solid waste (household thrash / refuse), hazardous waste, waste water, radioactive waste, and so on. According to the Basel Convention, "'Wastes' are substances or objects, which are disposed of or are intended to be disposed of or are required to be disposed of by the provisions of national law" [5]. Waste includes any scrap material effluent or unwanted surplus substances or article that that requires disposal because it is broken, worn out, contaminated or otherwise spoiled [6]. Wastes are "those substances or objects which fall out of the commercial cycle or chain of utility "[7]. Figure 2 shows a waste classification framework [8].

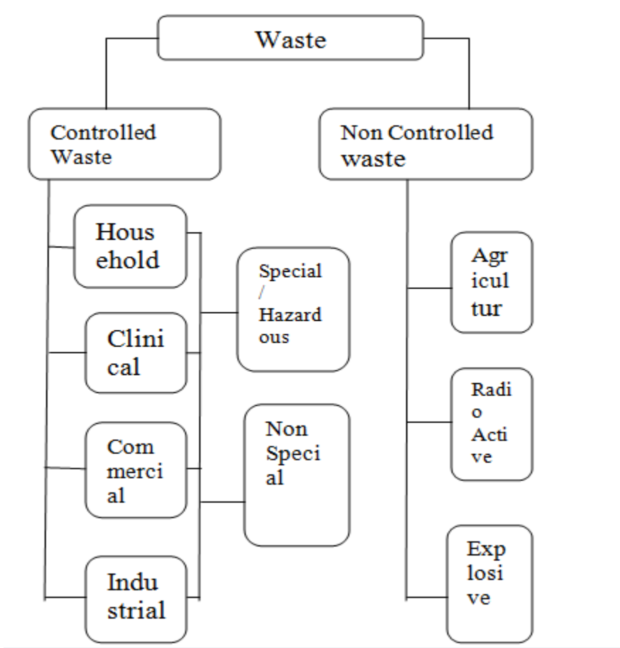

Figure 2 : Waste Classification Framework [8]

IV. Definition of Municipal Waste

Municipal Solid wastes (MSW) is more commonly known as thrash or garbage which consists of everyday items we use & then throw away. Such kind of things are food scraps, bottles, newspaper, paint, batteries, furniture, product packaging and so on. It also includes biodegradable waste, recyclable material, inert waste, electrical & electronic waste, composite waste, hazardous waste, toxic waste, medical waste etc. In developed municipalities without significant recycling activity it predominantly includes food wastes, market wastes, yard wastes, plastic containers and product packaging materials, and other miscellaneous solid wastes from residential, commercial, institutional, and industrial sources [9].

V. Municipal Solid Waste Collection Data in Different Municipalities

a) Chittagong City Corporation (CCC)

Table 2 : Average Waste Generation in Chittagong City Corporation [10]

Description	LGR	MGR	HGR
Per capita domestic waste generation rate	0.25703	0.25703	0.25703
Population in CCC	2978711	3293373	3411339
Total domestic waste (ton)	765.629	846.507	876.828
Market waste (ton)	146.050	146.050	146.050
Street sweeping waste	138.234	138.234	138.234
Total waste (ton)	**1049.913**	**1130.791**	**1161.113**

Table 3 : Density of Waste in Chitagong City Corporation [10]

BROAD CATEGORY	Specific Category	Average density of waste (kg/m3)
Household	High income area	305.88
	Middle income area	313.73
	Low income area	326.47
Markets	Free-port Vegetable Market	617.28
	Riazuddin Bazar	617.28
Trucks	Truck 1.5 Ton	638.96
	Truck 3 Ton	798.00
	Truck 5 Ton	854.29
	Container Truck	1037.58
	Tractor Wagon	676.47

Table 4 : Physical Composition of Solid Waste in Chittagong City Corporation [10]

Component	Landfill Site (%)	Market (%)	Household (%)
Vegetable, Food	81.74	84.09	70.50
Bones, Fishbone	0.00	0.12	0.63
Paper	5.43	0.70	4.68
Plastic	10.60	2.34	8.70
Textile, Rags, Jute	0.04	5.62	2.40
Glass	0.00	0.67	0.00
Leather, Rubber	0.01	0.45	5.80
Metals	0.00	0.48	2.65
Ceramic	0.00	0.32	3.45
Soil, Ash	0.87	0.00	0.00
Grass, Creepers, Herbs, Wood	0.28	0.69	1.20
Medicine, Chemical	0.05	0.00	0.00
Miscellaneous	0.07	4.53	0.00
Feather/coconut shell	0.89	0.00	0.00
Total	**100.00**	**100.00**	**100.00**
Compostable	82.02	84.78	71.70
Non-compostable	17.11	15.22	28.30
Ash	0.87	0.0	0.0

b) Rajshahi City Corporation (RCC)

Table 5 : Average Waste Generation in Rajshahi City Corporation [10]

Description	LGR	MGR	HGR
Domestic Waste Generation Rate (kg/capita/day)	0.203	0.203	0.203
Population in RCC	551124	795451	882246
Total Domestic Waste (ton)	112.120	161.825	179.483
Market Waste	32.738	32.738	32.738
Total Waste (ton)	**187.9**	**194.6**	**255.3**

Table 6 : Density of Waste In Rajshahi City Corporation [10]

Broad Category	Specific Category	Average Density of Waste (kg/m3)
Household	High income area	315.49
	Middle income area	320.27
	Low income area	325.67
Markets	Shaheb Bazar	280.95
	Laxmipur Market	279.76
Trucks	Truck 3 Ton	658.48

Table 7 : Physical Composition of Solid Waste in Rajshahi City Corporation [10]

Component	Household (%)	Market (%)	Landfill Site (%)
Vegetable, Food	82.05	83.65	79.4
Bones, Fishbone	0.27	0.13	0.37
Paper	4.40	1.23	2.3
Plastic	6.63	1.98	3.53
Textile, Rags, Jute	1.50	2.55	2.2
Glass	0.51	0.40	0
Leather, Rubber	0.22	0.20	0.85
Metals	0.00	0.13	0
Ceramic	0.33	0.38	0.39
Soil, Ash	3.60	8.21	10.51
Grass, Creepers, Herbs, Wood	0.42	1.12	0.45
Medicine, Chemical	0.07	0.00	0
Miscellaneous	0.00	0.00	0
Feather/coconut shell	0.00	0.00	0
Total	**100.00**	**100.00**	**100.00**
Compostable	82.47	84.77	79.85
Non-compostable	13.93	7.02	9.64
Ash content	3.60	8.21	10.51

VI. The Electricity Generation Process

In this process, a strong waste management system is very much important. Here electricity is generated from bio gas. To do this, the wastes should be sorted out according to their nature. In table 4 it is shown that the 82.02 % municipal waste is compostable waste in Chittagong City Corporation & in table 7 82.47 % waste is compostable in Rajshahi city corporation. So, it will be very much easier to sort out the collected waste according to their compostable nature (agricultural waste, cooked & raw food waste, fruits & vegetables wastes, fish & meat wastes, excreta of all domestic animals, waste water containing bio waste material) and non-compostable nature (plastic , glass and so on). We can only produce biogas from the compostable waste. Here we sort out the different types of waste first and then we collect the compostable or bio degradable waste for our purpose. Then this bio degradable waste is collected and then biogas is produced by an anaerobic process. This biogas is used in a gas generator to generate electricity. The whole process is shown in the following figure. This electricity generation process can be made more efficient and commercially more valuable by taking some more steps. If we place a gas filter between the biogas generation step and the gas generation step, then the efficiency of the electricity generation will increase. Again, we may produce organic fertilizer from the digester step which will be an

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economic backup for this type of electricity generation process. A flow chart is shown above for better understanding.

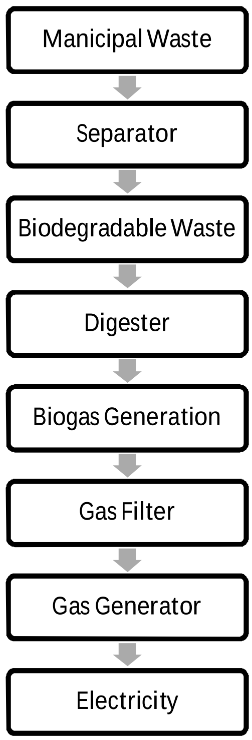

Figure 3 : Electricity Generation from Municipal Waste

VII. Advantages of the Proposed System

- It will be helpful for the municipalities to generate their own electricity (at least to generate electricity for municipal purposes like street light, water pump etc.)
- It could be helpful to meet up the increasing electricity demand of the city dwellers.
- It could be helpful to minimize the waste management cost.
- It is a way to generate green energy.
- It will decrease the dependency on conventional electricity generation sources.

VIII. Conclussion

Electricity is a crying need for the development of Bangladesh. Again it is one of the most important aspects the government has to consider for the improvement of the lifestyle of its citizens. A huge amount of people in Bangladesh are shifting from rural to urban areas in search of better living. As a result the cities are becoming more power hungry compared to the rural areas. To supply electricity to this huge no. of city dwellers and to release the extra pressure electricity generation, “Electricity from municipal solid waste “can be a better solution in Bangladeshi scenario. Because with the increase of populations in the urban areas it increases the municipal wastage amount. Which makes this electricity producing model not only very efficient but also it helps the urban areas becoming cleaner and environmentally sound. Hope that this process will be helpful for Bangladesh Govt. to supply the demanded electricity.

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Design of Low Power 4-Bit CMOS Braun Multiplier based on Threshold Voltage Techniques

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Abstract- A circuit design for a new Low Power 4-bit Braun Multiplier is presented. The multiplier is implemented by using different Threshold Voltage techniques. Power reduction techniques are proposed for 4-bit Braun Multiplier which is designed by Full Adders. To get Optimum design low threshold voltages are used at critical paths similar way high threshold voltages are used at non critical paths. The design uses CMOS digital circuits in order to reduce the power dissipation while maintaining computational throughput. This architecture is simulated at 90nm Technology with 1.2v power supply. The power dissipation of nearly 46%, Power Delay Product of 56% and delay 19.3% has been reduced by using proposed techniques with good performance.

Keywords: braun multiplier, full adder, high & low threshold voltage.

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Dayadi Lakshmaiah [α], Dr. M. V. Subramanyam [σ] & Dr. K. Satya Prasad [ρ]

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I. Introduction

In order to achieve the high speed and low power demand in DSP applications Braun's multiplier are broadly used. The Braun's multiplier is generally called as the Carry Save Array Multiplier. The architecture of a Braun's multiplier consists of AND gates and full adders. The prolific growth in semiconductor device industry has been Indicates to the high performance portable systems with enhanced reliability in data transmission. In order to maintain the high performance fidelity applications, emphasis will be on incorporation of low power modules in future system design [1-5]. The design of such modules power consumption or dissipation in fundamental arithmetic computation units such as adders and multipliers. This implies a need to design low power multipliers towards the development of efficient power & high-performance systems. The selection of the most efficient implemented multiplication has continually challenge DSP system designers [6-7]. Every system designer offers a wide range of tradeoffs in terms of speed, complexity and power consumption. Input sequences to the multiplier can be fed in parallel, serial or a hybrid (parallel serial) this proposal approaches gives high processing speed. Usually Parallel multipliers are adopted at the expense of high area complexity. Multiple parallel multiplications Algorithms (architectures) [8] have been proposed to reduce the chip area increase the speed of the multipliers' and reduce the power dissipation using various techniques. Several of these techniques reduce the power dissipation by eliminating spurious transitions in the circuit [9,11].

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II. Proposed Work

A full adder has been designed with 10 MOS Transistors for the implementation of logic expression of Eq. (1) & Eq. (2). The 1-bit full adder circuit consists of three modules, XNOR-I, XNOR-II, and MUX. The XNOR-I and XNOR-II modules are designed using 4 MOS transistors considering two inputs and one output, and MUX module is designed with two MOS transistors for optimum operation. The implementations of full adders are shown in Fig .1 to Fig.4 the XNOR and XOR logic is combined with 6 MOS transistors and MUX logic with 2 MOS transistors for optimum operation. The implementation of full adder with 10 MOS transistors is shown in Fig.5 Full Adders propose were is presented in the reference paper [10]

$$Sum = \left(A \bar{\oplus} B\right) C_{in} + \left(A \oplus B\right) \bar{C}_{in} \qquad (1)$$

$$C_{out} = \left(A \oplus B\right) C_{in} + \left(A \bar{\oplus} B\right) A \qquad (2)$$

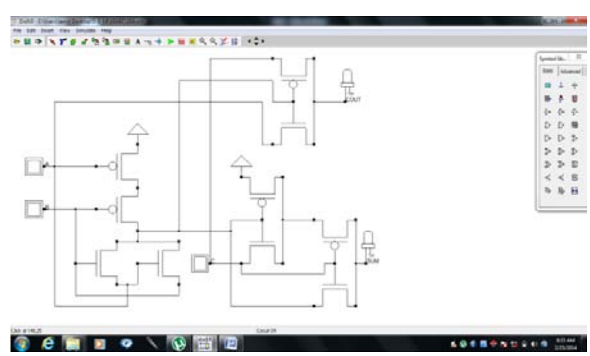

Fig. 1 : Full adder proposed work 1

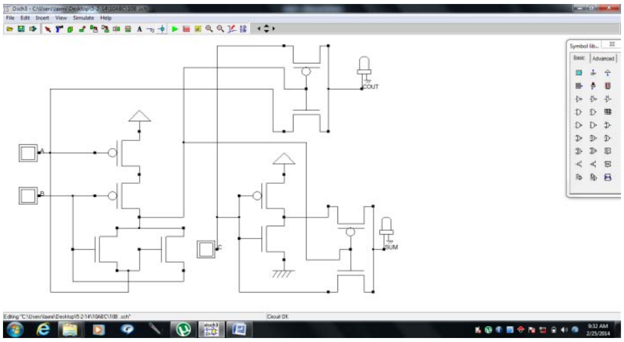

Fig. 2 : Full adder proposed work 2

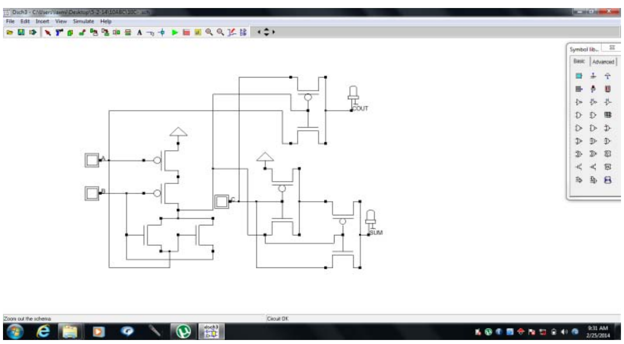

Fig. 3 : Full adder proposed work 3

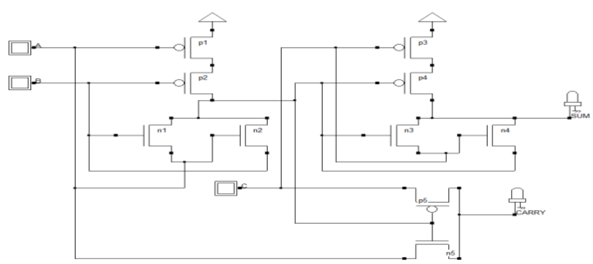

Fig. 4 : Full adder proposed work 4

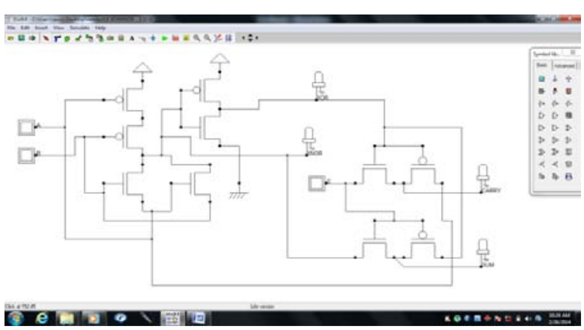

Fig. 5 : Full adder proposed work 5

a) Braun Multiplier

Consider the multiplication two un-signed 4- bit numbers

A= a3, a2, a1, a0

Multiplier is given by

B=b3, b2, b1, b0

Then product will be

P=p7, p6, p5, p4, p3p2, p1, p0

A				a3	a2	a1	a0
	B x			b3	b2	b1	b0
			.	a3b0	a2bo	a1b0	a0b0
		.	a3b1	a2b1	a1b1	a0b1	
	.	a3b2	a2b2	a1b2	a0b2		
.a3b3	a2b3	a1b3	a0b3				
P7	p6	p5	p4	p3	p2	p1	p0

This simplest parallel multiplier is the Braun array. All the partial products are computed in Parallel, then collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. Note that this multiplier is only suited for positive operands. The structure of the Braun algorithm for the unsigned binary multiplication is shown in Fig.6

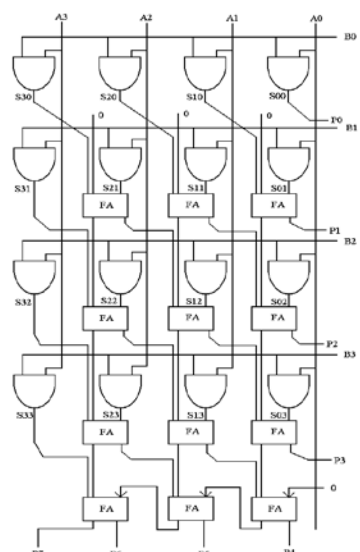

Fig. 6 : 4-Bit CMOS Braun multiplier Block Diagram

III. Performance and Simulation Results

Technology 90nm, Normal Threshold voltage =0.5v, High Threshold voltage=0.8v, Low threshold voltage=0.3v, VDD=1.2v.

Proposed work is implemented with the 210 MOS transistors parameters like power, area, Power Delay Product are compared with the reference paper

[11].proposed results are matched with the reference paper. The architecture is optimized to less MOS Transistors compared to reference paper [11]. Where same architecture is implemented with 222 MOS Transistors The architecture consists the 15 AND gates and 12 Full Adders which is shown in the above Fig.6. The product Boolean equation is shown in below .Where A_0 to A_3 and B_0 to B_3 are inputs and p_1 to p_7 are product of outputs.

$S_0=(A_1B_0).(A_0B_1)$, $S_1=(A_1B_1)\ \text{XOR}\ (A_2B_0)$, $S_2=(A_2B_0).(A_1B_1)$, $S3=(A_2B_1)\ \text{XOR}\ (A_3B_0)$, $S_4=(B_0A_3).(A_2B_1)$

$S_5=(A_0B_2).S_0+(A_0B_2).S_1+(S_0)(S_1)$, $S_6=(S_2)\ \text{XOR}\ (S_3)\ \text{XOR}\ (A_1B_2)$, $S_7=S_3.S_2+(A_1B_2).S_3+(A_1B_2).S_2$

$S_8=(A_2B_2)\ \text{XOR}(B_1A_3)\ \text{XOR}(S_4)$, $S_9=S_4.(A_2B_2)+S_4.(A_3B_1)+(A_2B_2)(A_3B_1)$, $S_{10}=S_5.S_6+S_5.(A_0B_3)+(A_0B_3).S_6$

$S_{11}=(A_1B_3)\ \text{XOR}\ S_7\ \text{XOR}\ S_{8,}$ $S_{12}=(A_1B_3).S_7+S_7.S_8+S_8.(A_1B_3)$, $S_{13}=(A_1B_3)$

$S_{14}=(A_2B_3).S_9+(S_9)(B_2A_3)+(A_2B_3)(B_2A_3)$, $S_{15}=S_{11}.S_{10,}$ $S_{16}=S_{13}.S_{12}+S_{13}.S_{15}+S_{12}.S_{15}$

$P_0=A_0B_{0.}$ -- (1)

$P1=(A_0B_1)\ \text{XOR}\ (A_1B_0)$ -------------------------- (2)

$P2=(A_0B_{2)}\ \text{XOR}\ (S_0)\ \text{XOR}\ (S_1)$ ------------------ (3)

$P_3=(A_0B_3)\ \text{XOR}\ (S5)\ \text{XOR}\ (S_{6)}$ ------------------ (4)

$P_4=S_{10}\ \text{XOR}\ S_1$ ------------------------------------ (5)

$P_5=S_{15}\ \text{XOR}\ S_{12}\ \text{XOR}\ S_{13}$ -------------------------- (6)

$P_6=S_{16}\ \text{XOR}\ S_{14}\ \text{XOR}\ (A_3B_3)$ ------------------- (7)

$P_7=(A_3B_3).S_{14}+S_{14}.S_{16}+S_{16}.(A_3B_3)$ ------------ (8)

Braun Multiplier Normal V_T (Normal threshold voltage) Table.1

Proposed 4-bit Multipliers	Power(μw)	Delay(ns)	Power Delay Product femito(10^{-15})	Area (μm^2)
2011 IEEE Reference paper	45.686	5.270	237	5610
4-bit Multiplier proposed work1	54.302	4.695	254	5712
4-bit Multiplier proposed work2	30.089	4.615	138	5456
4-bit Multiplier proposed work3	28.404	4.695	133	5910
4-bit Multiplier proposed work4	25.063	4.785	119	5661
4-bit Multiplier proposed work5	27.444	4.990	136	5700

Braun Multiplier Low V_T (Low threshold voltage) Table.2

Proposed 4x4 Multipliers	Power(μw)	delay(ns)	Power Delay Product femito(10^{-15})	Area (μm^2)
2011 IEEE paper	45.686	5.270	237	5610
4-bit Multiplier proposed work1	30.702	4.691	144	5354
4-bit Multiplier proposed work2	25.992	4.277	111	5654
4-bit Multiplier proposed work3	26.194	4.690	122	5504
4-bit Multiplier proposed work4	28.475	4.785	136	5500
4-bit Multiplier proposed work5	29.586	5.055	149	57.26

Braun Multiplier High V_T (High Threshold voltage) Table.3

Proposed 4-bit Multipliers	Power(μw)	delay(ns)	Power Delay Product femito(10^{-15})	Area (μm^2)
2011 IEEE paper	45.686	5.270	237	5610
4-bit Multiplier proposed work1	26.553	4.695	124	5530

4-bit Multiplier proposed work2	60.055	4.270	256	5534
4-bit Multiplier proposed work3	25.594	4.695	120	5516
4-bit Multiplier proposed work4	74.600	6.860	511	5660
4-bit Multiplier proposed work5	24.524	6.025	147	5752

Braun Multiplier Low V_T (Low Threshold voltage) & High V_T (High Threshold voltage) Table.4

Proposed 4-bit Multipliers	Power(μw)	delay(ns)	Power Delay Product femito (10^{-15})	Area (μm^2)
2011 IEEE paper	45.686	5.270	237	5610
4-bit Multiplier proposed work1	24.448	4.270	104	5524
4-bit Multiplier proposed work2	26.743	4.695	125	5918
4-bit Multiplier proposed work3	64.600	6.435	415	5706
4-bit Multiplier proposed work4	28.321	5.340	151	5959
4-bit Multiplier proposed work5	29.235	4.695	137	5736

The architecture is simulated with the cadence micro wind software. As shown in the above Table.1. The proposed work of the MOS transistors with normal threshold voltage was used at critical path. It is observed that 4-bit Braun multiplier using proposed Work4 Power Delay Product 119 femito (10^{-15}), with Reference paper [11], it is observed that 46% of power Delay Product has been reduced.

As shown in the above Table.2. The proposed work of the MOS transistors with low threshold voltage was used at critical path. It is observed that 4-bit Braun multiplier using proposed Work2 we got Power Delay Product 111 femito (10^{-15}), but comparatively to the Reference paper [11], it is 51% of power Delay Product has been reduced.

As shown in the above Table.3. The proposed work of the MOS transistors with high threshold voltage was used at critical path. It is observed that 4-bit Braun multiplier using proposed Work1 Power Delay Product 120 femito (10^{-15}), with Reference paper [11], it is observed that 47% of power Delay Product has been reduced.

As shown in the above Table.4. The proposed work of the MOS transistors with low threshold voltage was used at critical path and high threshold voltage at non critical path. It is observed that 4-bit Braun multiplier using proposed Work1 Power Delay Product 104 femito (10^{-15}), with Reference paper [11], it is observed that 56% of power Delay Product has been reduced. Simulation results are using Micro wind Tool.

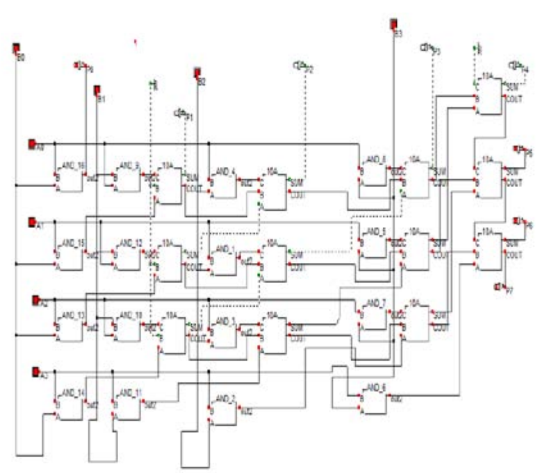

Figure 7 : Braun 4-Bit Multiplier using Micro wind Tool

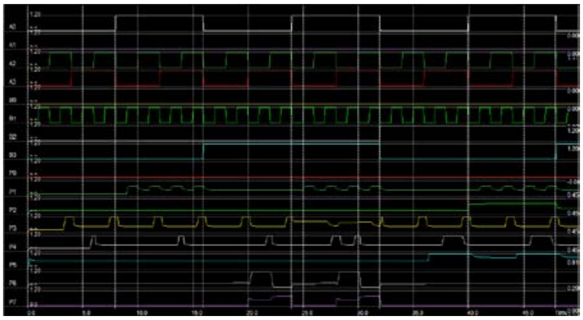

Figure 8 : 4-Bit CMOS Braun Multiplier Reference paper simulation result

IV. Conclusion

The present paper demonstrated the improvement in parameters v/s, Area, power, and delay with reduction in number of transistors to implement Full adder circuits. The simulations were performed using 90nm Micro wind 3 CMOS layout CAD Tool In this paper power consumption & Power Delay Product is calculated the results are optimized power consumption of 46% and Power Delay Product is 56 % still the performance of 4-Bit CMOS Braun Multiplier is improved by incorporating techniques which support reduced transistor implementations.

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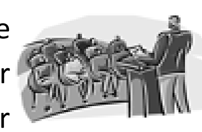

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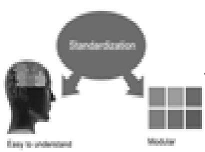

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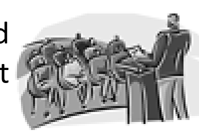

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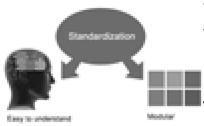

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"

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4. Manuscript's Category,

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18. Pick a good study spot: To do your research studies always try to pick a spot, which is quiet. Every spot is not for studies. Spot that suits you choose it and proceed further.

19. Know what you know: Always try to know, what you know by making objectives. Else, you will be confused and cannot achieve your target.

20. Use good quality grammar: Always use a good quality grammar and use words that will throw positive impact on evaluator. Use of good quality grammar does not mean to use tough words, that for each word the evaluator has to go through dictionary. Do not start sentence with a conjunction. Do not fragment sentences. Eliminate one-word sentences. Ignore passive voice. Do not ever use a big word when a diminutive one would suffice. Verbs have to be in agreement with their subjects. Prepositions are not expressions to finish sentences with. It is incorrect to ever divide an infinitive. Avoid clichés like the disease. Also, always shun irritating alliteration. Use language that is simple and straight forward. put together a neat summary.

21. Arrangement of information: Each section of the main body should start with an opening sentence and there should be a changeover at the end of the section. Give only valid and powerful arguments to your topic. You may also maintain your arguments with records.

22. Never start in last minute: Always start at right time and give enough time to research work. Leaving everything to the last minute will degrade your paper and spoil your work.

23. Multitasking in research is not good: Doing several things at the same time proves bad habit in case of research activity. Research is an area, where everything has a particular time slot. Divide your research work in parts and do particular part in particular time slot.

24. Never copy others' work: Never copy others' work and give it your name because if evaluator has seen it anywhere you will be in trouble.

25. Take proper rest and food: No matter how many hours you spend for your research activity, if you are not taking care of your health then all your efforts will be in vain. For a quality research, study is must, and this can be done by taking proper rest and food.

26. Go for seminars: Attend seminars if the topic is relevant to your research area. Utilize all your resources.

27. Refresh your mind after intervals: Try to give rest to your mind by listening to soft music or by sleeping in intervals. This will also improve your memory.

28. Make colleagues: Always try to make colleagues. No matter how sharper or intelligent you are, if you make colleagues you can have several ideas, which will be helpful for your research.

29. Think technically: Always think technically. If anything happens, then search its reasons, its benefits, and demerits.

30. Think and then print: When you will go to print your paper, notice that tables are not be split, headings are not detached from their descriptions, and page sequence is maintained.

31. Adding unnecessary information: Do not add unnecessary information, like, I have used MS Excel to draw graph. Do not add irrelevant and inappropriate material. These all will create superfluous. Foreign terminology and phrases are not apropos. One should NEVER take a broad view. Analogy in script is like feathers on a snake. Not at all use a large word when a very small one would be sufficient. Use words properly, regardless of how others use them. Remove quotations. Puns are for kids, not grunt readers. Amplification is a billion times of inferior quality than sarcasm.

32. Never oversimplify everything: To add material in your research paper, never go for oversimplification. This will definitely irritate the evaluator. Be more or less specific. Also too, by no means, ever use rhythmic redundancies. Contractions aren't essential and shouldn't be there used. Comparisons are as terrible as clichés. Give up ampersands and abbreviations, and so on. Remove commas, that are, not necessary. Parenthetical words however should be together with this in commas. Understatement is all the time the complete best way to put onward earth-shaking thoughts. Give a detailed literary review.

33. Report concluded results: Use concluded results. From raw data, filter the results and then conclude your studies based on measurements and observations taken. Significant figures and appropriate number of decimal places should be used. Parenthetical remarks are prohibitive. Proofread carefully at final stage. In the end give outline to your arguments. Spot out perspectives of further study of this subject. Justify your conclusion by at the bottom of them with sufficient justifications and examples.

34. After conclusion: Once you have concluded your research, the next most important step is to present your findings. Presentation is extremely important as it is the definite medium though which your research is going to be in print to the rest of the crowd. Care should be taken to categorize your thoughts well and present them in a logical and neat manner. A good quality research paper format is essential because it serves to highlight your research paper and bring to light all necessary aspects in your research.

Informal Guidelines of Research Paper Writing

Key points to remember:

- Submit all work in its final form.
- Write your paper in the form, which is presented in the guidelines using the template.
- Please note the criterion for grading the final paper by peer-reviewers.

Final Points:

A purpose of organizing a research paper is to let people to interpret your effort selectively. The journal requires the following sections, submitted in the order listed, each section to start on a new page.

The introduction will be compiled from reference matter and will reflect the design processes or outline of basis that direct you to make study. As you will carry out the process of study, the method and process section will be constructed as like that. The result segment will show related statistics in nearly sequential order and will direct the reviewers next to the similar intellectual paths throughout the data that you took to carry out your study. The discussion section will provide understanding of the data and projections as to the implication of the results. The use of good quality references all through the paper will give the effort trustworthiness by representing an alertness of prior workings.

Writing a research paper is not an easy job no matter how trouble-free the actual research or concept. Practice, excellent preparation, and controlled record keeping are the only means to make straightforward the progression.

General style:

Specific editorial column necessities for compliance of a manuscript will always take over from directions in these general guidelines.

To make a paper clear

· Adhere to recommended page limits

Mistakes to evade

- Insertion a title at the foot of a page with the subsequent text on the next page
- Separating a table/chart or figure - impound each figure/table to a single page
- Submitting a manuscript with pages out of sequence

In every sections of your document

· Use standard writing style including articles ("a", "the," etc.)

· Keep on paying attention on the research topic of the paper

· Use paragraphs to split each significant point (excluding for the abstract)

· Align the primary line of each section

· Present your points in sound order

· Use present tense to report well accepted

· Use past tense to describe specific results

· Shun familiar wording, don't address the reviewer directly, and don't use slang, slang language, or superlatives

· Shun use of extra pictures - include only those figures essential to presenting results

Title Page:

Choose a revealing title. It should be short. It should not have non-standard acronyms or abbreviations. It should not exceed two printed lines. It should include the name(s) and address (es) of all authors.

Abstract:

The summary should be two hundred words or less. It should briefly and clearly explain the key findings reported in the manuscript--must have precise statistics. It should not have abnormal acronyms or abbreviations. It should be logical in itself. Shun citing references at this point.

An abstract is a brief distinct paragraph summary of finished work or work in development. In a minute or less a reviewer can be taught the foundation behind the study, common approach to the problem, relevant results, and significant conclusions or new questions.

Write your summary when your paper is completed because how can you write the summary of anything which is not yet written? Wealth of terminology is very essential in abstract. Yet, use comprehensive sentences and do not let go readability for briefness. You can maintain it succinct by phrasing sentences so that they provide more than lone rationale. The author can at this moment go straight to shortening the outcome. Sum up the study, with the subsequent elements in any summary. Try to maintain the initial two items to no more than one ruling each.

- Reason of the study - theory, overall issue, purpose
- Fundamental goal
- To the point depiction of the research
- Consequences, including definite statistics - if the consequences are quantitative in nature, account quantitative data; results of any numerical analysis should be reported
- Significant conclusions or questions that track from the research(es)

Approach:

- Single section, and succinct
- As a outline of job done, it is always written in past tense
- A conceptual should situate on its own, and not submit to any other part of the paper such as a form or table
- Center on shortening results - bound background information to a verdict or two, if completely necessary
- What you account in an conceptual must be regular with what you reported in the manuscript
- Exact spelling, clearness of sentences and phrases, and appropriate reporting of quantities (proper units, important statistics) are just as significant in an abstract as they are anywhere else

Introduction:

The **Introduction** should "introduce" the manuscript. The reviewer should be presented with sufficient background information to be capable to comprehend and calculate the purpose of your study without having to submit to other works. The basis for the study should be offered. Give most important references but shun difficult to make a comprehensive appraisal of the topic. In the introduction, describe the problem visibly. If the problem is not acknowledged in a logical, reasonable way, the reviewer will have no attention in your result. Speak in common terms about techniques used to explain the problem, if needed, but do not present any particulars about the protocols here. Following approach can create a valuable beginning:

- Explain the value (significance) of the study
- Shield the model - why did you employ this particular system or method? What is its compensation? You strength remark on its appropriateness from a abstract point of vision as well as point out sensible reasons for using it.
- Present a justification. Status your particular theory (es) or aim(s), and describe the logic that led you to choose them.
- Very for a short time explain the tentative propose and how it skilled the declared objectives.

Approach:

- Use past tense except for when referring to recognized facts. After all, the manuscript will be submitted after the entire job is done.
- Sort out your thoughts; manufacture one key point with every section. If you make the four points listed above, you will need a least of four paragraphs.

- Present surroundings information only as desirable in order hold up a situation. The reviewer does not desire to read the whole thing you know about a topic.
- Shape the theory/purpose specifically - do not take a broad view.
- As always, give awareness to spelling, simplicity and correctness of sentences and phrases.

Procedures (Methods and Materials):

This part is supposed to be the easiest to carve if you have good skills. A sound written Procedures segment allows a capable scientist to replacement your results. Present precise information about your supplies. The suppliers and clarity of reagents can be helpful bits of information. Present methods in sequential order but linked methodologies can be grouped as a segment. Be concise when relating the protocols. Attempt for the least amount of information that would permit another capable scientist to spare your outcome but be cautious that vital information is integrated. The use of subheadings is suggested and ought to be synchronized with the results section. When a technique is used that has been well described in another object, mention the specific item describing a way but draw the basic principle while stating the situation. The purpose is to text all particular resources and broad procedures, so that another person may use some or all of the methods in one more study or referee the scientific value of your work. It is not to be a step by step report of the whole thing you did, nor is a methods section a set of orders.

Materials:

- Explain materials individually only if the study is so complex that it saves liberty this way.
- Embrace particular materials, and any tools or provisions that are not frequently found in laboratories.
- Do not take in frequently found.
- If use of a definite type of tools.
- Materials may be reported in a part section or else they may be recognized along with your measures.

Methods:

- Report the method (not particulars of each process that engaged the same methodology)
- Describe the method entirely
- To be succinct, present methods under headings dedicated to specific dealings or groups of measures
- Simplify - details how procedures were completed not how they were exclusively performed on a particular day.
- If well known procedures were used, account the procedure by name, possibly with reference, and that's all.

Approach:

- It is embarrassed or not possible to use vigorous voice when documenting methods with no using first person, which would focus the reviewer's interest on the researcher rather than the job. As a result when script up the methods most authors use third person passive voice.
- Use standard style in this and in every other part of the paper - avoid familiar lists, and use full sentences.

What to keep away from

- Resources and methods are not a set of information.
- Skip all descriptive information and surroundings - save it for the argument.
- Leave out information that is immaterial to a third party.

Results:

The principle of a results segment is to present and demonstrate your conclusion. Create this part a entirely objective details of the outcome, and save all understanding for the discussion.

The page length of this segment is set by the sum and types of data to be reported. Carry on to be to the point, by means of statistics and tables, if suitable, to present consequences most efficiently.You must obviously differentiate material that would usually be incorporated in a study editorial from any unprocessed data or additional appendix matter that would not be available. In fact, such matter should not be submitted at all except requested by the instructor.

Content

- Sum up your conclusion in text and demonstrate them, if suitable, with figures and tables.
- In manuscript, explain each of your consequences, point the reader to remarks that are most appropriate.
- Present a background, such as by describing the question that was addressed by creation an exacting study.
- Explain results of control experiments and comprise remarks that are not accessible in a prescribed figure or table, if appropriate.
- Examine your data, then prepare the analyzed (transformed) data in the form of a figure (graph), table, or in manuscript form.

What to stay away from

- Do not discuss or infer your outcome, report surroundings information, or try to explain anything.
- Not at all, take in raw data or intermediate calculations in a research manuscript.
- Do not present the similar data more than once.
- Manuscript should complement any figures or tables, not duplicate the identical information.
- Never confuse figures with tables - there is a difference.

Approach

- As forever, use past tense when you submit to your results, and put the whole thing in a reasonable order.
- Put figures and tables, appropriately numbered, in order at the end of the report
- If you desire, you may place your figures and tables properly within the text of your results part.

Figures and tables

- If you put figures and tables at the end of the details, make certain that they are visibly distinguished from any attach appendix materials, such as raw facts
- Despite of position, each figure must be numbered one after the other and complete with subtitle
- In spite of position, each table must be titled, numbered one after the other and complete with heading
- All figure and table must be adequately complete that it could situate on its own, divide from text

Discussion:

The Discussion is expected the trickiest segment to write and describe. A lot of papers submitted for journal are discarded based on problems with the Discussion. There is no head of state for how long a argument should be. Position your understanding of the outcome visibly to lead the reviewer through your conclusions, and then finish the paper with a summing up of the implication of the study. The purpose here is to offer an understanding of your results and hold up for all of your conclusions, using facts from your research and generally accepted information, if suitable. The implication of result should be visibly described. Infer your data in the conversation in suitable depth. This means that when you clarify an observable fact you must explain mechanisms that may account for the observation. If your results vary from your prospect, make clear why that may have happened. If your results agree, then explain the theory that the proof supported. It is never suitable to just state that the data approved with prospect, and let it drop at that.

- Make a decision if each premise is supported, discarded, or if you cannot make a conclusion with assurance. Do not just dismiss a study or part of a study as "uncertain."
- Research papers are not acknowledged if the work is imperfect. Draw what conclusions you can based upon the results that you have, and take care of the study as a finished work
- You may propose future guidelines, such as how the experiment might be personalized to accomplish a new idea.
- Give details all of your remarks as much as possible, focus on mechanisms.
- Make a decision if the tentative design sufficiently addressed the theory, and whether or not it was correctly restricted.
- Try to present substitute explanations if sensible alternatives be present.
- One research will not counter an overall question, so maintain the large picture in mind, where do you go next? The best studies unlock new avenues of study. What questions remain?
- Recommendations for detailed papers will offer supplementary suggestions.

Approach:

- When you refer to information, differentiate data generated by your own studies from available information
- Submit to work done by specific persons (including you) in past tense.
- Submit to generally acknowledged facts and main beliefs in present tense.

Please carefully note down following rules and regulation before submitting your Research Paper to Global Journals Inc. (US):

Segment Draft and Final Research Paper: You have to strictly follow the template of research paper. If it is not done your paper may get rejected.

- The **major constraint** is that you must independently make all content, tables, graphs, and facts that are offered in the paper. You must write each part of the paper wholly on your own. The Peer-reviewers need to identify your own perceptive of the concepts in your own terms. NEVER extract straight from any foundation, and never rephrase someone else's analysis.

- Do not give permission to anyone else to "PROOFREAD" your manuscript.

- Methods to avoid Plagiarism is applied by us on every paper, if found guilty, you will be blacklisted by all of our collaborated research groups, your institution will be informed for this and strict legal actions will be taken immediately.)
- To guard yourself and others from possible illegal use please do not permit anyone right to use to your paper and files.

Criterion for Grading a Research Paper (Compilation) by Global Journals Inc. (US)

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Topics	Grades		
	A-B	**C-D**	**E-F**
Abstract	Clear and concise with appropriate content, Correct format. 200 words or below	Unclear summary and no specific data, Incorrect form Above 200 words	No specific data with ambiguous information Above 250 words
Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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