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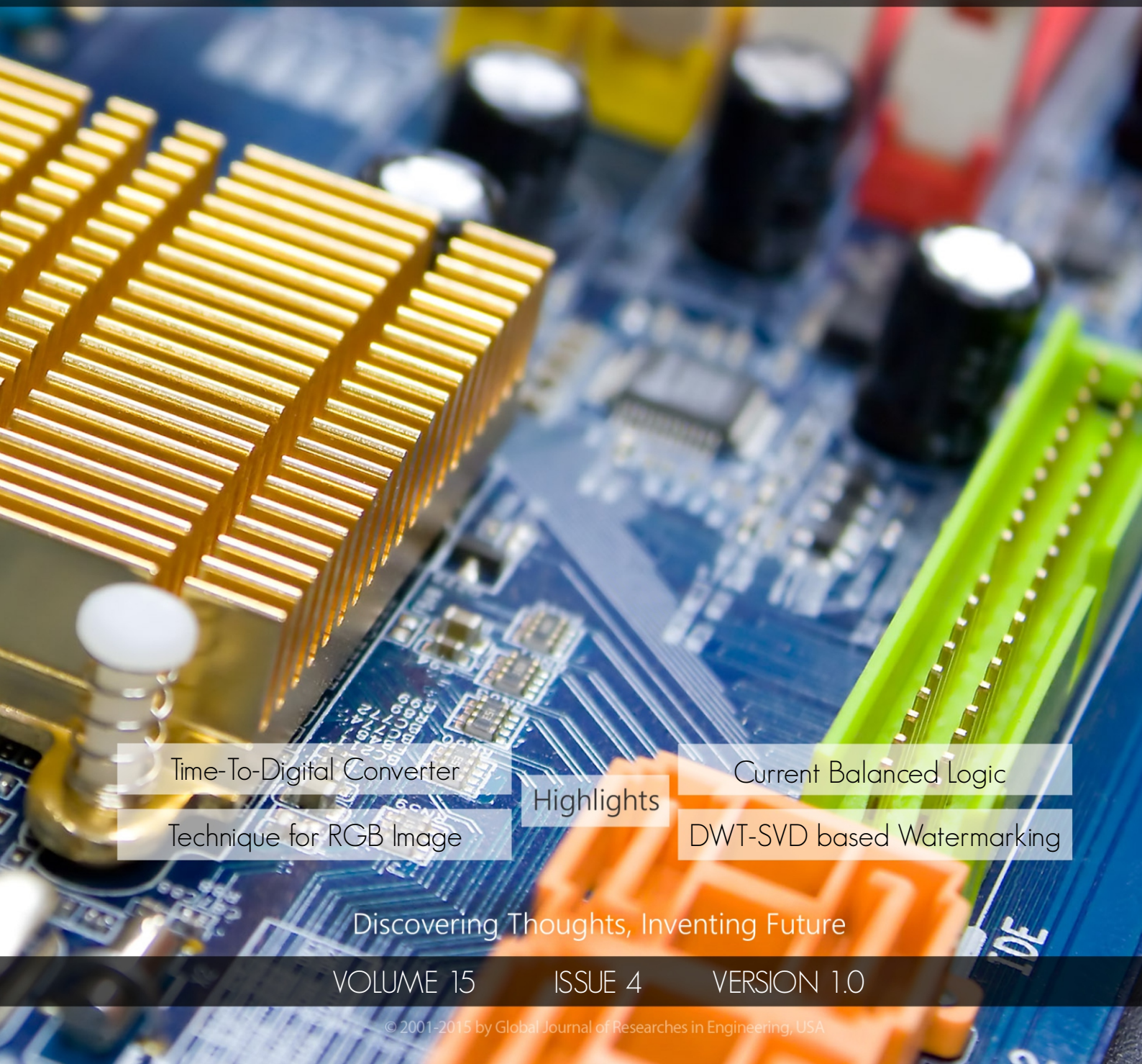

Time-To-Digital Converter

Technique for RGB Image

Highlights

Current Balanced Logic

DWT-SVD based Watermarking

Discovering Thoughts, Inventing Future

VOLUME 15 ISSUE 4 VERSION 1.0

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Non-Blind DWT-SVD based Watermarking Technique for RGB Image

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Abstract- The security of the multimedia file is one of the central concerns in this era of online trade and communication. This paper proposes an algorithm for the robustness of authenticity of digital image against various attacks through embedding and extracting watermarking into image. Using DWT-SVD technique, the RGB colors are separated from both cover and watermark image. For watermarking process, a threshold values from R planes of the watermark image is integrated into R channel of the cover image. The experimental result shows that this method has better robustness against known attacks.

Keywords: watermarking, DWT-SVD, image embedding, image extraction.

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Non-Blind DWT-SVD based Watermarking Technique for RGB Image

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Abstract- **The security of the multimedia file is one of the central concerns in this era of online trade and communication. This paper proposes an algorithm for the robustness of authenticity of digital image against various attacks through embedding and extracting watermarking into image. Using DWT-SVD technique, the RGB colors are separated from both cover and watermark image. For watermarking process, a threshold values from R planes of the watermark image is integrated into R channel of the cover image. The experimental result shows that this method has better robustness against known attacks.**

Keywords: watermarking, DWT-SVD, image embedding, image extraction.

I. Introduction

Digital watermarking technology has taken an important position in the industries where copyright, identification, protection and authenticity of a digital content are crucial and priority. Subsequently it has drawn attention to the researchers for developing and improving various techniques of using watermarking in different applications. In a traditional watermarking the watermark is intended to be visible due to identifying the manufacturing company. In contrast to traditional one, the digital watermarking is intended to be imperceptible in the noise tolerant signal of image, audio and video file in such way that the host data does not distort. The multimedia data on the internet has been integrated in the global economy in such a way that it become subject to attack with various readily available tools found in the internet. As a result the watermark in the data requires resistance against various attacks. Watermarking need to be within an acceptable limit and robust when different types of processing is applied in digital content namely adding noise, cropping, compression, resizing [1]. Some attacks are considered as the state-of-the art watermarking attacks which are geometric attacks, cryptographic attacks, removal attacks, protocol attacks and removal attacks [2]. There are mainly two general methods for watermarking which are commonly known as spatial domain technique and frequency domain technique. In the spatial domain approach the information is embedded by altering the pixel value of the cover image. On the other hand the frequency domain method uses the technique of domain transformation. The later one is more robust than the former one. In this method several transformation techniques is available such as Discrete Cosine Transformation (DCT), Discrete Fourier Transformation (DFT) and Discrete Wavelet Transformation (DWT). The obtained frequency component is then modified to hide the watermark. The RGB, YIQ and YUV color space are used for embedding watermark in an host image. The Discrete Wavelet Transformation (DWT) function is combined with the Singular Value Decomposition (SVD) for embedding the watermark in the YUV color space. The RGB color space can be converted into YUV color space and the watermark is embedded into its channels [3]. In the proposed method, the R planes of the watermark is converted using thresholds. Then combined with SVD and DWT to embed data in frequency domain of cover image. The review of related works is given in section II. In section III proposed algorithm is given. The result and analysis of the proposed result is given in section IV.

II. Review of Related Works

Some researchers have used DCT, DWT and SVD technique on the R, G and B components of a host and watermark image. The watermarking technique used with SVD overcomes the weakness that was found in other methods [4]. The technique of converting the RGB color components first into the YIQ color component and then embedding the watermark image into Y and Q color space is shown by Sun and Yu[5]. Gunjal and Mali proposed embedding watermark in all YIQ, RGB and YUV color channels [6].

III. Proposed Method

a) Algorithm for Embedding process

Step 1: The R, G and B planes of host image and watermark image are separated first. Then the R plane is used for embedding.

Step 2: A threshold technique is applied to R planes of watermark image and then 2D-DWT technique to R planes of cover image to decompose into four band of frequency namely LL, LH, HL and HH. The LL3 (Approximation Coefficient) of fourth level

decomposition increases the PNSR by reducing the effect of noise on the cover image.

Step 3: SVD technique is applied on LL3 band of original image and R planes of watermark image. The equation for embedding is:

$$S_{wmi} = S_{ori} + S_{wm} \quad (1)$$

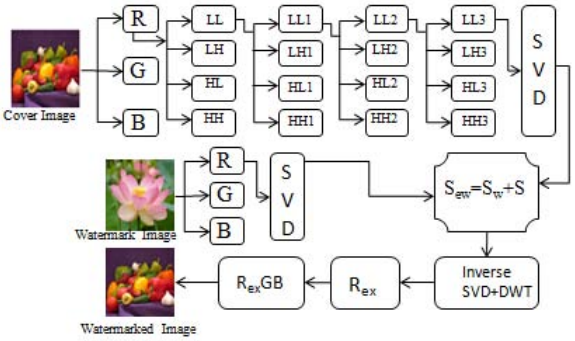

Fig. 1 : Embedding Process

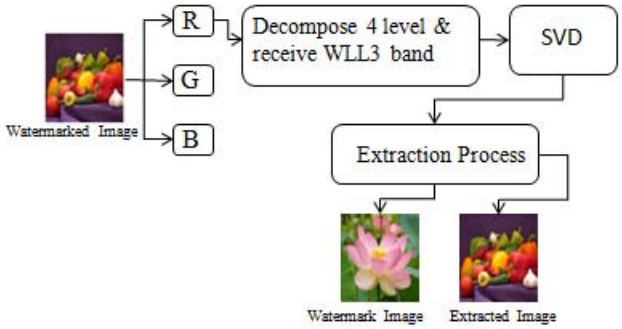

Fig. 2 : Extraction Process

Step 4: Apply inverse SVD and inverse DWT to obtain the customized band R. Then construct watermarked image. The embedding procedure is shown through the figure 1.

b) Extraction Process

The watermark and the cover picture are extracted applying the reverse process on the watermarked image. The extraction procedure is described below:

Step 1: Separate R_{wmi}, G_{wmi} and B_{wmi} planes from the watermarked image.

Step 2: Decompose R_{wmi} planes four times to receive W_{LL3} band.

Step 3: Apply SVD on W_{LL3} band and perform the equation $S_{EWM} = S_{WMI} - S_{ORI}$ to receive watermark. The SEWM is the extracted watermark. SWMI has come from watermarked image and SORI from cover image.

Step 4: Apply inversed SVD, inversed DWT and threshold technique to re-construct the watermark image. The extraction formula is exposed through the figure 2.

Step 5: Normalized Correlation is calculated between watermark and extracted watermark image using the following equation:

$$NC = \frac{\sum_{i=1}^{p}\sum_{j=1}^{q}\left(W^{r}_{i,j}EW^{r}_{i,j} + W^{g}_{i,j}EW^{g}_{i,j} + W^{b}_{i,j}EW^{b}_{i,j}\right)}{\sum_{i=1}^{p}\sum_{j=1}^{q}\left(\left(W^{r}_{i,j}+W^{g}_{i,j}+W^{b}_{i,j}\right)\left(EW^{r}_{i,j}+EW^{g}_{i,j}+EW^{b}_{i,j}\right)\right)} \quad (2)$$

Where W is Watermark image and EW is extracted watermark image.

Fig-3

Fig. 3

Step 6: Pick signal to noise ratio is calculated using the following equation:

$$MSE = \frac{\sum_{i=1}^{p}\sum_{j=1}^{q}\left(Wmi^{r}_{i,j} - A^{r}_{i,j} + Wmi^{g}_{i,j} - A^{g}_{i,j} + Wmi^{b}_{i,j}A^{b}_{i,j}\right)}{3*p*q} \quad (3)$$

$$PSNR = 10log_{10}\frac{255^2}{MSE} \quad (4)$$

Where Wmi is Watermarked image and A is attacked image.

IV. Experiment Result

In our experiment we have used a watermark to embed into a cover image to construct the watermarked image. Figure-3 shows the watermarked image derived with Cover image and watermark image. The performance of the proposed algorithm is measured through the obtained values. The peak signal to noise ratio (PSNR) and normalized correlation (NC) are used as the performance criteria.

The table-1 describes PSNR values between watermarked image and attacked image. It also demonstrates the NC values of original watermark and the extracted watermark from attacked image.

The PNSR value shows the intensity of noise added on the watermarked image through different types of noise attacks. The lower is PSNR, the higher is the noise added in watermarked image. The higher is normalized correlation (NC) the better is the similarity between original and extracted watermark image.

Performance of PSNR and NC		
Noise	PSNR for Watermarked and Corrupted Image	NC for Original and Extracted watermark
Gaussian	54.0385	1.0
Motion	38.3674	0.9998
Sobel	8.3661	0.9947
Average	39.4771	1.0
Prewitt	8.2853	0.9940
Unsharp	34.9559	0.9955
Log	8.0648	0.9926
Laplacian	8.0350	0.9924
Disk	35.4065	0.9992
Cropping	11.1895	0.9901
Gaussian High pass	10.2247	0.9928
Rotate(90)	11.0870	0.9941

Fig. 4 : (a)Cropping,(b)Deleting,(c)Highpass,(d)Prewitt

From the statistic of the tables it shows that some of the attacks like Sobel, Prewitt, Log, Laplacian, Cropping and Gaussian High pass add higher noise values in the watermarked image, though the extracted watermark from it produce higher NC values. The higher NC values mean the better perceptibility of extracted watermark image. The NC values of this table indicate that the proposed algorithm in this paper is more robust against the above mentioned attacks.

The figure-4 demonstrate watermarked image after diverse attacks.

V. Conclusion

In this paper we have proposed an algorithm for embedding and extracting digital watermark on color image by adopting the technique of DWT and SVD. The color components of the host and watermark image are separated into R, G and B channels separately. Then the value of the watermark image is embedded into R planes. A reverse system is applied to retrieve the watermark.

The experimental results are analyzed with PSNR and NC values. The result shows the robustness of the algorithm against malicious and unintentional attacks. The implanted method has received a highest PSNR and NC values which are 8.035 and 0.9924 respectively. This indicate the strength of robustness of the applied algorithm in this paper.

In future experiment we will concentrate on the new technique to improve the perceptibility of the cover image.

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Detection and Classification of Short Transients and Interruption using Hilbert Transform

By Shilpa R & Dr. P S Puttaswamy
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Abstract- Widespread use of electronics from home appliances to the control of more sophisticated and costly industrial processes has raised the awareness of power quality. Power quality disturbance is generally defined as any change in power (voltage, current, or frequency) that interferes with the normal operation of electrical equipment. The study of power quality and ways to control is a major concerned for electric utilities, large industrial companies, businesses, and even home users. The study has intensified due to equipment have become increasingly sensitive to even minute changes in the power supply voltage, current, and frequency. In electrical energy power networks, disturbances can cause problems in electronic devices so their monitoring is very fundamental. In this paper, we address the problem of disturbance detection by using Hilbert transform which is employed as an effective tool for tracking the voltage waveforms in electrical distribution systems. In addition to this classification of disturbance is carried out by using cross correlation technique. Simulation results obtained shows the accuracy and flexibility of Hilbert transform in detecting the time instants during which the disturbance has occurred. This has been tested for oscillatory transients, interruption and multiple event interruption and sag.

Index Terms: *power quality, hilbert transforms, empirical mode decomposition.*

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Detection and Classification of Short Transients and Interruption using Hilbert Transform

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Index Terms: power quality, hilbert transforms, empirical mode decomposition.

I. Introduction

The electrical power system is expected to deliver undistorted sinusoidal rated voltage and current continuously at rated frequency to the consumers. In recent years, grid users have detected an increasing number of drawbacks caused by electric power quality (PQ) variations. PQ problems have sharpened because of the increased number of loads sensitive to power quality. The problem is difficult to solve since the loads have become important causes of degradation of Power quality. Poor quality of electric power is normally caused by power line disturbances such as impulses, notches, glitches, momentary interruption wave faults, voltage sags, swell, harmonic distortion and flicker resulting in miss operation or failure of end user equipment. Many techniques can be employed for the detection of PQ disturbances, but the number of samples required was found to be large. Because of the above disadvantage, the algorithm becomes more complex and hence it cannot be applied to work in real-time. The disturbance detection algorithm should be able to detect disturbances as soon as possible, regardless of the nature of the voltage disturbance. At the same time, the disturbance estimation algorithm should have a good selection accuracy. In fact, fast detection algorithms may produce false trip operation of the mitigation equipment.

The main task of PQ analysis involves detection, identification, recognition and classification of various types of PQ disturbances. In this paper, we first generate the disturbances namely interruption, transient and sag + interruption. These are generated using IEEE standard equations with the necessary parameters. Decomposition of signal can be performed using empirical mode decomposition (EMD). Next phase is the detection of time instants at which the disturbance is occurring. This can be done by Hilbert Huang transform (HHT) i.e. EMD and Hilbert transform (HT). EMD gives intrinsic mode functions (IMF) for which HT is applied to get the amplitude plot and the amplitude plot gives time value. The final stage is classification and is done by cross correlation. Cross correlating amplitude plot with the standard sine wave will give the correlation coefficients (XCF). By comparing XCF with standard values, signal can be classified as an interruption, transient etc.

II. Literature Survey

Mario Ortiz et al., Proposed an advanced mathematical tool applicable to the recognition and classification of power system transients and disturbances. The Hilbert transform technique has been applied to analyze several short-term and steady events, like a short circuit, a capacitor-switching transient, or a line energisation used the instantaneous frequency to avoid overtraining errors. Simulation results demonstrated shows the performance, accuracy and flexibility of the HT techniques found superior [1]. Likhitha. R, et al., Proposed a mathematical model for a PQ signal generation which was developed and was validated against the real time PQ signal. PQ events such as sag, swell, transient, and harmonics were generated using the mathematical model. Real time signals consisting of PQ disturbances were generated and compared with the results of synthetic signals. Duration of occurrence of PQ disturbance was noted from real time results [2]. Tianshi Wang introduced a detection model to detect accurately interharmonics, based on HHT. The signals containing interharmonics

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were processed by EMD. It determined the instantaneous frequency and amplitude of each interharmonic, and the time of interharmonic mutations [3]. M.Caciotta et al., Provided a model for disturbance estimation by Hilbert transform which tracks the voltage waveforms in electrical disturbance systems. Tracking capability was detected by simulation and was tested for voltage dip, noise and frequency change [4]. Rajiv Kapoor et al., Proposed a method to detect and classify the power quality events based on demodulation concepts. The technique was well tested and detects transients, sag, and swell (for single PQ events) in real-time. Feedforward neural classifier has been employed for classification of PQ events from the knowledge base [5].M.Sushama et al., Proposed two prominent methods for detection and classification of sag and swell. The first one was based on the statistical analysis of adaptive decomposition signals and the second one is a new technique for detecting and characterizing disturbances in power systems based on wavelet transforms. The results obtained by the two methods are compared and tabulated [6].

III. Theory of EMD, HT and Cross Correlation

The EMD process will decompose a signal x(t) into IMFs which have the following properties:

- Each IMF must have exactly one zero between any two consecutive local extrema.
- Each IMF must have zero local mean.

An EMD algorithm decomposes adaptively the signal x(t) into intrinsic mode functions $c_i(t)$, i = 1, 2, …, n and into residue r(t):

$$x(t)= \sum c_i(t) + r(t); \text{ for } i=1 \text{ to } n \quad (1)$$

Where n means the number of IMF functions. Residue r (t) reflects the average trend of a signal x (t) or a constant value. The algorithm for searching of intrinsic mode functions is based on a procedure called "shifting" described in algorithm below.

a) Create upper envelope E_u (t) by local maxima and lower envelope E_l(t) by local minima of data x (t).

b) Calculate the mean of upper and lower envelope i.e... m_1(t)

c) Subtract the mean from original data i.e.

$$h_1 (t) = x (t)-m_1 (t). \quad (2)$$

d) Verify that h_1 (t) satisfies the conditions for IMFs. Repeat steps a) to d) with h_1 (t), until it is an IMF.

e) Get first IMF (after k iterations) i.e.

$$c_1(t) = h_{1(k-1)} (t)-m_{1k}(t) \quad (3)$$

f) Calculate first residue, i.e. $r_1(t)=x(t)-c_1(t)$ (4)

g) Repeat whole algorithm with r_1 (t), r_2 (t) … until residue is monotonic function.

h) After n iterations x (t) is decomposed according to equation 1.

Combination of EMD and HT is called Hilbert Huang transform (HHT). The Hilbert transform is useful in calculating instantaneous attributes of a time series, especially the amplitude and frequency. The instantaneous amplitude is the amplitude of the complex Hilbert transform, the instantaneous frequency is the time rate of change of the instantaneous phase angle. The Hilbert Transform H(t) of a signal S(t) of the continuous variable t is defined as:

$$H(t) = \frac{1}{\prod} \quad \mathrm{P}\int_{-\infty}^{\infty} \frac{S(\eta)}{\eta - t} d\eta \quad (5)$$

In a simple term, the Hilbert transform of a signal effectively produces an orthogonal signal that is phase shifted by 90 degrees from the original signal and independent of the frequency of the signal. Instantaneous frequency and amplitude of IMFs can be calculated as follows:

Instantaneous Amplitude

$$A(t)=\sqrt{S(t)^2+H(t)^2} \quad (6)$$

Instantaneous Phase

$$\phi(t)=\arctan \frac{H(t)}{S(t)} \quad (7)$$

Instantaneous frequency f(t) is found using:

$$\Phi'(t)=w(t)=2*pi*f*t \quad (8)$$

Where

$$w(t) = \frac{S(t)dH(t)\text{-}dS(t)H(t)}{\sqrt{S(t)^2+H(t)^2}} \quad (9)$$

Overall the HHT shows a great promise as a means to classify PQ events because of its flexibility and the ease with which the instantaneous magnitude and frequency information can be interpreted.

Cross-correlation, in simplest terms, is a measure of similarity between two waveforms. For two continuous functions f(t) and g(t), it is mathematically represented as:

$$[f * g](t) = \int_{-\infty}^{\infty} \bar{f}(\Gamma) g(t+\Gamma) d\Gamma \quad (10)$$

Where "*" stands for operation of cross-correlation and f(Γ) represents the conjugate of f(Γ). Cross correlation coefficients (XCF) are also capable of deciding whether a power event is multiple or single.

IV. Implementation

The first step is to generate the disturbances, using IEEE standard equations shown in Table 1. The

plots for these disturbances are obtained using Matlab. By varying the parameters mentioned in the Table 1, required plots can be obtained. Generated disturbance (interruption) shown in Figure 1 is input to EMD process. EMD decomposes the signal into IMF each of which has instantaneous amplitude and frequency. EMD uses the shifting process for decomposing the signal. The true IMF is obtained through EMD algorithm repetition. Once true IMF is obtained, residue function is calculated, until residue is either monotonic or constant. If the residue obtained is either monotonic or constant, then EMD stops. The residual value provides average trend of the input signal. To detect the duration of the occurrence of disturbance in input signal, it is necessary to apply Hilbert transform on the 1st IMF obtained. The reason to choose 1st IMF is because it contains maximum information, energy of the input signal. Apply Hilbert transform for the 1st IMF to get amplitude plots. This Hilbert amplitude plot detects the point of disturbance. The peak indicates the beginning and end of disturbance occurrence and is shown in Figure 1. The above procedure is repeated for transients, multiple event interruption and sag and the plots for the same are presented in Figure 2 and 3.

In the classification phase, the output of the Hilbert plot of disturbance and a standard sine wave of frequency 50Hz is considered as input. Next, is to perform cross correlation between them according to the equation 10. This function provides us the correlation coefficients, XCF obtained is compared with values of single, multiple, interruption or for no event. If the value of XCF <=0. 1, then it is classified as an interruption. If XCF value lies in between 0.5 to 0.95 then signals is a single event, i.e. The signal has single disturbance. If XCF value lies in between 0.1 and 0.5 then the signal is classified as multiple event and the signal has multiple distortion. For all values of XCF >=0. 95, the signal is a pure sine without any disturbance, and hence it is classified as no event. The above condition is tabulated in Table 2. Once the signal is classified as single or a multiple event, it is necessary to find out the disturbances. There is a set of standard values for each disturbance shown in table 3. By comparing these with obtaining XCF, the signal can be easily classified according to the standard form. For all the values of XCF <=0.8, the signal is classified as transient.

Table 1 : Different types of power quality disturbances

Disturbance	Equation	Parameters
Pure Sine	$y(t)=\sin(w_d t)$	$w_d=2*pi*50$
Interruption	$y(t)=\sin(w_d t)*[1-\alpha(u(t-t_1)-u(t-t_2))]$	$0.9<=\alpha<=1$; $T<=t_2-t_1<=9T$;$T=1/50$
Sag	$y(t)=\sin(w_d t)*[1-\alpha(u(t-t_1)-u(t-t_2))]$	$0.1<=\alpha<=0.9$;$T<=t_2-t_1<=9T$; $T=1/50$
Transient	$y(t)=\sin(w_d t)+e^{((t_2-t_1)*(u(t-t_1)-u(t-t_2))} *\sin(2*pi*f_n*t)$	$0.1<=\alpha<=0.8$; $0.5T<=t_2-t_1<=3T$; $T=1/50$; $300Hz<=f_n<=900Hz$; $5ms<=\tau<=40ms$

Table 2 : Type of PQ event with their XCF

Range of XCF	Type of PQ event
>=0.95	None
0.5 to 0.95	Single
0.1 to 0.5	Multiple
>=0.1	Interruption

Table 3 : PQ classification based on XCF

PQ event	XCF
Transient	<=0.8
Interruption	<=0.1

V. Result

Figure 1, 2, 3 shows the detection and classification results of disturbances corresponding to interruption, transients and multiple event. The GUI shows the plots of input signal (disturbances), 1st IMF, residue and the Hilbert plot for the 1st IMF. The correlation coefficient based on which the disturbances are classified are shown, and the results are tabulated in Table 4.

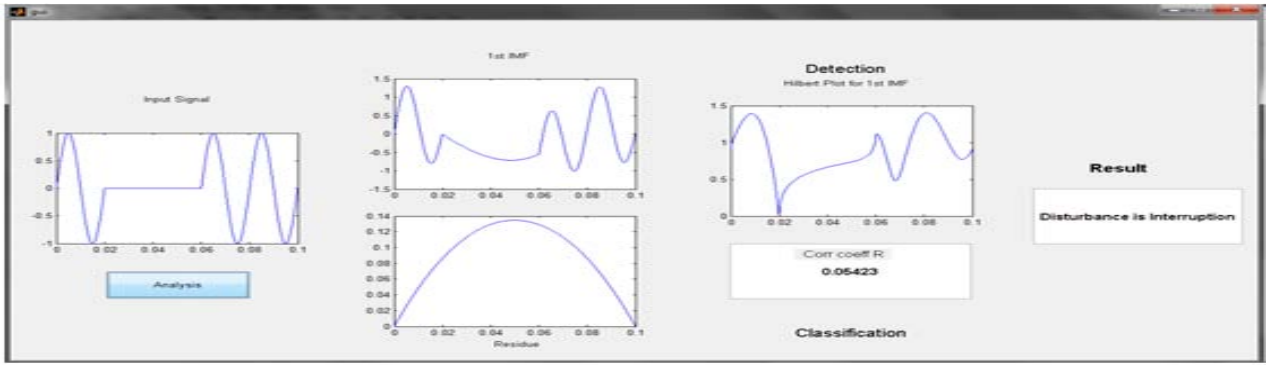

Figure 1 : Detection and classification of Interruption

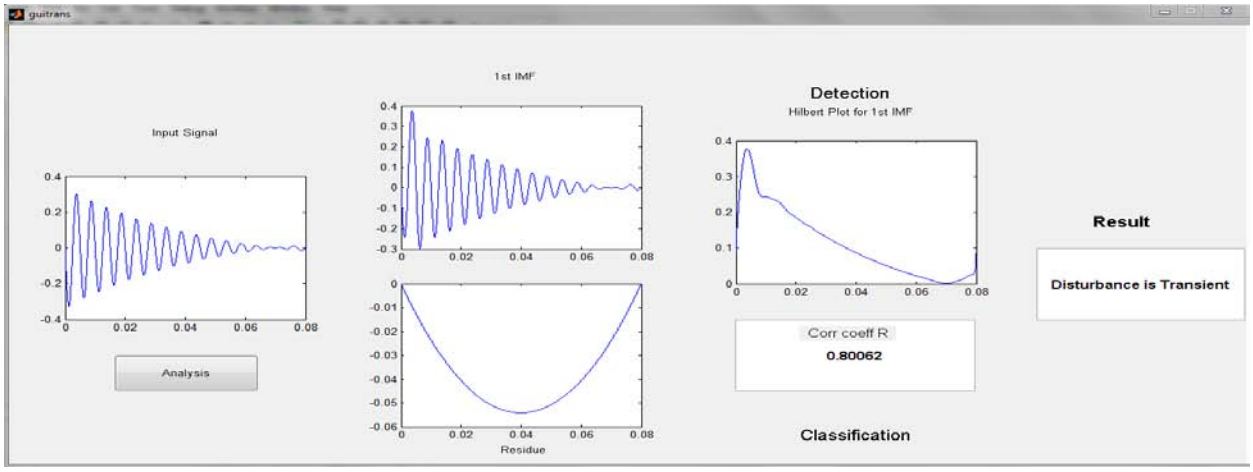

Figure 2 : Detection and classification of transients

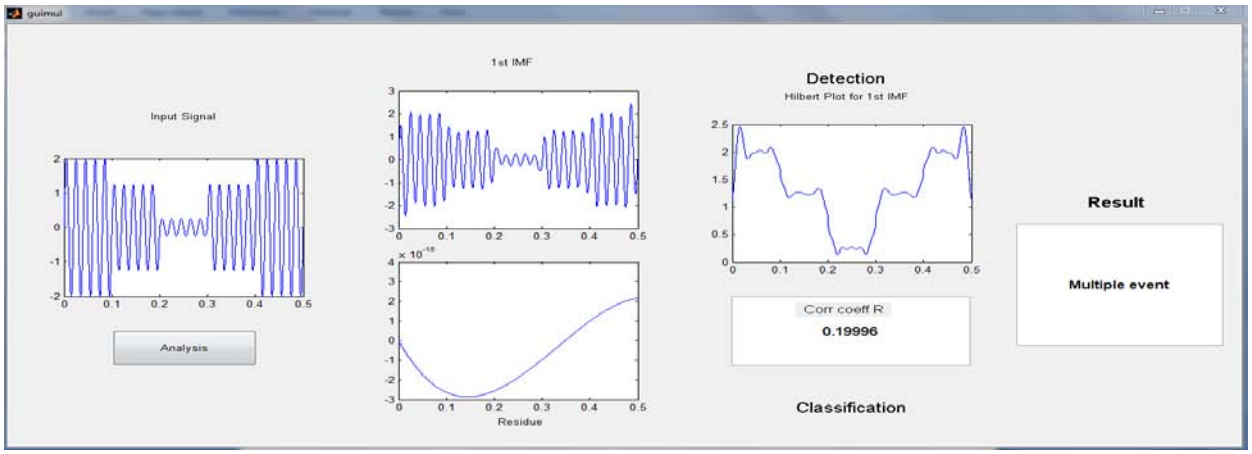

Figure 3 : Detection and classification of multiple event

Table 4 : Results of detection and classification

Disturbances	Detection interval	Correlation coefficients
Interruption	0.02 to 0.06	0.05
Transient	0.01 to 0.08	0.8006
Multiple event Interruption from 0.2 to 0.3 Sag from 0.1 to 0.4	0.2 to 0.3	0.19996

VI. Conclusion

This paper has presented the application of the Hilbert transform to the identification of electric power transients, interruption and multiple distortion by first filtering the signal into the IMF. The signal decomposition method EMD is used to extract signal components, and determine disturbance or quality phenomena components to identify patterns such as the instantaneous frequency of various types of disturbance with a simplified configuration of a power system. The use of instantaneous frequency is to avoid overtraining errors which improves the orthogonality of the results and therefore, the interpretation of them. Simulation result demonstrates that the performance, physical meaning, robustness, accuracy and flexibility of the Hilbert transform techniques are found to be superior.

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A Current Balanced Logic Buffer based Time-To-Digital Converter with Improved Resolution

By Pooja Saxena, K. Hari Prasad & V. B. Chandratre
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Abstract- This paper presents design and implementation of TDC based on time stamping using current balanced logic (CBL) buffer in 0.35 μm CMOS technology. The CBL logic buffer provides smaller delay compared to widely used current starved inverter, allowing better resolution in a given technology node. The CBL buffer based tapped delay line (TDL) provides accurate reference timing signals for time stamping through latching their status by event signal. The time stamping is designed with dynamic range of 40 μs and allows tunable resolution with minimum value of 136 ps by varying CBL delay using off-chip reference voltage. Across process voltage & temperature (PVT) variations, by stabilizing the CBL delay with the help of delay lock loop (DLL), the attained resolution is 174 ps. This TDC is designed to work in two modes- Time Interval (TI) measurement mode and common stop multi-hit mode to enhance scope of its utilization.

Keywords: time-to-digital converter, time stamping, tapped delay line, current balanced logic, delay lock loop, high energy physics (HEP).

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A Current Balanced Logic Buffer based Time-To-Digital Converter with Improved Resolution

Pooja Saxena [α], K. Hari Prasad [σ] & V. B. Chandratre [ρ]

Abstract- This paper presents design and implementation of TDC based on time stamping using current balanced logic (CBL) buffer in 0.35 μm CMOS technology. The CBL logic buffer provides smaller delay compared to widely used current starved inverter, allowing better resolution in a given technology node. The CBL buffer based tapped delay line (TDL) provides accurate reference timing signals for time stamping through latching their status by event signal. The time stamping is designed with dynamic range of 40 μs and allows tunable resolution with minimum value of 136 ps by varying CBL delay using off-chip reference voltage. Across process voltage & temperature (PVT) variations, by stabilizing the CBL delay with the help of delay lock loop (DLL), the attained resolution is 174 ps. This TDC is designed to work in two modes- Time Interval (TI) measurement mode and common stop multi-hit mode to enhance scope of its utilization.

Keywords: time-to-digital converter, time stamping, tapped delay line, current balanced logic, delay lock loop, high energy physics (HEP).

I. Introduction

Time-to-digital converter (TDC) is an important functional unit for accurate time interval (TI) measurement between 'start' and 'stop' events in HEP experiments. In India based Neutrino Observatory (INO) HEP experiment, TI measurement between 'start' & 'stop' with resolution better than 200 ps is required. Also, multiple start transitions along with width of 'start' signal need to be measured over dynamic range (DR) of 32 μs. The measurement of multiple start transitions is used to find delayed events. The width of 'start' signal is used for 'time over threshold' [1] implementation required in time walk error correction.

To cater to above stated requirements in 0.35 μm CMOS technology, this paper presents a design & implementation of TDC based on time stamping [2]. This TDC stamps arrival time of events with respect to reference clock (100 MHz) using tapped delay line (TDL) combined with a counter. The number of bits in counter is chosen as 12 to achieve time stamping range of (212-1) ×10 ns = 40.95 μs, which is higher than the required value of 32 μs. The resolution of TDC depends on the least delay provided by the delay element, used to realize TDL. In the chosen technology, the least achievable delay in current starved inverter based delay element is ~ 400 ps, which does not fulfill the required resolution of TI measurement. To achieve resolution better than that attainable in a given technology in the earlier reported TDCs [3] [4], a delay interpolation technique has been used. This technique requires multiple DLLs to interpolate the delay of current starved inverter, leading to large power & area consumption. In second approach used in [5], a high speed differential delay element has been used, which requires high static current (~1 mA) to provide small delays. In this design, with constrained requirement of low power due to millions of detector channels, a high speed voltage controlled buffer based on Current Balanced Logic (CBL) [6][7] is designed. It has advantages of small area (4 transistors), identical edge transition delays, wide delay regulation range (~1.6 ns) and propagation delay (136 ps), which is smaller than that (~ 400 ps) in current starved inverter. Also, the CBL delay element has less design complexity as both transition delays are controlled by single bias voltage whereas in current starved inverter two bias voltages are needed to control the rising and falling edge delays.

This paper is organized in three sections. Section-II discusses the design and implementation of time stamping based TDC ASIC. The simulation results in support of performance validation of this design are discussed in section-III. Finally, conclusions are drawn in section-IV.

II. TDC ASIC Architecture

The TDC ASIC is designed to work in two measurement modes: 8-channel TI and 4-channel multi-hit, by stamping the arrival time of events with respect to a reference clock (100 MHz). It consists of following blocks: control logic block, Pre-processor, CBL based TDL along with DLL, transition detector, 12-bit coarse counter, 17 fine & 17 coarse registers, memory & its interface logic and readout interface, as shown in Fig. 1(a).

The logic control block enables a 'clock' for TDL and counter on an external 'event reset' signal to initialize the time stamping. Subsequently, it opens a 'dynamic range (DR) window' of duration 40 μs to enable the pre-processor block. It processes the inputs 'start', 'stop' and 'trigger' events for stamping their arrival times within DR window in both the modes of TDC.

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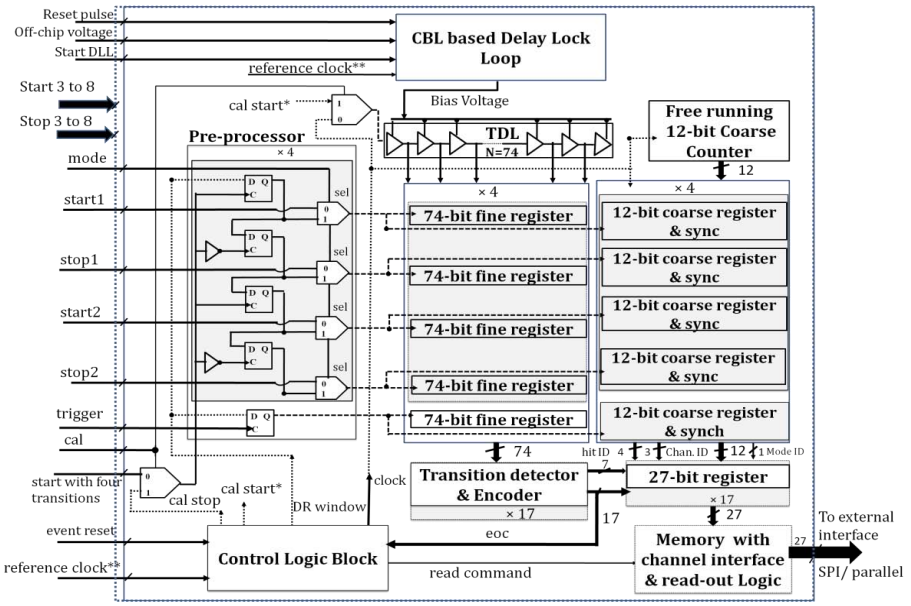
In TI mode, each pre-processor block is dedicated for two channels of TDC. In each channel, arrival times (T1 and T2) of 'start' and 'stop' is stamped independently with respect to clock as shown in Fig. 1(b). The difference of their time stamped values is used to measure TI between them.

In multi-hit mode, each preprocessor block is dedicated to the single channel of TDC to separate out the four transitions (1, 2, 3, & 4) in the 'start' signal. The arrival time of each transition is stamped independently with respect to clock. The difference in time stamped values corresponding to first two transitions is used to measure pulse width of 'start' signal. The stamped times of third and fourth transitions are used to find delayed events. The time of trigger is also stamped with respect to clock to find its associated events within DR window. The design aspects of time stamping are given in sub-section A.

The time stamped data from each channel of TDC is transferred to inbuilt memory. The data transfer is controlled by the logic control block. It issues a read command to the memory; to read the channels only if stop and trigger is present in the window in TI and multi-hit modes respectively. In their absence, the channel data is discarded. The TDC channel data from memory is transferred to external interface by using either Serial Peripheral Interface (SPI) or parallel interface based read-out logic. The resolution of TDC is defined by the CBL delay, which is stabilized across PVT variations by the control voltage provided by DLL. The DLL and time stamping blocks are designed in close proximity of each other to minimize the process induced CBL delay mismatch in both the blocks. Along with DLL, an optional provision for CBL delay tuning by using off-chip reference voltage is designed. To find the tuned CBL delay value, a calibration scheme is designed. The design and implementation of CBL delay stabilization, tuning, & calibration is discussed in sub-section B.



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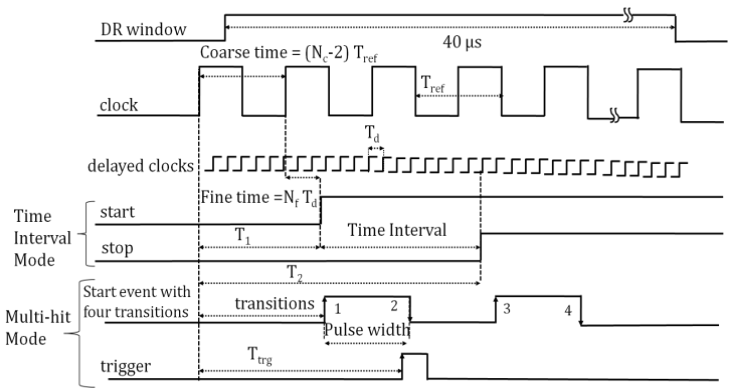


(b)

Fig. 1 : TDC Architecture (a) Block Diagram (b) Timing Diagram

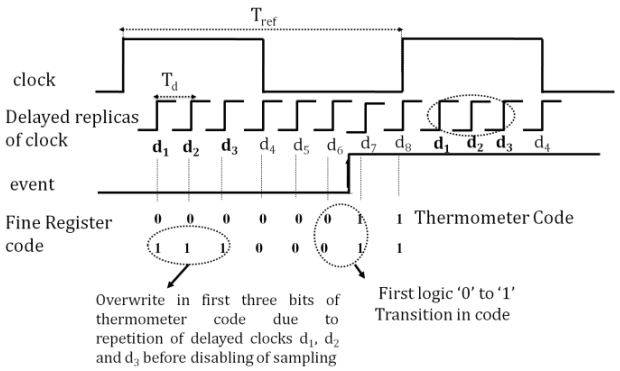
a) Design aspects of Time stamping

The occurrence time of event (start/stop/trigger) is stamped in two parts- coarse and fine (Fig. 1(b)). The coarse time, corresponding to the elapsed full cycles of clock till the occurrence of event, is measured by using 12-bit counter. The fine (fractional) time within one clock period (T_{ref} =10 ns) covered by an event is measured by using TDL.

The TDL is realized by a chain of cascaded 'N' number of CBL buffers each with delay 'T_d', which defines the resolution of time stamping. For stabilized CBL delay of 174 ps, 58 number of CBL buffers are required for TDL to cover a range of one clock period T_{ref} = 10 ns, by using equation (1). However, in this design to allow the least tunable CBL delay of 136 ps at V_{dd} = 3.6 V as resolution for time stamping, 74 CBL delay elements are used in TDL. It provides 74 uniform delayed replicas of applied 'clock' signal with TI of T_d. These delayed clocks are shared among 17-fine registers, 16 for measurement channels (4 channels in multi-hit or 8-channels in TI) and one for trigger channel to measure fine time of events.

$$T_{ref} = N \times T_d \quad (1)$$

The fine time of each event is measured by finding the elapsed number of delayed clocks till its occurrence. To determine this number, two architectures of fine time measurement are analyzed. In the first, the delayed clocks sample and latch the status of event signal in fine register as shown in Fig. 2(a). The first logic '0' to '1' transition count in the thermometer code of fine register gives fine count (N_f). For correct fine count, it is desired to disable the sampling of 'event' status before next clock cycle. However, due to uncontrolled processing delays, the first few bits of fine register in the thermometer code are overwritten before sampling gets disabled.



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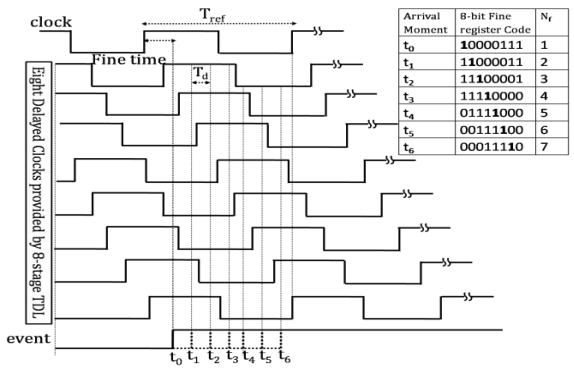
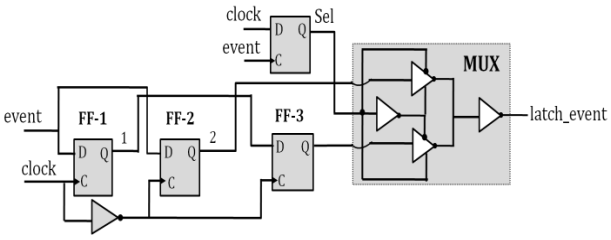


Arrival Moment	8-bit Fine register Code	N_f
t_0	10000111	1
t_1	11000011	2
t_2	11100001	3
t_3	11110000	4
t_4	01111000	5
t_5	00111100	6
t_6	00011110	7

(b)

Fig. 2 : Timing Diagram of fine time measurement for N= 8 delay elements (a) first architecture (b) second architecture

This issue of code overwrite is avoided in second architecture of fine time measurement. Here, the 'event signal samples and latches the status of 74-delayed clocks in fine register as shown in Fig. 2(b). The first logic '1' to '0' transition count in the fine register non-thermometer code gives the fine count (N_f). This transition count is detected by using a transition detector based on magnitude comparison between two consecutive bits of fine register. Further, the encoder converts the 74-bit fine count to 7-bit binary value to reduce the number of bits of fine count. This 7-bit fine count (N_f) multiplied with CBL delay 'T_d' (≥ 136 p s) evaluates the fine time of event with respect to the rising edge of clock cycle in which it lies. The elapsed full clock cycles before arrival of event is measured by coarse time.



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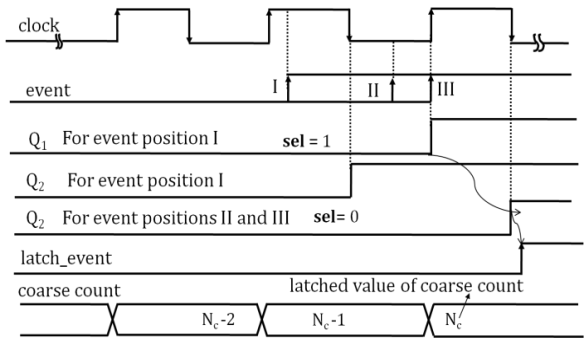


(b)

Fig. 3 : Dual Edge Synchronizer (a) Timing Diagram of (b) Schematic Diagram

In coarse time measurement of event, it samples and latches the status of free running counter. While sampling if event occurs during switching of counter, the latched count will be incorrect due to setup time violation or dead zone in the coarse register. Also, the coarse and fine counts need to be synchronized to avoid an error of one coarse count. To address these issues, a dual edge synchronizer based on the dual synchronization scheme [8] is designed as shown in Fig. 3(a). This synchronizer samples & latches the status of counter when it is in idle state, thereby avoids timing violations in coarse register. The latched count of elapsed clock periods has one extra count, which is irrespective of event position (I, II & III) within a clock period as shown in Fig. 3(b). This is carried out by synchronizing the 'event' signal to both the rising and falling edges of clock, resulting in the generation of latched signals Q_1 and Q_2 respectively. A MUX selects the signals 'Q_1' or 'Q_2' as per the 'event' position to obtain the 'latch_event' at falling edge of clock in next cycle. It samples and latches the count status 'N_c'.

The measured coarse count (N_c) and fine count (N_f) are used in calculation of arrival time (T) of event with respect to clock by using equation (2). The considered value of coarse count is 'N_c-2' as two counts are subtracted- one due to synchronization scheme and other due to addition of fine time with coarse time (Fig. 1(b)).

$$T=(N_c-2)\times T_{ref}+N_f\times T_d \quad (2)$$

b) CBL delay stabilization & Tuning

The CBL delay in time stamping block is stabilized across PVT variations by the control voltage obtained from DLL as shown in Fig. 4. The DLL is enabled by applying a rising edge of 'start DLL' signal in the 'start control circuit'. It provides a clock (clock_TDL) for reference TDL, whose initial delay is set to minimum value (4.09 ns) by pre-setting the capacitor voltage through 'preset switch' to avoid false locking in DLL. The feedback loop consisting of phase detector, charge pump and filter capacitor, locks the TDL delay to the half clock period (5 ns) of reference clock (complementary clock_TDL) across PVT variations in acquisition time of 124 cycles of clock. The attained stable voltage across filter capacitor is used to stabilize the CBL delay to 174 ps across PVT variations.

The half clock period locking in DLL is designed to reduce its acquisition time. To further reduce the acquisition time, the initial delay of reference TDL can be fixed nearer to the target value by 'preset switch'. Thus, the present architecture achieves better performance as compared to earlier reported architecture [9][10], where the TDL delay with load of fine register channels is locked to reference clock period in long acquisition time. Along with CBL delay stabilization, an option for its delay tuning using off-chip reference voltage is designed. It is selected by resetting the D flip-flops used in start control circuit. It turns on the 'preset switch' as well as disables DLL, so that the filter capacitor is charged to the off-chip reference voltage.

The voltage across filter capacitor is applied to TDL (time stamping block) for delay stabilization or tuning through bias circuit [8]. The purpose of bias circuit utilization is to avoid the loading of long delay lines on filter capacitor (C) by charge sharing with the parasitic capacitances of TDL.

The tuned value of CBL delay is determined by measuring on-chip generated time intervals of 10 ns and 5 ns in between 'calstart' and 'calstop' signals (Fig. 1(a)). These time intervals are generated by using reference clock. The calibration mode is selected by 1-bit 'cal' signal. The CBL delay 'T_d' is given by the difference of measured time intervals by using equation (3), where N_{f1} and N_{f2} are the counts of fine registers corresponding to 10 ns and 5 ns time intervals respectively. The calibrated CBL delay is used to calculate the final stamped time of event using equation (2).

$$T_d = \frac{(10-5)ns}{(N_{f1}-N_{f2})} \quad (3)$$

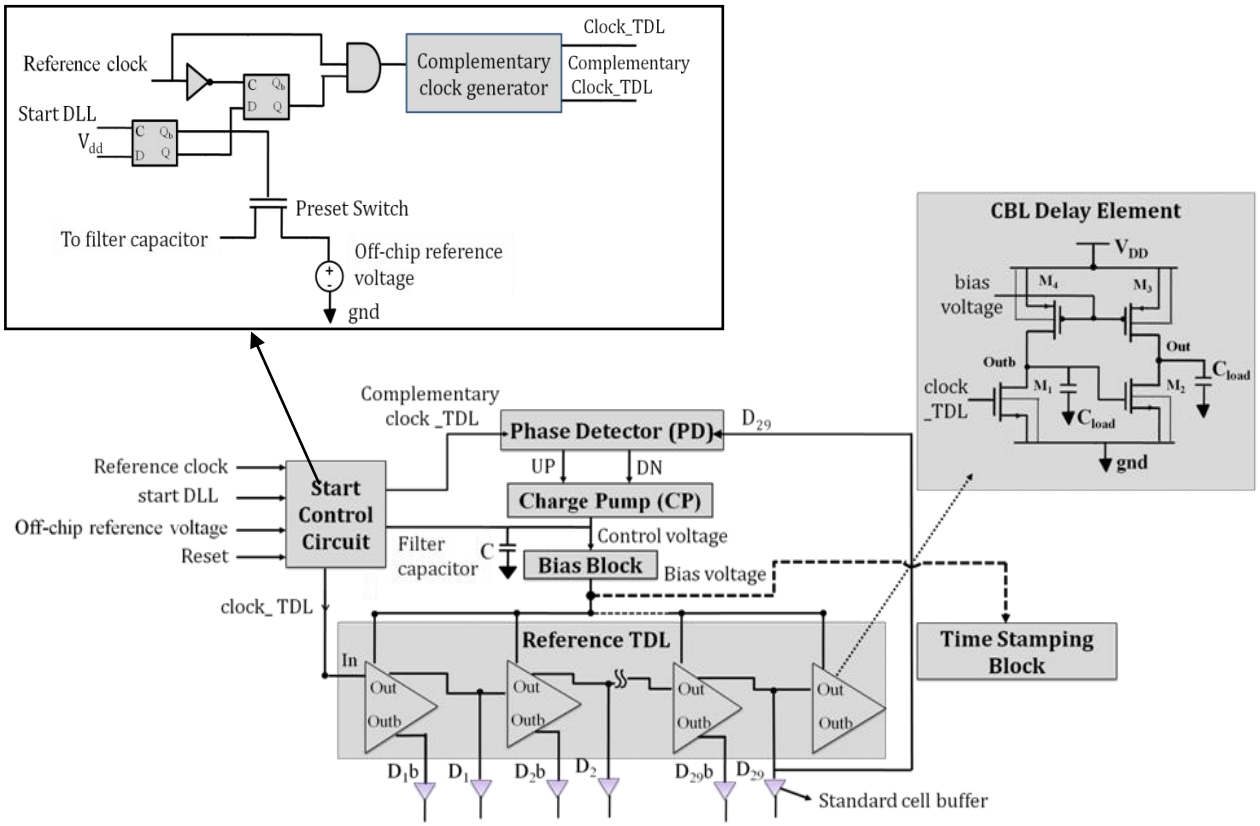
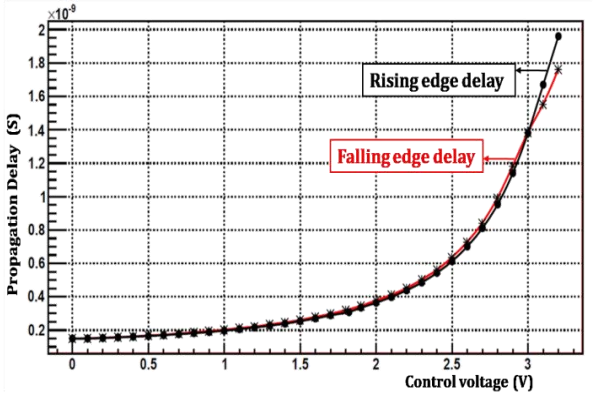


Fig. 4 : Block Diagram of CBL delay element based DLL with start control circuit

III. Simulation Result

The post layout performance of CBL delay element is verified by using Spectre simulator across design process corners. The CBL delay characteristic for both rising and falling edge transitions is shown in Fig. 5(a) on typical corner. Fig. 5(b) depicts the CBL rising edge delay across process corners, where on the worst case slow corner (WS), the smallest attainable delay is 200 ps. The performance of post layout CBL based DLL is also verified using specter simulator across design process corners for CBL delay of 174 ps at clock frequency of 100 MHz. Fig. 6 shows the profile of control voltage versus acquisition time.



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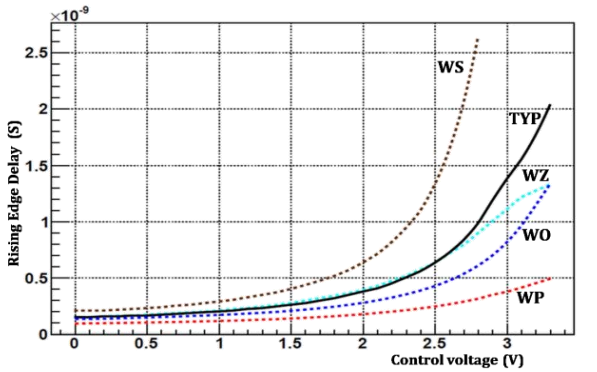


(b)

Fig. 5 : Delay versus Control Voltage Characteristic of CBL DE at 3.3 V supply voltage (a) Typical corner (b) Design Process Corners

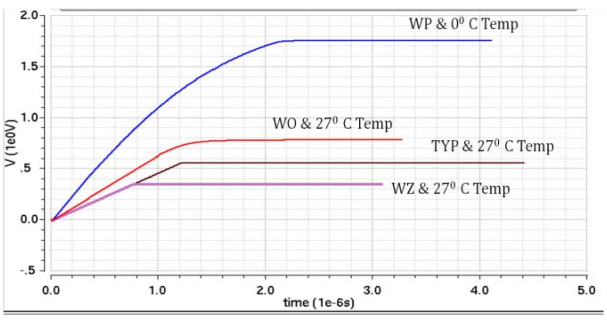


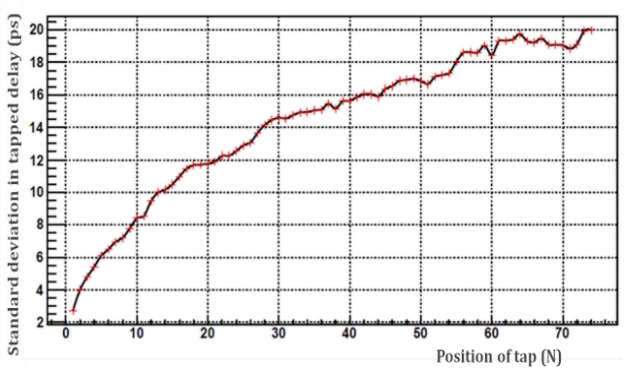
Fig. 6 : Control voltage vs. acquisition time

The variation in tapped delays for 74-stage TDL due to local process variations is evaluated by using Monte Carlo simulator for 100 runs. The standard deviation of delay variation on each tap of TDL is shown in Fig 7(a). The maximum standard deviation of delay at the end (output of 74th tap) of TDL is 20 ps.

The ripple of 40 µV in the DLL control voltage after attaining the locked state also causes variation in tapped delays. This is evaluated by simulating the extracted netlist of TDL with DLL for 1000 number of clock cycles. The standard deviation of delay variation is shown in Fig. 7(b) with maximum value of 0.14 ps at the end of delay line.

To find the variations in tapped delays due to device component noise, noise coupling through parasitics and variation in layout drawing, the extracted netlist of TDL is accurately simulated by Spectre simulator with transistor noise models. The maximum delay variation is 17 ps as shown in Fig. 7(c) and its RMS value is 10 ps.

The RMS quantization error for the resolution of 174 ps is evaluated by: 174 ps/$\sqrt{12}$ = 50.28 ps. The total theoretical RMS error in TI measurement, considering above evaluated RMS delay variations and quantization error, is calculated as 55.02 ps.



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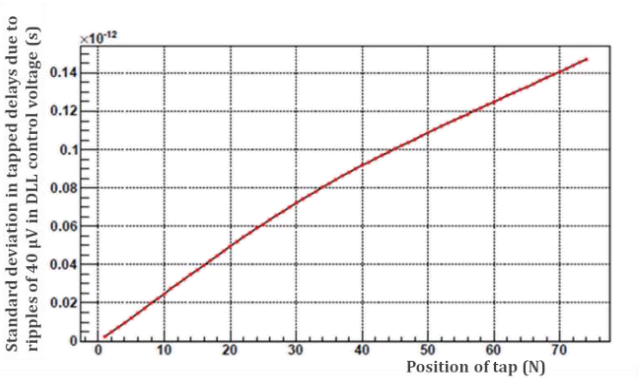
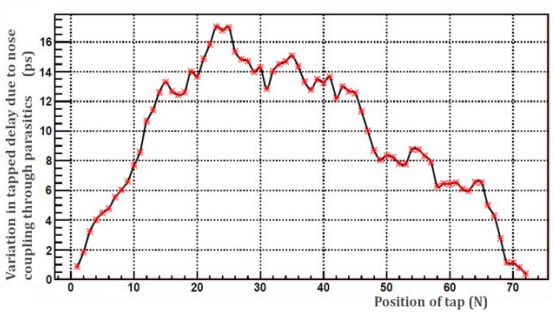


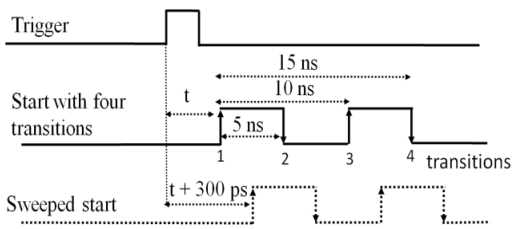
(b)



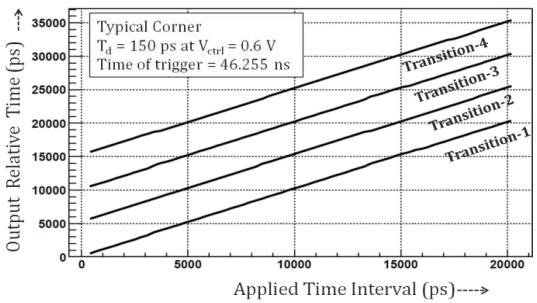
(c)

Fig. 7 : Standard deviation of tapped delays versus Position of Tabs (a) due to device mismatch using Monte Carlo simulator (b) due to ripples of 40 µV in control voltage provided by DLL (c) variation in tapped delay due to noise coupling and device component noise

The performance of time stamping is verified by using Spectre Verilog simulator. The linearity of measured output versus applied input characteristic is verified by applying a linear sweep of start event (Fig.8 (a)) in steps of 300 ps with respect to trigger over 20 ns with the help of Verilog test bench. On typical (TYP) corner, the measured relative time of hits is in agreement with the applied time steps as shown in Fig. 8(b). This test is also successfully carried out on slow (WS) corner for CBL delay of T_d = 200 ps (control voltage = 0.1 V) as shown in Fig. 9(a). The linearity of time stamping over full dynamic range of 40 µs is also verified by applying a linear sweep of 'start' with time steps of 223 ns with respect to trigger. Fig. 9(b) shows the plot of relative time versus applied time step for first transition on TYP corner.

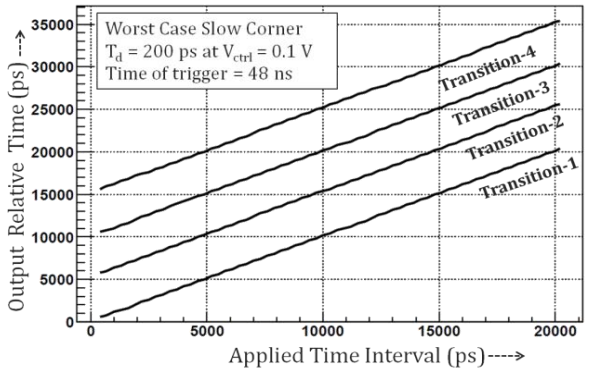


(a)

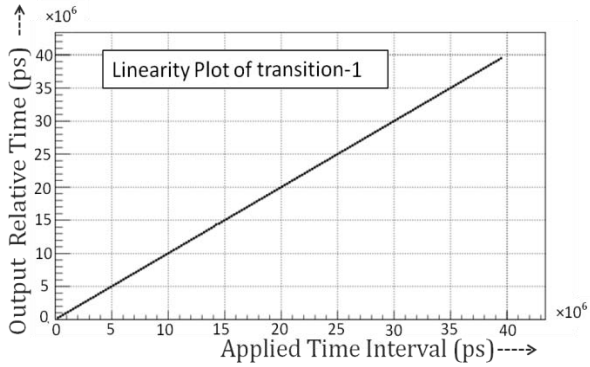


(b)

Fig. 8 : (a) Applied Input pattern of 'start' signal (b) Plot between Relative Time versus Applied Time on typical corner



(a)



(b)

Fig. 9 : Plot between Relative Time versus Applied Time (a) on WS corner with Td = 200 ps over 20 ns range (b) On typical corner with resolution of 150 ps over 40 μs range

IV. Conclusions

The TDC based on CBL logic achieves improved resolution in 0.35μm CMOS technology. The designed architecture of time stamping allows tunable resolution with least value of 136 ps. Across PVT variations; the attained resolution is 174 ps by stabilizing the CBL delay with the help of DLL. The CBL buffer provides identical rising and falling edge delays, which enables to control both delays with a single DLL feedback loop which in turn reduces design complexity. The designed TDC can be utilized in TI and Multi-hit operating modes with dynamic range of 40 μs. The multi-hit operating mode features pulse width measurement of 'start' signal with duration better than ~5 ns, which is independent of used clock frequency. Also, it enables measurement of delayed events over range of 40 μs. This design is successfully tested for its linearity as well as robustness across design process corners. The theoretical RMS error in time interval measurement is calculated as 55.02 ps.

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27. Refresh your mind after intervals: Try to give rest to your mind by listening to soft music or by sleeping in intervals. This will also improve your memory.

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Final Points:

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- Significant conclusions or questions that track from the research(es)

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	A-B	**C-D**	**E-F**
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Introduction	Containing all background details with clear goal and appropriate details, flow specification, no grammar and spelling mistake, well organized sentence and paragraph, reference cited	Unclear and confusing data, appropriate format, grammar and spelling errors with unorganized matter	Out of place depth and content, hazy format
Methods and Procedures	Clear and to the point with well arranged paragraph, precision and accuracy of facts and figures, well organized subheads	Difficult to comprehend with embarrassed text, too much explanation but completed	Incorrect and unorganized structure with hazy meaning
Result	Well organized, Clear and specific, Correct units with precision, correct data, well structuring of paragraph, no grammar and spelling mistake	Complete and embarrassed text, difficult to comprehend	Irregular format with wrong facts and figures
Discussion	Well organized, meaningful specification, sound conclusion, logical and concise explanation, highly structured paragraph reference cited	Wordy, unclear conclusion, spurious	Conclusion is not cited, unorganized, difficult to comprehend
References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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