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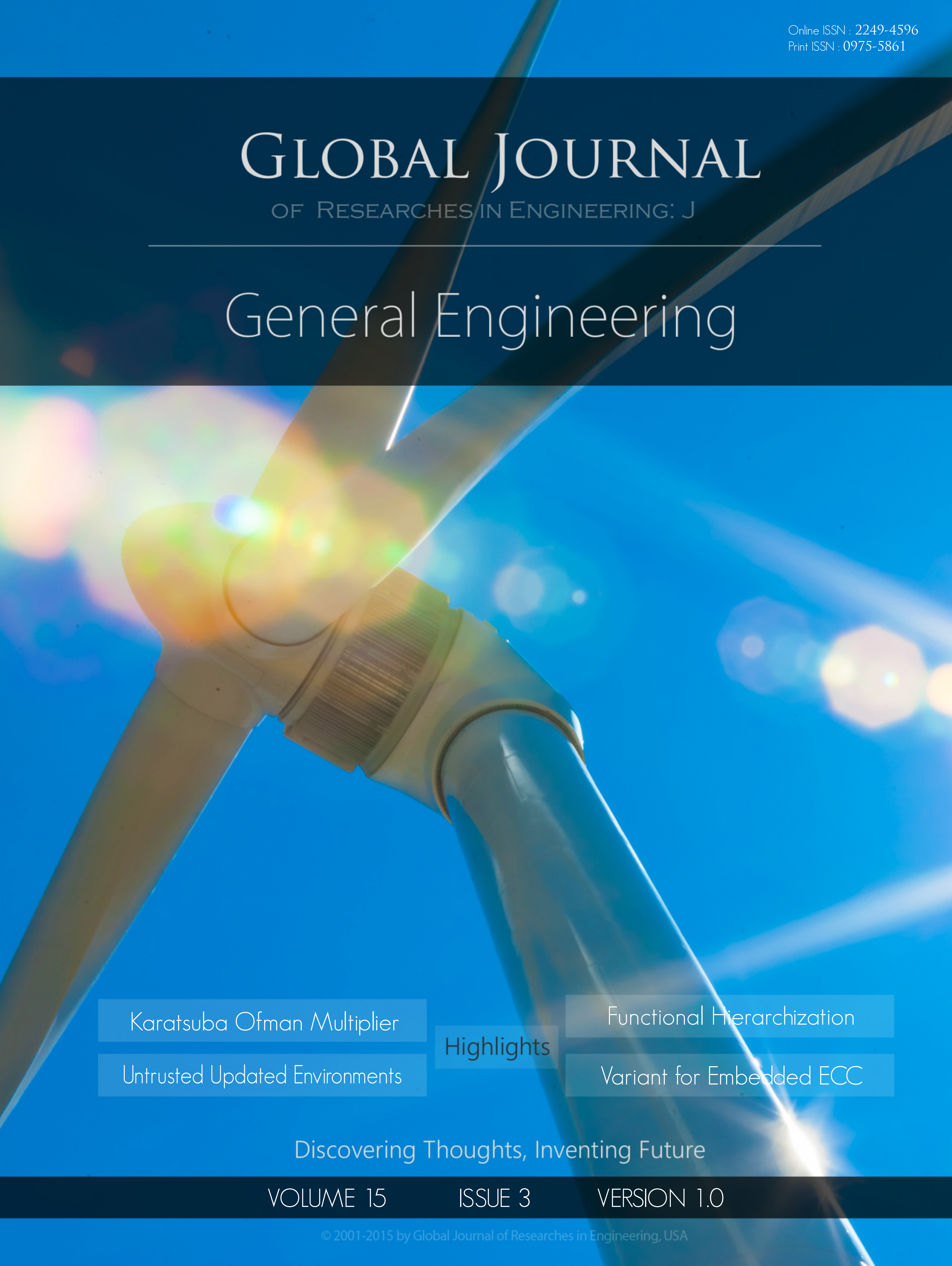

Karatsuba Ofman Multiplier

Untrusted Updated Environments

Highlights

Functional Hierarchization

Variant for Embedded ECC

Discovering Thoughts, Inventing Future

VOLUME 15 ISSUE 3 VERSION 1.0

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Proposal for a Methodology based on Functional Hierarchization for Product Development

By Adriana Yumi Sato Duarte, Marilia Colozio Favaro, Fabio Mazzariol Santiciolli & Franco Giuseppe Dedini

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Abstract- This research aims to permit a simultaneous visualization of primary and secondary functions, sub-functions and subsystems in order to establish, according to its position in the plane, the influence on the overall function and how it can be inserted into the product design. The methodology described consists of an in depth-study of the functional deployment starting from a basic need. Since it is a conceptual study with a philosophical approach, three hypotheses underlie this methodology: the union of two techniques of functional deployment is not possible since there is no correlation; the union of two functional deployment techniques provides similar result if applied separately or the union of two functional deployment techniques provides better results since it allows a comprehensive view of the project. Until this point, this research suggests the union of the two functional deployment techniques provides better results since it allows a comprehensive view of the project.

Keywords: *function; functional deployment; design methodology; design tools; product design.*

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Adriana Yumi Sato Duarte [α], Marilia Colozio Favaro [σ], Fabio Mazzariol Santiciolli [ρ]
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I. Introduction

The key factor for the product development is design methodology: an innovative and iterative process to design a product by relating functional requirements and customer needs [4]. A technique that encompasses the study and the systematization of a function is the Functional Analysis, which allows the transcription of consumers' needs in a semantic structure that, afterwards, may be broken down into sub-functions until the most basic and simple level is achieved.

Authors such as [2,3, 6,9, 16, 17, 21] describe function and functional analysis from different points of view. However, there is a consensus among these authors that the function deployment technique must be inserted into the stage of concept generation, in which consumers' needs are described and broken down in order to apply creativity tools later.

The functional analysis can be classified in two groups: the function structure and the function tree. Some authors [9, 16, 21] proposed studies on the function structure:a chart that encompasses the functions and their connecting flows. The function tree based on "why-how" approach was a consequence of the Value Analysis/Value Engineering described by Lawrence D. Miles[6]. The most widespread function tree is the Function Analysis System Technique (FAST) by Charles By the way.

Although both functional analysis are well established and supported a great number of projects around the world [1] asserts that function structures demand a high level of abstraction from the designer that can result in ambiguous or redundant functions. Moreover, the function trees do not reflect the connecting flows between the functions and the correlation between the functions and the product components.

Two functional basis to reduce the cases of redundancy and ambiguity were proposed by [9, 18]. However, even if the functional deployment is guided by a functional basis or taxonomy, some cases of redundancy and ambiguity will still remain [1].

On the other hand, some efforts have been made to correlate the function trees to the product components. [25] Proposed the intersection between the FAST diagram and the components by means of the "Removal and Operation" technique. [13] implemented the integration between the Function Analysis System Technique and the Axiomatic Design Theory to boost the capacity of defining the functional requirements and correlate the functions with others design domains.

The debate regarding different approaches for functional deployment is encouraged by [7], who explains that the function definitions are complementary and the coexistence of various techniques is beneficial to the design process and design teaching.

The present paper contributes to the debate about the coexistence of the design methodologies. Assuming that both function tree and function structure start from the product overall function, it is proposed a technique that merges the function structures to the function trees. Thus, it allows a simultaneous visualization of primary and secondary functions, sub-functions, and sub-systems aiming to establish, according to their position, their influence upon an overall function.

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The design methodology described in this research consists of an in-depth and conceptual study of two functional deployment techniques, based on By the way [3] and Pahland Beitz[16]. Section 2 describes different function definitions as well as establishes the function definition adopted in this paper. Section 3 is a literature review about functional analysis. Are search gap is reported in Section 4.The main goal of this paper, which is the proposal of a design methodology based on the literature review and the research gap, is presented in Section 5. Section 6 exemplifies the use of the proposed design methodology by analyzing a Hot Air Popper. Section 7 presents concluding remarks and discusses directions for future research.

II. Function Definition

There is an intense academic debate regarding the function definition. One example of function definition is proposed by[18] and states that a function is the operation to be performed by an artifact or a device. According to [23], function is the relation between the inputs and the output of a system or particular solution, in overall or local positions. Moreover, [9] emphasize that the functions are performed by the products in order to fulfill customer needs.

There are several other definitions for the term function in literature. [24] Explains this fact as a conceptual anomaly: function is a key term but there is no general agreement about its definition. However, it is indicated that the function definitions usually refers to “goals of the device”, “actions with the device”, “behavior of the device” and/or “structure of the device”. Finally, [7] investigated the awareness about the functional concepts among the designers and engineers who worked in product development in industry. As a result, it was noticed that they misused the word “function” for behavior, purpose or performance of a product. Furthermore, when these professionals were asked to describe a functional deployment of a product, many of them neglected the methodologies proposed by literature.

In order to avoid this type of misuse, we will adopt the definition of function as a description of desired or necessary capabilities that make the product accomplish its objectives by using a semantic structure of a verb that indicates an action, and a noun which is the object of the action.

III. Functional Analysis Methods

Functional analysis may be applied to the different stages of product development, but it is usually associated with the concept generation stage, before the feasibility study stage [2, 16, 17, 21, 22]. Due to the ease of measuring, behavior and performance are two terms associated with functions [21].

The functional analysis of a product is described in different ways by literature. According to [21], firstly, one must find the overall function to be carried out so as to describe it in a black box, in which the input and the output of material, energy and signal are considered. The second stage of this technique is to describe the sub-functions involved in the system, so as to guide the search for solutions in order to achieve a better understanding of the problem and to make the correlation between components and function easier.

Following the same line of reasoning [17] describe function modeling starting with the determination of an overall function so as to structure, afterwards, a function tree, with black boxes and establishing boundaries. Also, according to the authors, function modeling allows the creation of alternative structures to meet the overall function by means of (a) division or combination of functions, (b) alteration in specific dispositions, (c) alteration in the type of connection, and (d) alteration in the limit of the system.

A method of function deployment in five steps is described by [22] and [5], so as to divide a complex issue into sub-issues. The first step is based upon the clarification of the issue, including mission, consumer needs and product specification. After that, the issue is subdivided and described in black boxes. At this point, the author emphasizes that the objective is to describe the functional elements of the product without involving a specific technological principle [22]. The second step is to research external information, by means of interviews with users, consulting specialists, patents and the literature. The third step presents the same technique, but the search is internal, based on both individual and collective knowledge. The fourth step is exploring systematically. At this point, the function analysis is developed to generate benefits related to the identification of a solution that may seem irrelevant at first glance, to the adequate allocation of resources, and to refinement upon dividing the issue. Next, it is necessary to combine solutions in a systematic manner. Finally, the fifth step consists of reflection and the identification of opportunities for improvement [5, 22].

The axiomatic design proposes that the design is composed of four domains: the customer domain, the functional domain, the physical domain and the process domain. The customer domain contains the customer needs and/or the attributes the customer requires from the product. The requested needs and attributes are translated into functional requirements inside the functional domain. Design parameters are set in the physical domain in order to satisfy the functional requirements. Finally, the process variables are established in the process domain to accomplish the design parameters set in the physical domain [19]. The correlation between the members of each domain is verified in a “zigzagging” process that requires attention and experience from the design team because it defines the product coupling and the hierarchies for the functional requirements, the design parameters and the process variables [11]. It is stated that products with minor coupling present superior design. The couplings can be organized in a matrix base, making possible the design of large systems such as cargo/public transport [20].

a) Value Analysis (VA)

The functions of a product are classified according to their hierarchy or purpose. The classification of functions according to their purpose allows the determination of use value, which enables the functioning of the product, and esteem value, a characteristic that makes the product attractive to consumers. Besides, use function must be measurable, while esteem function is, in most cases, immeasurable [15].

Regarding the hierarchy, there are the overall functions, the basic functions and the secondary. The overall function explains itself the existence of a product. The primary functions are placed above the overall function and are the ones responsible for making the product work. Without them the product will have its value decreased and may lose the identity. Finally, the secondary functions support or enhance the basic functions [2].

As value analysis (VA) is a systematic analysis of the characteristics of a product, it requires the knowledge of its functioning [2]. Thus, VA is executed by a group of designer selected taking into account their expertise in specific domains related to the product on development process; this group is coordinated by a VA expert [4]. The first step of VA is to generate the functions of the product, asking what the product "does", and not only what the product "is". After determining the functions, it is necessary to organize them systematically in a function tree.

The Function Analysis System Technique organizes functions schematically, emphasizing their relations and hierarchy. Upon developing a FAST diagram, the designing team is questioned regarding (a) the reasons for the existence of the product, (b) the critical path between functions and, (c) the definition of the functions. This happens by using the terms "Why?" and "How?"[3] as shown in figure 1.

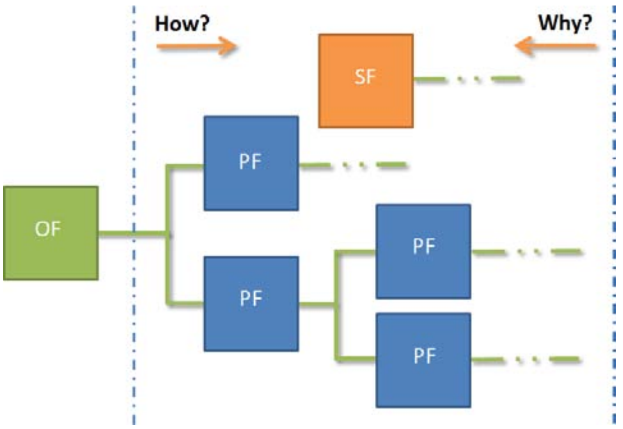

Fig. 1 : FAST Diagram

The functions expanded to the "How Direction" answer how the major function can be performed. In the opposite way, the functions expanded to the "How Direction" answer the reason why the inferior minor functions are performed. The first step in this top-down functional decomposition is the determination of the Overall Function of the product. Going through the "How direction", the Basic Functions are found, than the sub-functions are defined. At the same level of abstraction, Secondary Functions may arise. They may contribute with the performance of the Overall and Primary Functions and/or with the product value, but they also can be harmful or undesired but necessary functions [10].

b) Function Deployment According to Pahland Beitz

The Pahl and Beitz'sFunction Deployment is established above functional structures. It is widely accepted all over the world because it is closer to industrial practice and human thinking system [14]. [16] Define overall function as the overall relation between the input and output of a plant, a machine or assembly. Therefore, input and output, which consist of material, signal, and energy flow, are represented by different types of line in a block diagram. If the overall function is complex, it is necessary to divide it into sub-functions, so as to seek simple and unequivocal solutions.

First of all, the authors indicate that sub-functions must be structured around a main flow. When the function structure reaches the lowest level of complexity, the next step is to detail auxiliary flows and their sub-functions. Thus, function deployment continues until a simpler level is reached, such as described in figure 2. For didactic reasons, these functions are named as Pahl and Beitz functions in this paper.

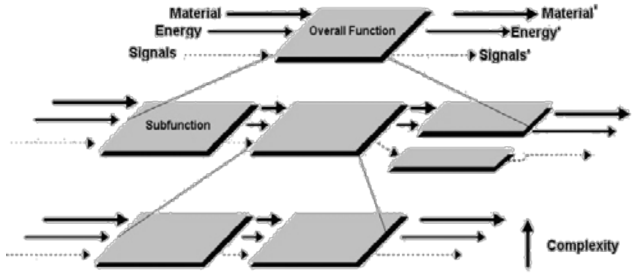

Fig. 2 : Function Structure. Adapted from [16]

IV. Research Gap

The literature presents well established tools and methodologies for the functional deployment in function trees or in function structures. On the other hand, there is a debate about the different kinds of functional analysis, and their possible complementary relations. Also some studies have proposed kinds of hybrid methodologies, however there is a lack of proposals on the explicit merge of a functional tree with a functional structure. The present article intends to contribute to the academic debate by investigating this gap with the proposal in the next section.

V. Proposal for a Design Methodology based on Function Deployment

The methodology described below consists of an in-depth study of function deployment starting from a basic need. This study derives from functional analyses described by Bytheway [3] and Pahland Beitz [16]. As this is a conceptual study with a philosophical approach to these two classical authors in this field, three hypotheses permeate this research: (a) the combination of both function deployment techniques is not possible because they do not present a correlation; (b) the combination of both function deployment techniques presents a similar result if they are applied separately; (c) the combination of both function deployment techniques presents a superior result because it enables an encompassing view of the design.

For didactic purposes, the proposed methodology is divided as figure 3 shows.

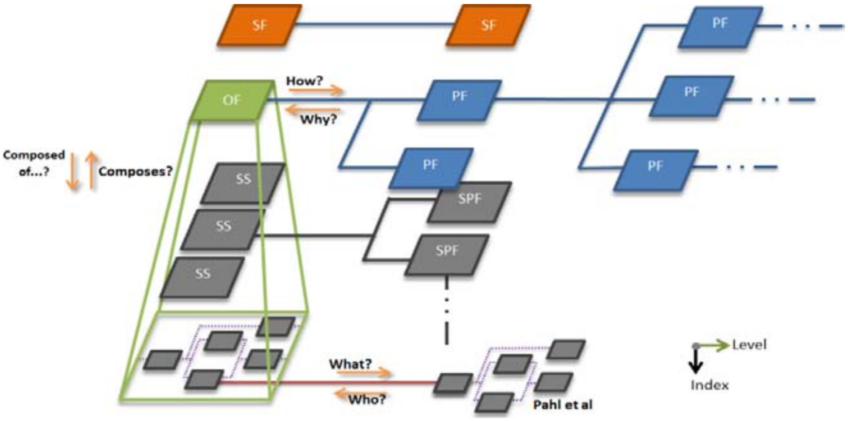

Fig. 3 : Design Methodology based on function deployment

This methodology starts from an Overall Function (OF) and goes on to function deployment with the determination of Primary Functions (PF) and/or Secondary Functions (SF), which, afterwards, are divided into Primary Sub-functions (PSF) and/or Secondary Sub-Functions (SSF), which are related to Sub-systems (SS) that, in turn, make up the Overall Function (OF).

Based on this information, the proposed methodology consists of the following steps:

Step 1: The basic need is described by an Overall Function (OF), which consists of an overall and desired relation between the input and the output of a product, with a view to accomplishing an overall task. In this context, the black box is of most importance so as to indicate the input and output parameters of the system, as in figure 4.

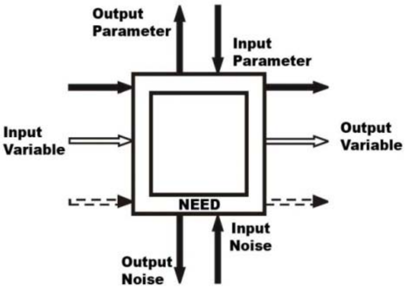

Fig. 4 : Step 1: The overall function and its input and outputs

Step 2: The Overall Function (OF) is divided into sub-systems, which correspond to the components that constitute the overall task. Moreover, each sub-system may be divided into new sub-systems so as to reach the basic sub-system, as [16] propose. Given that, as mentioned before, there is no consensus among authors regarding nomenclature and terms, this proposal indicates that sub-systems should be obtained by means of asking “Composes?” and “Composed Of?”, as shown in figure 5. Nomenclature at this stage follows the pattern “sub-system n.x”, in which “n” is the level of deployment and “x” is the index of the sub-system at an “n” level.

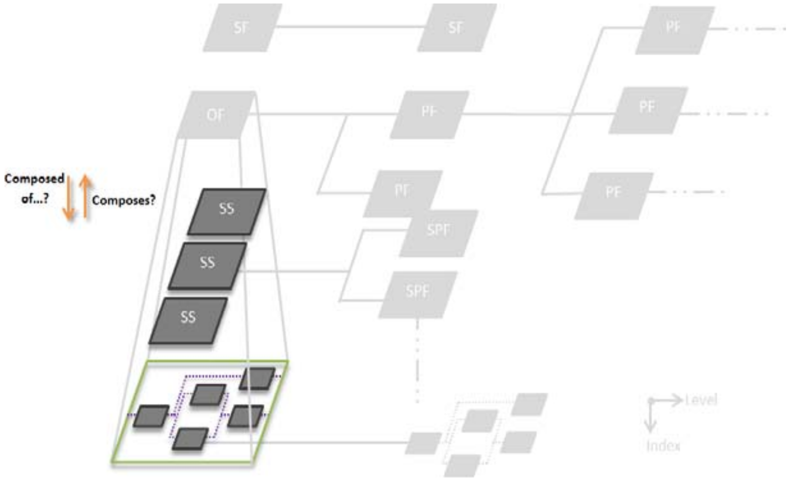

Fig. 5 : Step 2: Sub-systems and components deployment

Step 3: The Overall Function (OF) is divided into Primary Functions (PF), which correspond to how the OF is carried out, as in figure 6. Moreover, each primary function may be divided into new primary functions so as to reach the basic primary function, as [6] proposes. In this case, the terms “How?” and “Why?” are used for deployment. The nomenclature at this stage follows the pattern “primary function m.y”, in which “m” is the level of deployment and “y” is the index of the primary function at an “m” level.

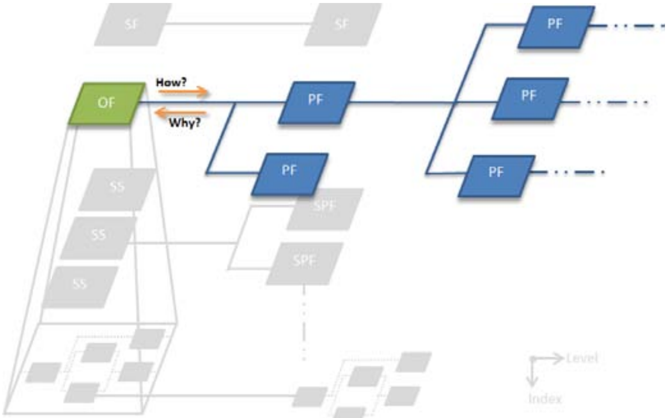

Fig. 6 : Step 3: Primary Functions deployment

Step 4: Secondary Functions (SF) are related to the overall function (OF) and, as it is a combined value, their deployment is indicated by the authors of this research. By doing this, SFs can be divided into new secondary functions so as to reach the basic secondary function, forming the basis for the questions recommended by[3], as indicated in figure 7. Nomenclature at this stage follows the pattern "secondary function m.y", in which "m" is the order of deployment and "y" is the index of the primary function in an "m" order.

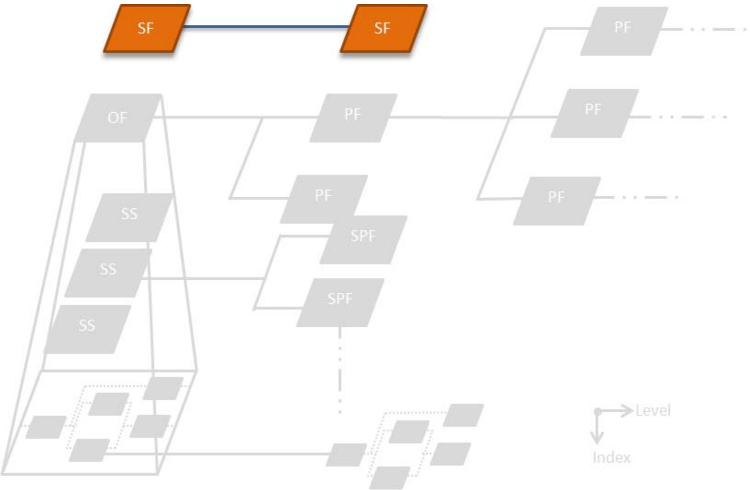

Fig. 7 : Step 4: Secondary Functions deployment

Step 5: Both primary and secondary functions may still be divided into sub-functions using Pahl and Beitz [16] deployment, as in figure 8. Thus, nomenclature at this stage follows the pattern "primary sub-function n.y" and "secondary sub-function n.y", in which "n" is the level of deployment and "y" is the index of the primary or secondary function at an "n" level.

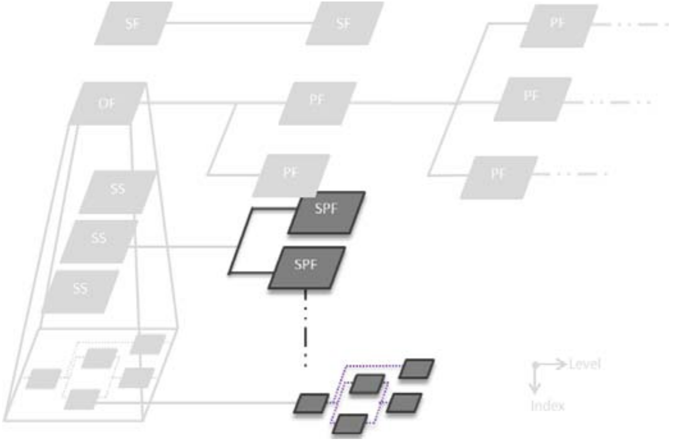

Fig. 8 : Step 5: Sub-functions deployment based on Pahl and Beitz[16] technique

Step 6: After describing the functions, sub-functions, and sub-systems, the last step is to relate basic sub-functions to basic sub-systems. In the end, it is still necessary to eliminate redundancies or repeated elements so as to make the design uncoupled and modular, a design in which each sub-function relates only to a single sub-system.

This methodology shows the sequence of functions, according to levels and order, and their respective relations to sub-systems. Thus, upon generating the complete design, it is possible to distinguish two initial approaches: by presenting alternative solutions to new products and/or by looking for faults in existing products. In a new product, there is the possibility of adding auxiliary tools during the design development, mainly at the concept generation stage, with creativity tools. By doing this, exploring alternative solutions makes innovation and the generation of patents easier. As for existing products, when there are faults in the design, the sequence of the divisions of functions makes the identification of the origin of the error easier. At this point, this research, of a philosophical and conceptual nature, suggests that the combination of both techniques of function deployment produces superior results since they enable an encompassing view of the design.

intrinsically related to functional basis. Once the Hot Air Popper requires little technical knowledge for functioning and operating, we decided to adopt this product as a didactic example to illustrate the proposed methodology.

First of all, it is necessary to define the overall function as described in Step 1. By studying the product and the user manual [8], the main objective of the Hot Air Popper is to "pop corn kernels". After that, the inputs and the outputs indicated by [18] were organized in "energy flow" and "material flow" as shown in figure 9.

The Step 2 connects the flows and the components in order to relate every subfunction to a component. Thus, the product components (pictured in figure 11) were inferred from the functional model adapted from [18] (illustrated in figure 10).

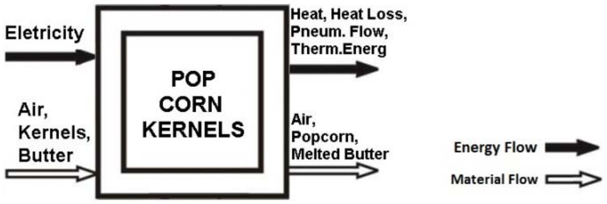

Fig. 9 : Hot Air Popper overall function black box

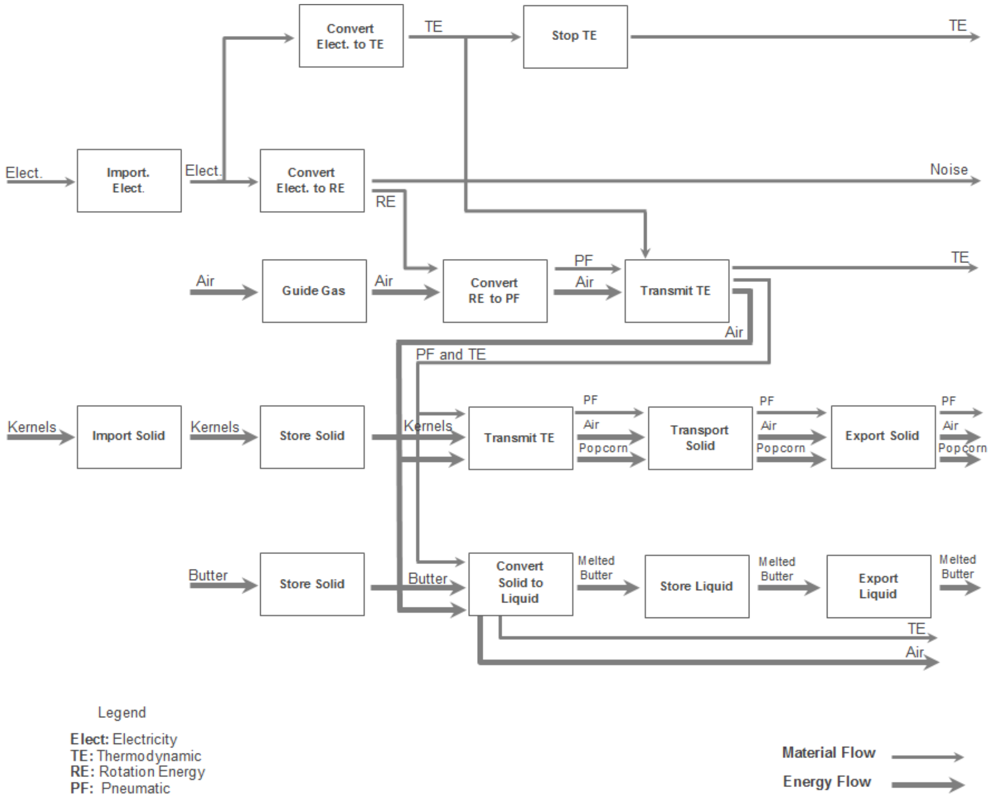

Fig. 10 : The Hot Air Popper functional deployment adapted from [18]

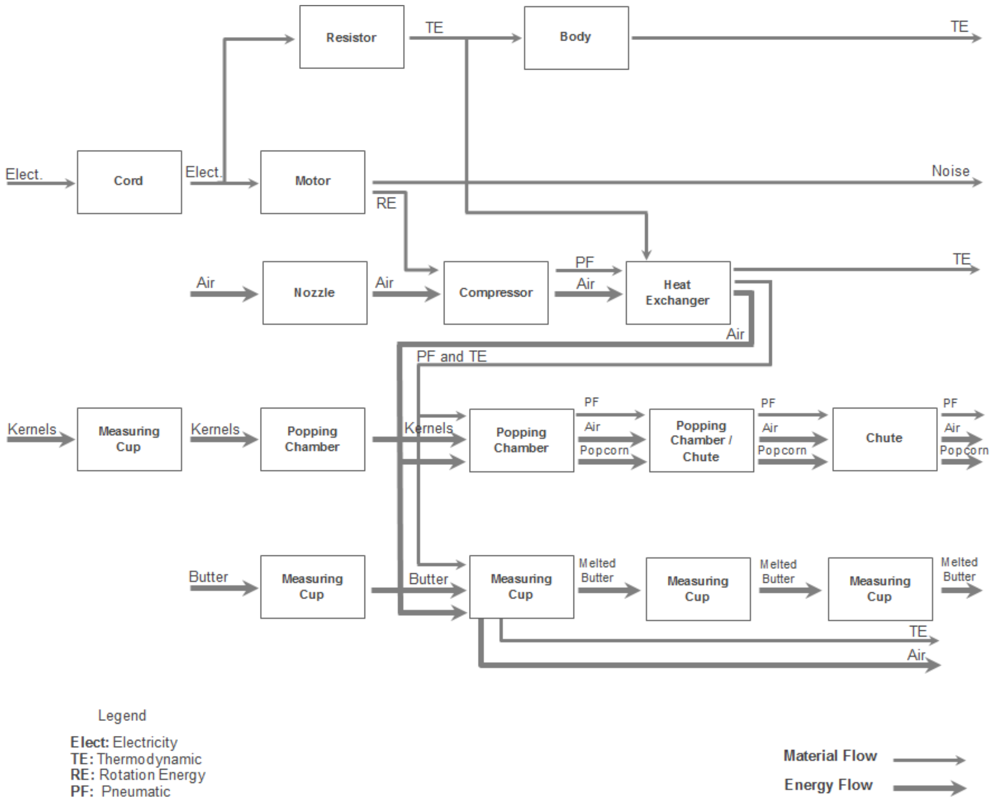

Fig. 11 : The Hot Air Popper components and the respective flows

The third step consists in the deployment of the primary functions based on the "why-how" approach, and the forth step is related to the deployment of the secondary functions. With these two steps, the FAST diagram is completed. To achieve the overall function – pop corn kernels – it is necessary to heat kernels by moving or storing kernels. With the hot air stream it is possible to move kernels, and in the end the air is heated and pumped to form a circuit. The secondary functions are related to melt butter and remove the popcorn. Figure 12 shows the complete diagram.

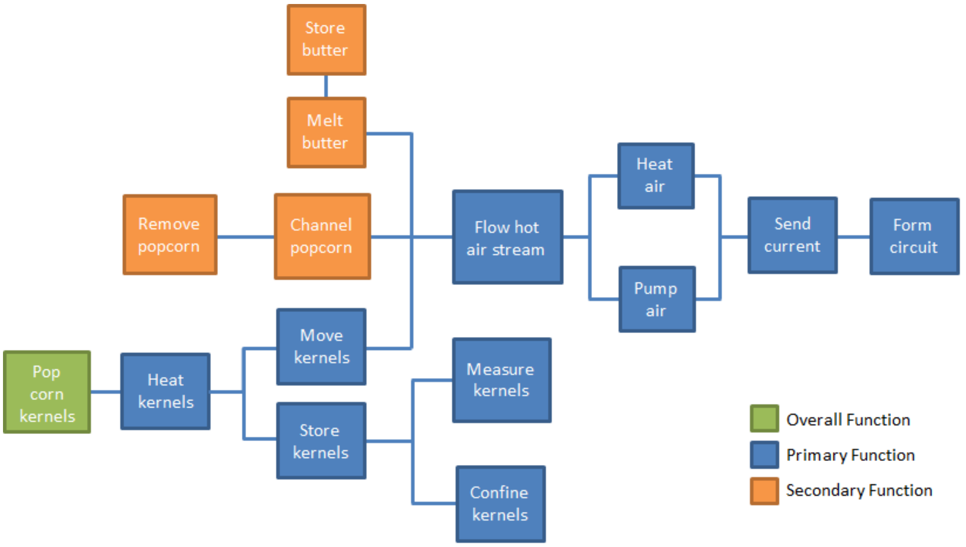

Fig. 12 : FAST diagram of the Hot Air Popper

The step 5 is the execution of the functional deployment according to [16]. As mentioned before, in this example this step is based on the deployment proposed by [18]. Finally, step 6 is the result of the superposition of the function tree and the function structure. It is possible to verify the correlation between the FAST diagram and the Pahl and Beitz functional deployment in figure 13.

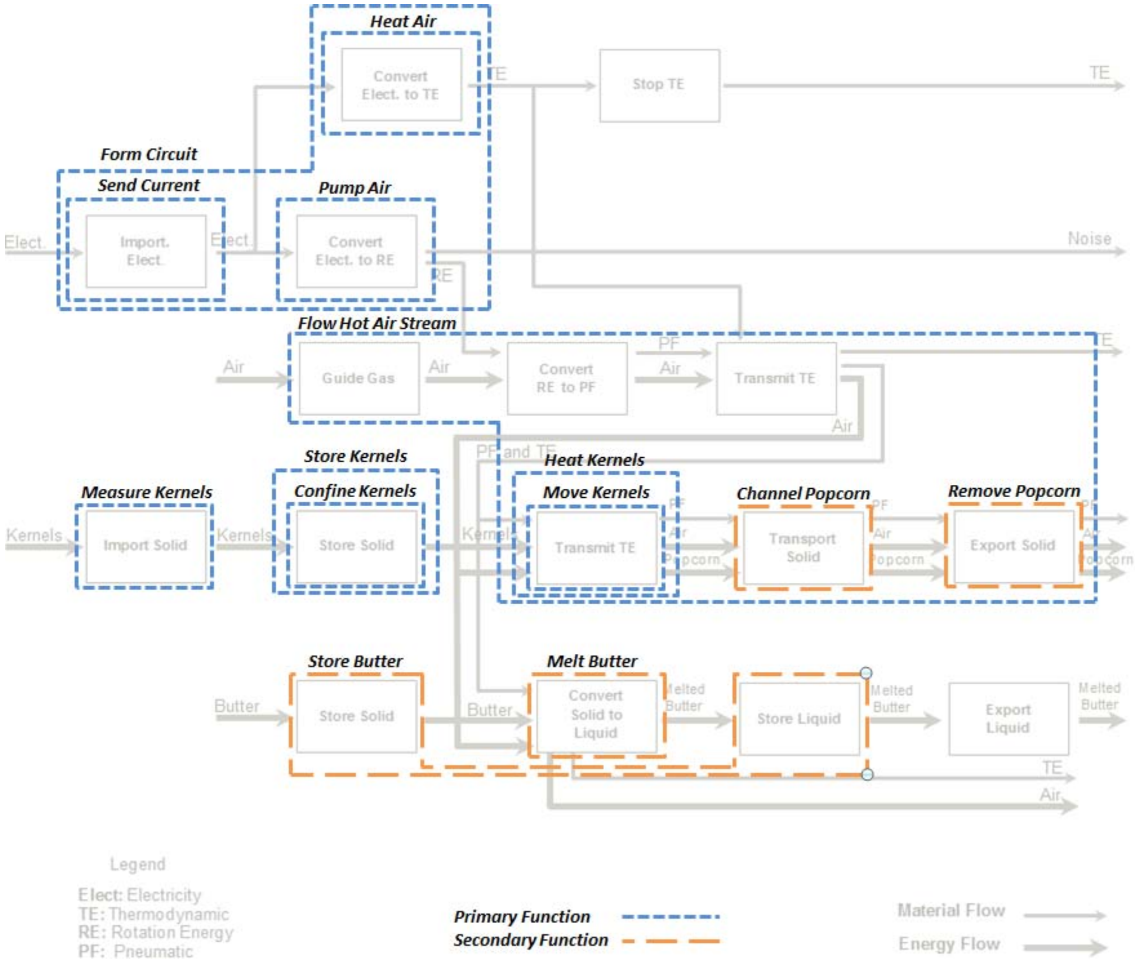

Fig. 13 : The function structure and function tree merge

This example presents a general view of how the proposed methodology correlates the functional deployments and the components. It enhances the design of products focused on the excellence of one characteristic (e.g. quality, manufacturing, cost, sustainability, etc.) because it supports the addition and/or substitution of functions. For example, in a future sustainable version of this product, a FAST function “recover heat loss” in figure 13 would be correlated to the FAST function “form circuit” and/or “heat air”. Automatically a Pahl and Beitz function “convert heat loss to electricity” would be added to the function structure, and finally a component that executes this function would be found, e.g. Peltier cell.

In Axiomatic Design the ideal product is decoupled, which means that every single part of it performs only one function [12]. The proposed methodology makes explicit the functional couplings in one single component. For example, by comparing figure 11 with figure 13, the popping chamber performs the functions “move kernel”, “heat kernels” and “flow hot air stream”; and the measuring cup executes “measure kernels”, “store butter” and “melt butter”. If it is necessary, the design team can optimize the butter melting by designing a specialized butter melting component, decoupling this function from the measuring cup. Thus, at the same time that the proposed methodology boosts the identification of couplings, it also supports the insertion of decoupling components.

During the execution of the proposed methodology, it is possible to notice some FAST functions with no correlation with Pahl and Beitz functions or vice versa. In figure 13, for example, the Pahl and Beitz functions “stop TE”, and “exportliquid” do not have a correlated FAST functions. Two hypotheses can be drawn: (a) there could be redundant or missing functions in one of the functional deployments; (b) there could be irrelevant functions in one of the functional deployments.

Finally, it is possible to link one component exclusively to primary functions, exclusively to secondary functions or both types of functions. For example, the compressor executes only a primary function (“flow hot air stream”), while the component “chute” executes one primary function (“flow hot air stream”) and two secondary functions (“channel popcorn” and “remove popcorn”). The design team can decide on splitting the components to execute exclusively primary or secondary functions, or on aggregating both types of function in one component depending on the value engineering.

VI. Concluding Remarks and Future Research

The theoretical basis allowed an analysis of the definition of the term function within the scope of design methodology. By doing that, a consensus among the several authors there were analyzed was noticed, in the semantic structure of a function based on the use of a verb and a noun. Nevertheless, these very same authors disagree over the categorization of function into hierarchical levels and purpose, and, mainly, when they transpose functions to the stages of functional analysis and function deployment. Upon dealing with tools that aim at both functional study and the classification of each function, it is possible to notice that there are conflicts regarding description and practical application stemming from the lack of clarity of the base terms. This context indicates that the study on the topic is pertinent, since it is necessary to fill in the gap left by both the definition of function and the methodology that approaches functional analysis. Therefore, the methodology proposed in this research aims at the functional study based on a need to form a representation that takes into consideration, at the same time, primary functions, secondary functions, sub-functions, and sub-systems. Considering that the proposal allows the function deployment of an Overall Function (OF), followed by the determination of Primary Functions (PF) and/or Secondary Functions (SF), divisions into Primary Sub-functions (PSF) and/or Secondary Sub-Functions (SSF) that, related to Sub-systems (SS), fulfill the Overall Function (OF), it is possible to approach alternative solutions and/or identify faults. The didactic example illustrates advantages of using the proposed methodology. The correlation between FAST functions and Pahl and Beitz functions is deeply explored, emphasizing the connection between both types of function and the product components. It allows the identification of couplings and the insertion of decoupling components. If there is one type of function with no connection, this function can be considered redundant or irrelevant or there are missing functions in the functional deployments. Thus, the proposed methodology indicates that the combination between FAST and Pahl and Beitz deployment results in a more comprehensive functional analysis by connecting function trees, function structures and components. In future researches the proposed methodology will be implemented by a multidisciplinary team on different areas of expertise such as hybrid vehicular dynamics and artisanal braiding in order to validate the procedure and contrast results.

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Area Optimized Low Latency Karatsuba of man Multiplier Variant for Embedded ECC

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Abstract- Due to resource constrains, implementation of secure protocols for securing embedded systems has become a challenging task. System designers are advised to design and install area efficient versions of existing, proven security protocols. System designers are finding ways and means to compress existing security protocols without compromising security and without tampering with basic security structure of algorithm. Modular multiplication, point multiplication, point doubling are few critical activities to be carried out in ECC algorithm. By optimizing Modular Multiplier, area efficiency in ECC algorithm can be achieved. In this paper, we propose Area optimized and low latency multiplier that implements the efficient KOA algorithm in altogether novel style to be used in ECC architecture. The proposed algorithm uses a novel technique of splitting input operands based on exponent's parity and it eventually helps in reducing FPGA footprint and offers low latency by avoiding overlapping, prime concern for any embedded system. The complete modular multiplier and the crypto processor module is synthesized and simulated using Xilinx ISE Design suite 14.4 software. We have investigated area occupancy of proposed multiplier and crypto processor and concluded that proposed scheme occupies relatively reduced percentage area of FPGA as compared to the one using traditional KOA multiplier.

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Sunil Devidas Bobade [α] & Dr.Vijay R. Mankar [σ]

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I. Introduction

Integrating security protocols in embedded systems is not an easy proposition. Embedded system designers have so far failed to install required levels of security in embedded systems, due to unusual design constraints like storage limitation, restricted processor performance and easy power drain in embedded devices. Regular cryptography algorithms are not suitable for Embedded systems due to wide footprint.

Due to resource constrains in the design and implementation of secure protocols, system designers are well advised to use area efficient versions of existing, proven security protocols, rather than developing their own protocols or implementations. This call for refined, area and space optimized; easy to deploy versions of original cryptography algorithms tailor made for resource constrained Embedded system.

Of the available choices, AES is the most powerful, most secured encryption algorithm with a key size ranging from 128 to 256. RSA is another well established and most preferred public key cryptography algorithm. To provide security equivalent to AES, RSA public-key sizes would have to range between 3,072 and 15,000 bits long, too big for embedded implementation. One appealing solution to the key size problem is the promising family of asymmetric algorithms known as Elliptic Curve Cryptography, or ECC.

Victor Miller and Neal Koblitz proposed the concept of elliptic curve cryptography in the mid of 1980's as an advancement in public key cryptographic systems such as DSA and RSA. The main advantage of ECC is the usage of shorter key helping compact implementations, resulting in faster cryptographic operations, running on smaller chips or more compact software. For hardware-based implementations of security functions, the benefits of ECC are more in comparison to RSA and AES. Optimized ECC chip designs have been designed and are as much as 37 times faster than its software counterparts. ECC offers other advantages of small software footprint, low hardware implementation costs, low bandwidth requirements, high device performance. Due to these many advantages of ECC a number of hardware implementations have been proposed, and included in many standards such as IEEE 1363and NIST.

Modular multiplication is the most primitive and critical operation in ECC. The design of Finite field multipliers is the complex design issue in the implementation of the ECC processor. A number of multipliers with different area and time complexity are reported in the available literatures. The Karatsuba Ofman algorithm is agreed upon as a most efficient multiplication algorithm and is widely adopted in VLSI implementation. Here input operands are processed as the "most significant half" and the "least significant half".

In proposed multiplier, instead of splitting input operands into the "most significant half" and the "least significant half", our method split operands according to the parity of multiplicands's exponent. Both the space and time complexities of the resulting multiplier are found to be much better than that of traditional multiplier. Here we have concentrated and investigated on area optimization. This is a significant achievement if we intend to use this multiplier in FPGA implementation of elliptical curve cryptography for embedded systems.

The basic step of Karatsuba Ofman's algorithm is a formula that computes the product of two large

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numbers using three multiplications of smaller numbers, each with about half as many digits as operands, plus some additions and digit shifts. Karatsuba Ofman method of multiplication is a faster way of multiplying two integers of length n. For the first step of the algorithm, it initially requires the breaking of multi digit integers into parts. These parts can then be used in three multiplications to produce a solution.

The Karatsuba algorithm is an effective multiplication algorithm. It diminishes the multiplication of two ***n*** -digit numbers to at most single-digit multiplications in general (and exactly when n is a power of 2). It is along these lines quicker than the traditional algorithms, which requires n^2 single-digit products. If n = 2^{10} = 1024, in particular, the precise counts are 3^{10} = 59,049 and $(2^{10})^2$ = 1,048,576, respectively. Here the operands α and β can be divided into two equal-size parts α_L and α_H , β_L and β_H respectively, which represent the $l/2$ higher and lower order bits of α and β . We can split them in two parts as follows:

$$\alpha(x)=\sum_{i=0}^{l-1}a_i x^i=\sum_{i=\frac{l}{2}}^{l-1}a_i x^i+\sum_{i=0}^{\frac{l}{2}-1}a_i x^i$$

$$=\alpha^{\frac{l}{2}}\sum_{i=0}^{\frac{l}{2}-1}a_{i+\frac{l}{2}}x^i+\sum_{i=0}^{\frac{l}{2}-1}a_i x^i$$

$$\alpha(x)=x^{\frac{l}{2}}\alpha_H+\alpha_L$$

Likewise,

$$\beta(x)=x^{\frac{l}{2}}\beta_H+\beta_L$$

The product $\gamma(x)*$ can be computed as

$$\gamma(x)*=\alpha(x).\beta(x)$$

By using above equation output can be represented as,

$$\gamma(x)*=\alpha_L\beta_L+\alpha_H\beta_H x^l+(\alpha_H\beta_L+\alpha_L\beta_H)x^{\frac{l}{2}}$$

To further improve the computation of the product $\gamma(x)*$ equation can be modified as,

$$\gamma(x)*=\alpha_L\beta_L+\alpha_H\beta_H x^l+(\alpha_L\beta_L+\alpha_H\beta_H+(\alpha_H+\beta_L)(\beta_H+\beta_L)x^{\frac{l}{2}}$$

II. Related Work

Several modular multiplication algorithms have been proposed. Of them all, Karatsuba- Ofman algorithm, KOA is widely used for performing modular arithmatic. In [1] a variant of Karatsuba multiplier of the type GF $((2^n)^8$ is presented and is highly area efficient. Kimmo U. Järvinen *et.al* [2] adopted an efficient implementation of point multiplication on Koblitz curves and was designed for extremely-constrained, secure applications. In that approach a new technique was introduced for point addition which required fewer registers and small processor. In [3] Hossein Mahdizadeh and Massoud Masoumi built elliptic curve cryptographic processor by organizing multipliers in parallel.

In [4], hybrid multiplier was proposed that intelligently switches between two variants of multiplier depending on the size of multiplicands. The Karatsuba multiplier is efficient algorithm ensuring fewer LUTs and stable number of Flip-flops for the smaller bit multiplications, while the systolic variant ensures fewer LUTs count for the bigger size multiplicands. This hybrid multiplier does the initial recursion using the systolic algorithm while final small sized multiplications are accomplished using the Karatsuba algorithm. Area analysis report suggested that by using a hybrid multiplier instead of just traditional Karatsuba Multiplier, eventually helps in reducing FPGA footprint. This hybrid multiplier exhibits a savior of 7.56 % in terms of Flip flop slices. Involves 52 % fewer LUTs and utilizes 47% fewer slices as compared to traditional Karatsuba multiplier for 256 bit multiplication.

In [5], FPGA based area efficient ECC processor was built using Digit multiplier. Instead of processing vector (polynomial) bit by bit or parallelly, operands are process in 16-bit word format. This Modular multiplier exhibits a savior of 23.88% in terms of Flip flop slices. Proposed Multiplier involves 62 % fewer LUTs and utilizes 59% fewer slices as compared to traditional Karatsuba multiplier for 256 bit multiplication. Further reduction was achieved in ECC processor by employing efficient double point multiplication algorithm.

Area and speed efficient 163 bit Scalar multiplier with improved area and speed was designed by Sujoy Sinha Roy *et.al* [6]. Scalar multiplication was performed on Xilinx Virtex V platforms over GF (2^{163}). The implementation used a novel three stage pipelined bit-parallel Karatsuba multiplier with subquadratic complexity. Scalar multiplication algorithm, optimized field primitives, balanced pipeline stages, and enhanced scheduling of point arithmetic all contributed to a high-speed architecture with a significantly small area Hybrid binary-ternary number system for elliptic curve cryptosystems was designed by Jithra Adikari *et.al* [7]. In their newly designed system three novel algorithms for both single and double scalar multiplication were implemented. The first algorithm is w-HBTF and the other two algorithms, namely, HBTJF and RHBTJF. The output results showed that hybrid algorithms are almost always faster than classical w-NAF methods or JSF. Kazuo Sakiyama et.al [8] implemented modular multiplication algorithm that integrates three different existing algorithms, based on Barrett reduction and

Montgomery reduction. This modular multiplier is highly speed efficient.

III. Proposed Area Optimized Low Latency Multiplier

Proposed multiplier is based on Karatsuba Ofman Algorithm. Two operands A and B in KOA can be represented in polynomial format as

$$\mathrm{A} = \sum_{i=0}^{n-1} \mathrm{a_i X^i}$$

$$= X^m \sum_{i=0}^{m-1} a_{m+i} X^i + \sum_{i=0}^{m-1} a_i X^i$$

$$= \mathrm{X^m A_H + A_L}$$

Similarly,

$$\mathrm{B} = \sum_{i=0}^{n-1} \mathrm{b_i X^i}$$

$$= X^m \sum_{i=0}^{m-1} b_{m+i} X^i + \sum_{i=0}^{m-1} b_i X^i$$

$$= \mathrm{X^m B_H + B_L}$$

Where

$$\mathrm{A_H} = \sum_{i=0}^{m-1} a_{m+i} X^i \text{ and } \mathrm{A_L} = \sum_{i=0}^{m-1} a_i X^i$$

$$\mathrm{B_H} = \sum_{i=0}^{m-1} b_{m+i} X^i \text{ and } \mathrm{B_L} = \sum_{i=0}^{m-1} b_i X^i$$

The product of A and B can be written as

$$\mathrm{AB = A_H B_H X^{2m} + \{[(A_H + A_L)(B_H + B_L)]}$$

$$\mathrm{- [A_H B_H + A_L B_L]\}Xm + A_L B_L}$$

In Modulo 2 domain, addition and subtraction operation can be accomplished using XOR Gate and product using AND gate. Total gates involved for implementing above expression will be five AND gates for accomplishing five multiplication activities and four XOR gates for performing modulo 2 addition. Further, it is a three level realization, as input operand has to pass through maximum of three levels of XOR gate before reaching output line because of overlapping. Therefore, total XOR gate delay for implementing the above expression will be $3T_D$ besides the cost of the recursive computation of the three partial products. Thus basic KOA multiplier utilizes five AND gates and four XOR gates to accomplish the basic multiplication activity.

Instead of splitting input operands into the "most significant half" and the "least significant half", the method split operands according to the parity of X's exponent.

Accordingly, Operands A and B may be rewritten as

$$\mathrm{A} = \sum_{i=0}^{n-1} \mathrm{a_i X^i}$$

$$= \sum_{i=0}^{m-1} a_{2i} X^{2i} + \sum_{i=0}^{m-1} a_{2i+1} X^{2i+1}$$

$$= \sum_{i=0}^{m-1} a_{2i} X^{2i} + X \sum_{i=0}^{m-1} a_{2i+1} X^{2i}$$

Similarly,

$$\mathrm{B} = \sum_{i=0}^{n-1} \mathrm{b_i X^i}$$

$$= \sum_{i=0}^{m-1} b_{2i} X^{2i} + \sum_{i=0}^{m-1} b_{2i+1} X^{2i+1}$$

$$= \sum_{i=0}^{m-1} b_{2i} X^{2i} + X \sum_{i=0}^{m-1} b_{2i+1} X^{2i}$$

Now let us define

$$\mathrm{A_E} = \sum_{i=0}^{m-1} a_{2i} X^{2i} \qquad \mathrm{A_O} = \sum_{i=0}^{m-1} a_{2i+1} X^{2i}$$

$$\mathrm{B_E} = \sum_{i=0}^{m-1} b_{2i} X^{2i} \qquad \mathrm{B_O} = \sum_{i=0}^{m-1} b_{2i+1} X^{2i}$$

Let i=2 and X^2=Y,

Then product AB can be written as

$$\mathrm{AB = (A_E(y) + XA_O(y))\ (B_E(y) + XB_O(y)) = \{A_E(y)B_E(y) + X^2A_O(y)B_O(y)\} + X\{A_E(y)B_O(y) + A_O(y)B_E(y))\}}$$

Applying KOA formula to above expression,

$$\mathrm{= \{[A_E(y)B_E(y) + YA_O(y)B_O(y)]\} + X\{[(A_E(y) + A_O(y))(B_E(y) + B_O(y))] - [A_E(y)B_E(y) + A_O(y)B_O(y)]\}}$$

In VLSI implementation of above expression multiplying a polynomial by x or y = x^2 is equivalent to shifting its coefficients left, and no gate is required. For implementing this revised expression four AND gates and three XOR gates are required. The expressions in the three square brackets can be computed concurrently, and these addition operations require one XOR gate delay $1T_D$. We conclude that computing product AB needs only a total delay of $2T_D$ besides the cost of the recursive computation of the three partial products.

Compared to the $3T_D$ gate delays required in traditional formula, one XOR gate delay $1T_D$ is saved for each recursive iteration. Thus compared to the four EXOR gates delays required in traditional formula, one XOR gate and also one AND gate is saved for each recursive iteration, which is a significant achievement considering embedded systems are highly resource constrained. . Thus this variant of KOA multiplier utilizes four AND gates and three XOR gates to accomplish the basic multiplication activity.

Table 1 : Resource Utilization Comparison of Two Multipliers

	Karatsuba Ofman Multiplier				Proposed New Version Multiplier			
Multiplicand Size	Flip flops	LUTs	Occupied Slices	IOBs	Flip flops	LUTs	Occupied Slices	IOBs
2 bit	17	25	16	9	15	16	13	9
4 bit	32	75	43	17	21	31	19	13
8 bit	46	150	79	33	29	57	32	21
16 bit	54	162	87	65	45	78	42	37
32 bit	102	315	168	129	81	142	78	69
64 bit	266	665	411	257	145	270	143	133
128 bit	646	1782	1000	513	273	526	272	261
256 bit	1118	13761	7008	913	530	1038	529	517

From the above basic concept, it is observed that by splitting the operand polynomials, based on the parity, results in reduction of hardware (fewer AND and XOR gates) and latency time (fewer levels due to little overlapping). By extending this very concept of splitting the operands based on parity to FPGA implementation, we have explored and implemented FPGA based finite field multiplier and compared FPGA footprint with that of traditional KOA multiplier. Also we have incorporated the proposed multiplier in ECC processor and investigated its impact on the footprint of entire processor. In this paper, we have only concentrated on area occupancy of proposed multiplier, its impact on processor footprint but haven't investigated quantum of latency improvement, which forms the future scope of investigation.

IV. Results and Discussion

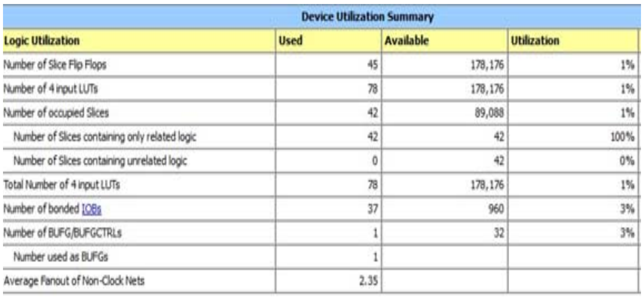
In this section, we focus on the FPGA implementation of the proposed multiplier. The proposed architecture is coded in verilog HDL and is synthesized using Xilinx ISE version 14.4 design software and is implemented on Xilinx Virtex-4 xc4vlx200ff1513 FPGA. The RTL schematic for the proposed Finite Field multiplier is shown in figure 1.

Fig. 1 : RTL Diagram of Proposed multiplier

a) *Area Report of Proposed Multiplier*

Since the area of the complete processor mainly depends on the incorporated GF multiplier, most of the slices in the target device are utilized by it. From table 2, for 16 bit multiplicands, proposed modular Multiplier needs 42 slices out of 89,088 available slices in the target device. Among the 178,176 available four input LUTs only 78 are used. The multiplier also needs only 45 out of 178,176 Flip Flops.

Table 2 : Resource Utilization By Multiplier For L=16



Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	45	178,176	1%
Number of 4 input LUTs	78	178,176	1%
Number of occupied Slices	42	89,088	1%
Number of Slices containing only related logic	42	42	100%
Number of Slices containing unrelated logic	0	42	0%
Total Number of 4 input LUTs	78	178,176	1%
Number of bonded IOBs	37	960	3%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	2.35		

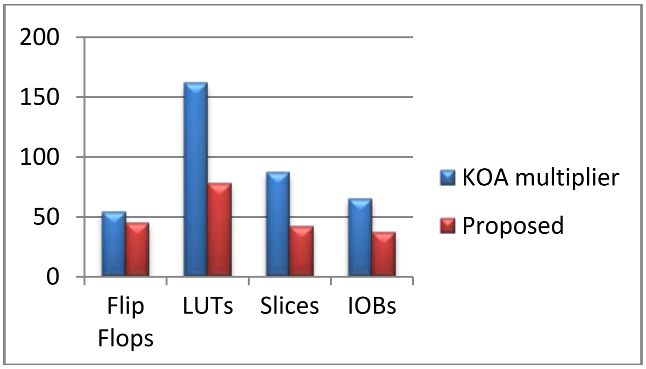
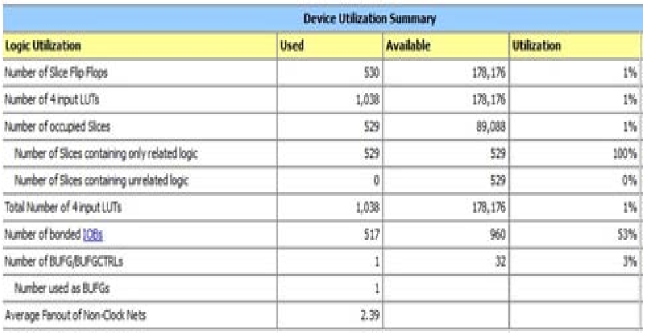


Fig. 2 : Resource utilization comparison of two KOA variants for L=16

A bar chart representation shown in figure 2 compares the resource utilization of Proposed multiplier with traditional Karatsuba Ofman Multiplier for L =16. Thus proposed multiplier exhibits a savior of 20 % in terms of Flip flop slices. Proposed Multiplier involves 53 % fewer LUTs and utilizes51.72% fewer slices as compared to traditional Karatsuba Ofman multiplier for 16 bit multiplication. This helps in bringing down the footprint of modular multiplier on FPGA while building cryptography schemes.

Table 3 : Resource Utilization By Multiplier For L=256



Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	530	178,176	1%
Number of 4 input LUTs	1,038	178,176	1%
Number of occupied Slices	529	89,088	1%
Number of Slices containing only related logic	529	529	100%
Number of Slices containing unrelated logic	0	529	0%
Total Number of 4 input LUTs	1,038	178,176	1%
Number of bonded IOBs	517	960	53%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	2.39		

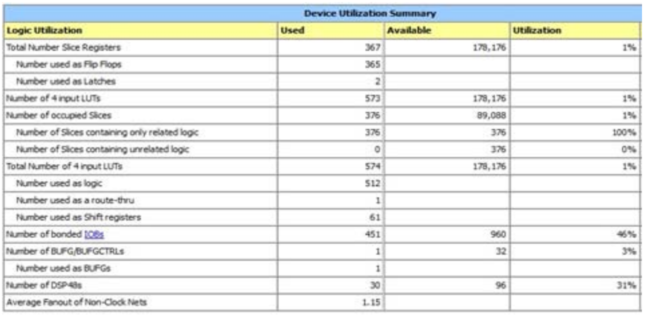
This saviour is more significant for L= 256. Proposed multiplier exhibits a savior of 52.49 % in terms of Flip flop slices. Proposed Multiplier involves 92 % fewer LUTs and utilizes 92% fewer slices as compared to traditional Karatsuba multiplier for 256 bit multiplication as indicated in table 3.

b) Area Report of Crypto Processor

The ECC processor implementation uses a double point multiplication algorithm proposed in [9]. We have adapted revised and area optimized version of Montgomery's PRAC algorithm [10]. The area comparision is carried out for crypto processors using proposed multiplier the one proposed in [11].

Table 4 below shows device utilization summary of Crypto processor, when the above proposed multiplier is employed for performing modular multiplications. Processor needs 376 slices out of 89,088 available slices in the target device. Among the 178,176 available four input LUTs only 573 are used. The multiplier also needs only 451 out of 178,176 Flip Flops.

Table 4 : Resource Utilization by Ecc Processor



Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Total Number Slice Registers	367	178,176	1%
Number used as Flip Flops	365		
Number used as Latches	2		
Number of 4 input LUTs	573	178,176	1%
Number of occupied Slices	376	89,088	1%
Number of Slices containing only related logic	376	376	100%
Number of Slices containing unrelated logic	0	376	0%
Total Number of 4 input LUTs	574	178,176	1%
Number used as logic	512		
Number used as a route-thru	1		
Number used as Shift registers	61		
Number of bonded IOBs	451	960	46%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Number of DSP48s	30	96	31%
Average Fanout of Non-Clock Nets	1.15		

We have investigated area occupancy of cryptoprocessr built using proposed variant of Karatsuba Ofman multiplier and compared it with similar ECC work. Bar chart representation shown in figure 3 compares the resources utilized by proposed ECC with a similar work [11]. The comparison of implemented ECC processor employing proposed modular multiplier and the crypto Processor using traditional Karatsuba Multiplier with respect to the area occupied (Slice registers, Slices, LUTs and IOBs) is tabulated in Table 5 and compared in figure 3. Proposed implementation utilize about 23.93 % reduced slices and 62.65 % fewer LUTs. This is a significant achievement as we intend to put this ECC hardware for providing security services in embedded system which is known to be highly resources thirsty.

Table 5 : Resource Utilization Comparison of Two Ecc Processors

Work	/	Slices	LUTs	IOBs
[11]	193	466	932	932
Proposed	233	376	573	451

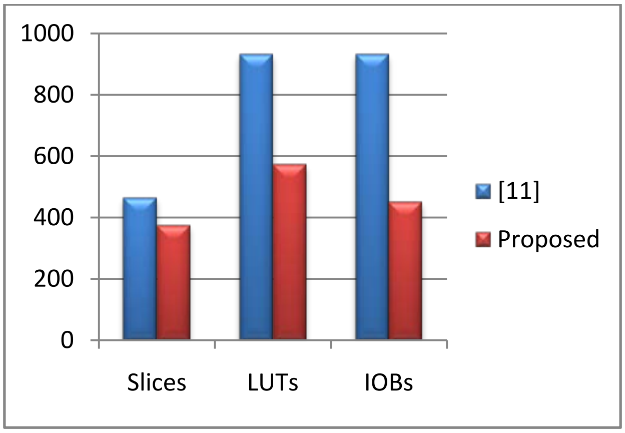


Fig. 3 : Resource utilization comparison of ECC processor using proposed multiplier and [11]

V. Conclusion

We have proposed a novel method to implement the modular multiplier for performing critical multiplication activities in ECC processor. Area occupancy of the resulting multiplier is found to be far superior than that of traditional KOA multiplier. This contributes in bringing down the footprint of entire ECC process. While injecting this modification, nowhere we have tampered with the basic flow and structure of basic ECC protocol. Just by processing the operands in different style, we have achieved area optimization of complete ECC protocol and made it suitable for embedded system with no compromise on security of ECC algorithm.

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Security in Untrusted Updated Environments

By Jahnavi Terva, Jaya Krishna K & K. Kondaiah
K L University, India

Abstract- At present days, technology growth was rapid and its use is very often. So the attacks were concentrated on the user systems mainly by using the network applications. Bugs in the application of a network can ruin the applications in a system that are running. When the user is in the use of internet or e-commerce sites, etc.., the applications will be considered that they are in an unsafe environment. Providing security to the network applications like web servers, mails, etc... Is very difficult because they are usually very big applications to make them free from bugs.

Now this paper describes how to provide security to the network applications which are in unsafe environment. This idea describes that all the applications were wrapped together for the security purpose and there will be no use to rewrite the network applications.

Keywords: internet security, network applications, secure environment [2], sandbox technique.

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Security in Untrusted Updated Environments

Jahnavi Terva [α], Jaya Krishna [σ] K & K. Kondaiah [ρ]

Abstract- At present days, technology growth was rapid and its use is very often. So the attacks were concentrated on the user systems mainly by using the network applications. Bugs in the application of a network can ruin the applications in a system that are running. When the user is in the use of internet or e-commerce sites, etc.., the applications will be considered that they are in an unsafe environment. Providing security to the network applications like web servers, mails, etc... Is very difficult because they are usually very big applications to make them free from bugs.

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I. Introduction

Because of the easy access of the Internet throughout the globe, many various applications can be runned on the hardware platforms, which gives any opportunities in the commercial field. Developing an application is also an issue for providing the security from the internal attacks of users system. With a correct Securitas guard, the attacks can be detected. Different security solutions should be provided to the different attacks from the network. Many applications which are developed cannot provide a guarantee that can give total security. To develop a bug free application is very complex for the network applications which can result in a security issue.

In this paper, CMW which mean Common Mode Workstation Operating system with a B1-level grade is used to secure the applications from the unsafe helper environments. In this rewriting will not be done for an existing application as the applications will be wrapped and can be upgraded safely and securely.

II. Background

There are many protocols for the network security like SHTTP, SHHP, TLS, BITCOIN Protocol, etc… to give some protection where the communication is done at the two Ends of a receiver and sender. Unwanted connections can be kept out by using the Firewall [3]. If the bugs which are hidden in the server side is connected with the data of a user that may lead to the leakage of data from user system. Because of the bugs that are present in the network applications, either internal attacks can be done to sensitive data or leakage of data will be done. Providing security to a network application is almost impossible. While providing security, rewriting of the application will be done which also leads to a security issue. Mainly while providing security to the social networking sites is a complex issue.

While opening these networking sites the data transfer should not be done from receiver to the sender. All the applications should be developed keeping the security issue in the mind.

III. Existing Techniques

The traditional technique used is called sandboxing which can prevent the vulnerable applications running in a confined environment. Protecting the data from hackers and unwanted network applications from the break ins. There are many possibilities to the hacker to develop many privileged applications to break the security policies. Let us consider an example TIS96 which depends on the physically distinguish hardware which gives us information separation. Another example GWT96 which depends on operating systems. There is a user and security check at the user level. There is still the possibilities that the hacker can make use of compromised privileged applications to alter the security policies and further his attacks.

IV. Our Approach for Security

HP-UX[1] CMW can be used to combine all the untrusted network applications. In this approach we are going to design an Operating systems [5] that facilitates a group of fine grained administrative security assigns and operations to handle these assigns. Security checks should be done at each level to the Operating System in which process are running simultaneously so that it can guarantee maximum protection. Because of these features, it will be able to distinguish the network application format from security format, to provide a general platform for combining the existing untrusted dumb applications for security. For explaining how to use CMW in sandbox for untrusted applications, for serving as case studies we took two typical examples. One of those examples is the HP's Presidium Virtual Vault, which prevents the unauthorized access unauthorized modification of the data in the server by wrapping the Web server. Other example is Trusted Send mail Proxy which was developed in HP Labs[4],

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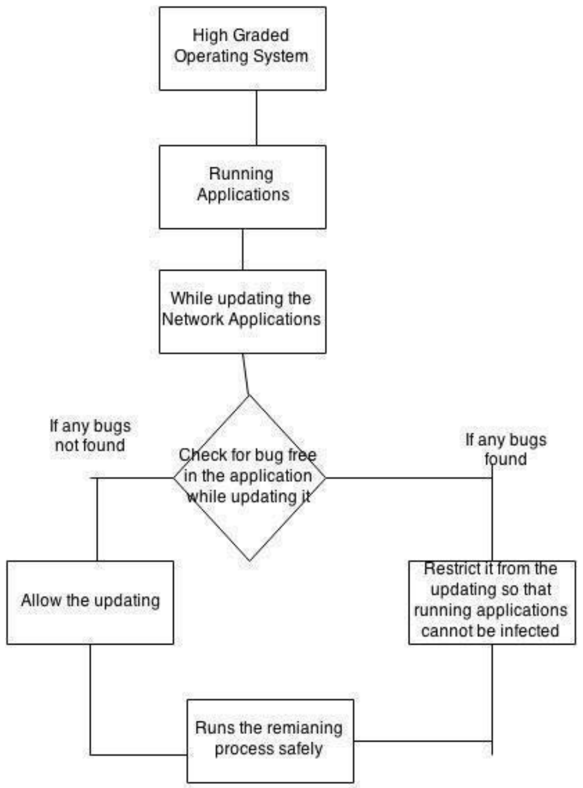
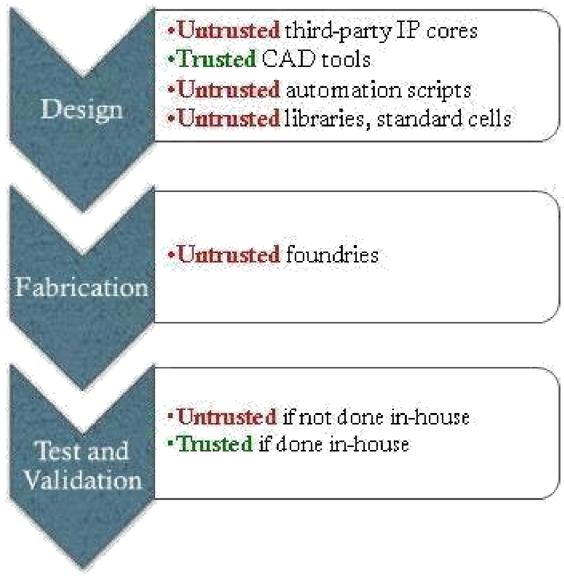
Bristol and this prevents highly privileged but vulnerable send mail that are running on the system without causing any fatal damages to the users system.

The objective of the work is to provide the network application services safely by combining untrusted applications and to have a view on the advantages of introducing CMW to solve the security issues in the commercial field.

V. Flow Chart for the Approach


High Graded Operating System
Running Applications
While updating the Network Applications
Check for bug free in the application while updating it
If any bugs not found
If any bugs found
Allow the updating
Restrict it from the updating so that running applications cannot be infected
Runs the remiang process safely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•Trusted CAD tools
•Untrusted automation scripts
•Untrusted libraries, standard cells
Fabrication
•Untrusted foundries
Test and Validation
•Untrusted if not done in-house
•Trusted if done in-house

Fig. 1 : Example of tokens to be generated for security purpose to the network application

VI. Working of the Idea to Provide Security to Application

a) Finding an restricted process

The parent and child privileges are given to the applications which are to be updated so that safe transfer of the information can be done. Let us consider an example in which a child process cannot get access to the privileges of a parent process by inheriting, it can be restricted as inheritance is an automatic process. If it can get access from the parent process it can be given an token that it is an trusted application. So by this way we can find which process is to be restricted and which process is to be continued with security. If the child process which cannot gain access is allowed to continue further it leads to a serious issue for the internal attacks of the users system.

b) How CMWis used to combine the Untrusted Applications

As our objective is to prevent an third party gaining the access of user's system and to protect oneself from the untrusted vulnerable network applications. We use two typical network applications to wrap the application data i.e. by using the web server and send mail illustrating what is done to apply the methods to give security. A trusted mail is sent at the ending by illustrating what is done in the process.

VII. Security Analysis of the Network Application

Even if the data is broken by the bugs then the damage will be confined to only the compartment which is considered as system inside. It doesn't harm much because the data in the system inside of the operating systems cannot get access to the connections of the data which is provided from outside network.

VIII. Conclusion and Future Work

An operating system with highly grained administrative security management helps to meet many security policies while using the network applications and can protect us from an intruder accessing the gain root access of the data in a system of user. Security dumb applications can be easily found and can be issued an unsafe token to prevent access and is restricted. Depending on the various commercial applications security infrastructures should be modified according to that and should have possibility to extend the CMW for the application platform of that network.

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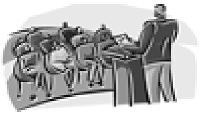

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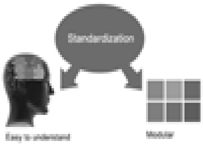

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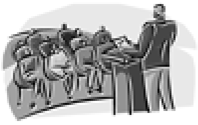

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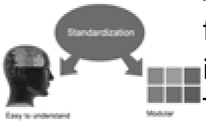

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- Recommendations for detailed papers will offer supplementary suggestions.

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- When you refer to information, differentiate data generated by your own studies from available information
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References	Complete and correct format, well organized	Beside the point, Incomplete	Wrong format and structuring

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