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Simulation and Analysis of Power Quality Improvement using Multilevel Unified Power Quality Conditioner

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Simulation and Analysis of Power Quality Improvement using Multilevel Unified Power Quality Conditioner

G. Annapurna [α] & G. Tulasiramdas [σ]

Abstract- Unified Power Quality Conditioner (UPQC) is an effective device to solve the power quality problems. The UPQC is a combination of series and shunt filters which simultaneously compensate load voltage and source current imperfections. This paper presents harmonic mitigation using three level Neutral Point Clamped inverter based Unified Power Quality Conditioner. The use of three level Neutral Point Clamped converters allows a better performance of equipment by reducing harmonics and the ripple of the generated oltages and currents. The performance of UPQC in the reduction of harmonics is evaluated when employed with Multi carrier based SPWM and three level novel SVPWM techniques. Simulation results based on MATLAB/SIMULINK are presented to verify the effective compensation of harmonics using the two different modulation techniques.

Keywords: active filters, neutral point clamped converters, total harmonic distortion, power quality, SVPWM.

I. Introduction

The increased use of non-linear loads deteriorate power system voltage and current waveforms as they inject harmonics into the system. This results in increased losses, lower efficiency, failure of equipment etc. in the power system. Apart from voltage and current harmonics, voltage sag, voltage swell, voltage outage also can lead to poor quality of power [1]. Harmonic compensation and voltage regulation have become more important as imbalance in the voltage and presence of harmonics have been serious issues. Hence, there is a great need to mitigate these power quality issues.

The introduction of advanced power electronics technology has led to the development of active power filters which are viable solution to these power quality problems[1,2].

The general arrangement of Unified power quality conditioner is shown in Fig.1. The main function of a UPQC is to compensate voltage and current harmonics.

The UPQC combines series and shunt active filters with a common dc link. The series active filter suppresses voltage distortions while the shunt filter cancels current distortions such that this combination allows simultaneous compensation of voltages and currents supplied to the sensitive load to see that they are sinusoidal and balanced.

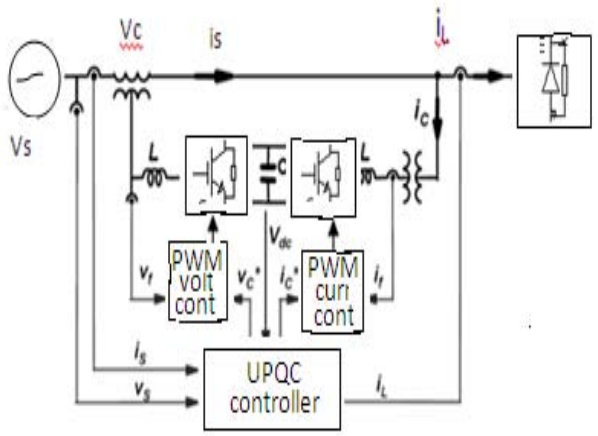

Fig.1 : General configuration of UPQC

Multilevel inverters play an important role in the reduction of harmonic content in the voltages and currents. The multilevel inverters can synthesize high output voltage from smaller voltage levels and thus the current ripples and voltage harmonics are reduced. The UPQC presented in this work consists of three level converter topology [3,4]. The performance of UPQC can be optimized because of reduction in the size of passive components and transformers [4].

II. The Upqc Controller

The UPQC controller is composed of PLL circuit, Reference Voltage Algorithm and Reference Current Algorithm [4,5,6].

The PLL circuit has the system voltages Vab and Vcb i.e (Vab =Vas – Vbs, Vcb = Vcs - Vbs) as inputs and the outputs are the signals Pll_a, Pll_b and Pll_c as shown in Fig.2.

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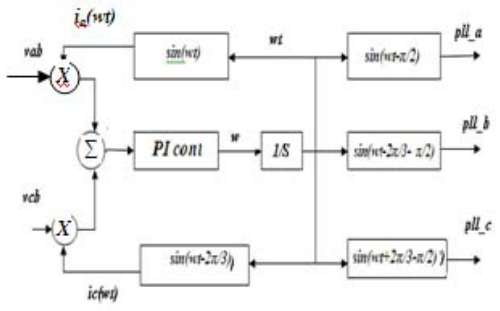

Fig. 2 : The synchronizing ciruit

The PLL circuit guarantees the load voltages and source currents to be balanced sinusoidal waveforms at fundamental frequency.

The reference current control strategy is shown in Fig.3. The reference currents algorithm control block determines six reference currents (i_{aref1},i_{bref1},i_{cref1}) and (i_{aref2},i_{bref2},i_{cref2}) by using the outputs of PLL (Pll-a,Pll-b,Pll-c) , the DC link voltages (V_{dc1},V_{dc2}) and the load currents (I_{al},I_{bl},I_{cl}) as inputs. The shunt active power filter will then synthesize the reference currents.

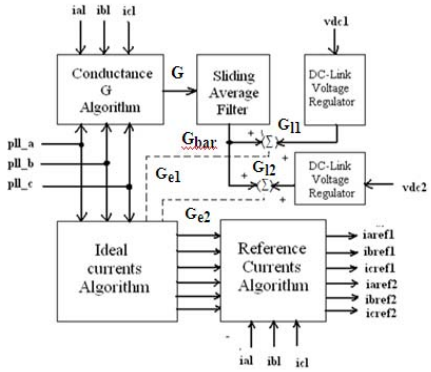

Fig. 3 : Reference current algorithm control strategy

The "reference voltage algorithm" shown in Fig.4 calculates, the reference voltages (V_{aref}, V_{bref}, V_{cref}) by using system input voltages (V_{as}, V_{bs}, V_{cs}) and PLL outputs(pll-a, pll-b, pll-c) that will be synthesized by the series power converter.

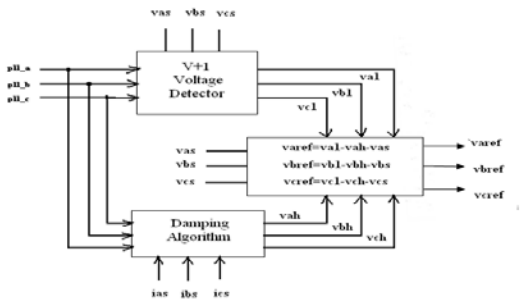

Fig. 4 : Reference voltage algorithm control strategy

III. Switching Strategy of Three Level Converters

In order to illustrate the switching control technique applied to the series and shunt active power converters, a basic three level NPC (Neutral Point Clamped) topology as shown in Fig. 5 is used [7,8].

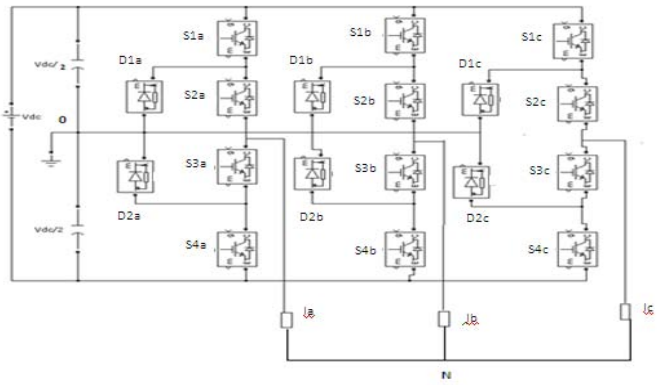

Fig. 5 : Three level Neutral point clamped converter

Each leg has four switching devices connected in series. As an example, phase "a" is considered to explain the behavior of the circuit.

The output of the inverter can take three voltage levels based on the switching states of the devices. The output Va is positive when switches S1a and S2a are ON, it is negative when S3a and S4a are turned ON, and it is '0' when switches S2a and S3a are ON. The switching states of the devices and the corresponding output voltages with respect to the dc mid-point are indicated in the following Table I.

The switching strategy of the series active filter is shown in Fig 6. In this technique, the reference signal is compared with measured signal, the error is amplified and processed by PWM generator to obtain V*a_PWM.* This signal is compared with two triangular waves of different limits having unit magnitude.

Table.I : Switching states and output voltages

SWITCHING STATES				OUTPUT VOLTAGE
S1a	S2a	S3a	S4a	Va
ON	ON	OFF	OFF	+Vdc/2
OFF	OFF	ON	ON	-Vdc/2
OFF	ON	ON	OFF	0

The switching control strategy of the shunt active converter is shown in Fig 7. This strategy compares the two reference signals Iaref1 and Iaref2 with measured currents, the errors are then amplified and processed by PWM generator to produce *I a1-pwm and I a2-pwm.* These signals are compared with two triangular trigger waves of different limits having unit magnitude.

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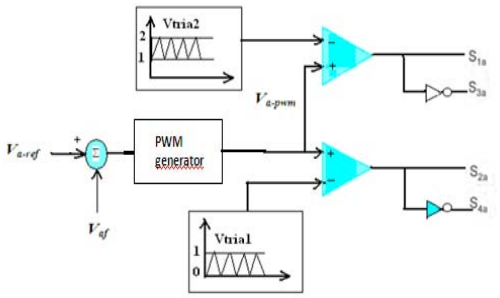

Fig. 6 : Series switching control strategy

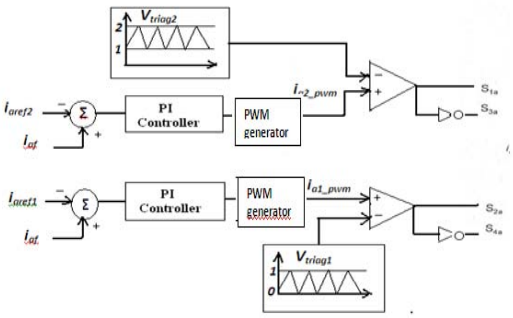

Fig.7 : Shunt switching control strategy

IV. Modulation Strategy

a) Sinusoidal Pulse Width Modulation

i. *Carrier based PWM schemes*

In carrier based PWM schemes, for m- level inverter, (m-1) carrier waves are used. The carrier base PWM schemes are classified into two, they are,(i) Phase shifted multi carrier modulation,(ii) Level shifted multi carrier modulation. The level shifted multi carrier modulation schemes are again classified into three, they are,(i) In phase disposition method (ii)Alternative phase opposition disposition method and (iii) Phase opposition disposition method.

In this work, Phase Disposition multicarrier scheme is applied to Sinusoidal PWM. In this modulation, the reference sine wave is compared with the level shifted carrier triangular waves for producing the pulses. For a three level inverter, two triangular carrier waves of same frequency and amplitude are compared with the reference wave.

b) Space Vector Pulse Width Modulation

ii *Space Vector diagram of 3-level SVPWM inverter*

The space vector diagram of 3-level inverter is shown in Fig.8 [9,0,11].

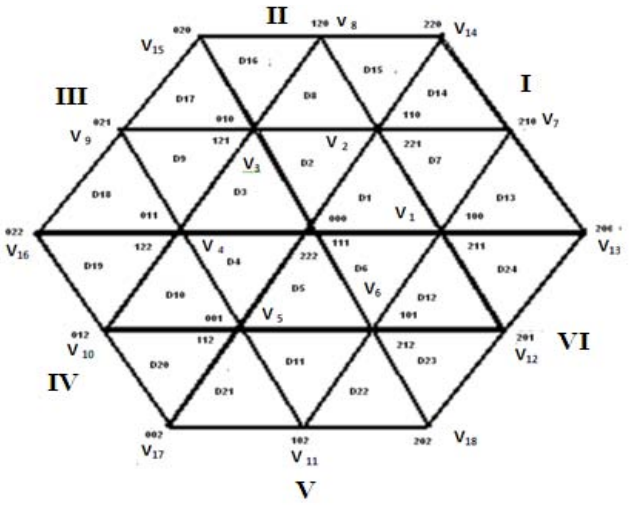

Fig.8 : Space vector diagram of three-level inverter

The plane is divided into 6 triangular major sectors numbered I to VI each of 60^0 of fundamental cycle. There are 4 minor sectors within each major sector such that 24 minor sectors are there in the plane.

The vertices of these minor sectors represent the voltage vectors. In the above plane, V0 is the zero voltage vector, large voltage vectors are represented by V13, V14, V15, V16, V17, V18 and V7, V8, V9, V10, V11, V12 are the medium voltage vectors. To determine the location of the command vector V* in a given major sector, first space vector phase angle' α' is calculated and then sector is determined. The determination of major sector is done as follows:

Table I : Determination of major sector

Range of 'α'	Major sector number
$0 \leq \alpha < 60^0$	I
$60 \leq \alpha < 120^0$	II
$120 \leq \alpha < 180^0$	III
$180 \leq \alpha < 240^0$	IV
$240 \leq \alpha < 300^0$	V
$300 \leq \alpha < 360^0$	VI

Let us consider space vector diagram of sector I as shown in Fig .9. It contains 4 minor triangles D1, D7, D13 and D14. The reference vector can be located in any of these 4 regions, where each region is limited by three adjacent vectors.

If the triangular sector where the command vector lies is defined by vectors Vx, Vy, and Vz assuming their durations Tx, Ty, and Tz respectively and Tx + Ty + Tz = Ts ,then V*= Vref can be synthesized by Vx, Vy, and Vz as follows :

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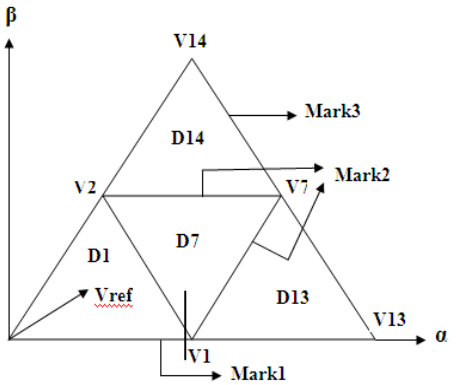

Fig.9 : Space vector diagram of Sector - I

$$Vref = V^* = Vx\,(Tx/Ts) + Vy\,(Ty/Ts) + Vz\,(Tz/Ts)$$
$$Tx/Ts + Ty/Ts + Tz/Ts = 1,$$
$$Tx/Ts = X,\ Ty/Ts = Y \text{ and } Tz/Ts = Z$$

Where, T_S is the switching period.

Based on vector synthesis principle, the following equations can be written.

$$X + Y + Z = 1,\quad Vx\,X + Vy\,Y + Vz\,Z = V^*$$

The equations for the boundaries of modulation ratio Mark I, Mark 2, and Mark 3 can be obtained as follows:

$$\text{Mark 1} = \frac{\sqrt{3}/2}{\sqrt{3}\cos\theta + \sin\theta}$$

$$\text{Mark 2} = \frac{\sqrt{3}/2}{\sqrt{3}\cos\theta - \sin\theta},\ \theta \le \pi/6$$

$$= \frac{\sqrt{3}/4}{\sin\theta},\ \pi/6 \le \theta \le \pi/3$$

$$\text{Mark 3} = \frac{\sqrt{3}}{\sqrt{3}\cos\theta + \sin\theta}$$

Case 1 : If the modulation ratio m<Mark1, the rotating voltage vector V* lies in sector D1 and the same can be synthesized by vectors V0, V1, and V2. Then the following equation is obtained

$$\frac{1}{2}X + \frac{1}{2}(\cos 60^0 + j\sin 60^0)\,Y = m(\cos\theta + j\sin\theta)$$

We can obtain X, Y, and Z as follows:

$$X = 2m.\,[\cos\theta - \frac{\sin\theta}{\sqrt{3}}]$$

$$Y = m\frac{4\sin\theta}{\sqrt{3}}$$

$$Z = 1 - 2m\,[\cos(\theta) + \frac{\sin\theta}{\sqrt{3}}]$$

Case 2 : when (Mark1 < m < Mark2), V* lies in sector D7 and can be synthesized by vectors V1, V2, and V7 . The corresponding X, Y, and Z are:

$$X = 1 - m\frac{4\sin\theta}{\sqrt{3}}$$

$$Y = 1 - 2m.\,[\cos\theta - \frac{\sin\theta}{\sqrt{3}}\}]$$

$$Z = -1 + 2m\,[\cos(\theta) + \frac{\sin\theta}{\sqrt{3}}]$$

Case 3: When (Mark2<m<Mark3) and (0<θ<π/6), V* lies in sector D13 and can be synthesized by V1, V13, and V7. are selected to synthesize V*. The corresponding X, Y and Z are obtained as follows:

$$X = -1 + 2m\,[\cos(\theta) - \frac{\sin\theta}{\sqrt{3}}]$$

$$Y = m\frac{4\sin\theta}{\sqrt{3}}$$

$$Z = 2 - 2m\,[\cos(\theta) + \frac{\sin\theta}{\sqrt{3}}]$$

Case 4: When (Mark2 < m < Mark3) and (π/6<θ<π/3), V* lies in sector D14 and can be synthesized by Vectors V2. V7, and V14. X, Y, and Z can be determined as follows:

$$X = 2m\,[\cos(\theta) - \frac{\sin\theta}{\sqrt{3}}]$$

$$Y = -1 + m\frac{4\sin\theta}{\sqrt{3}} \qquad Z = 2 - 2m\,[\cos(\theta) + \frac{\sin\theta}{\sqrt{3}}]$$

Similar argument can be applied ,when the reference vector lies in the others major sectors. The above calculations for the entire coordinate plane can be obtained by replacing θ by θ -60^0, θ -120^0, θ -180^0, θ -240^0, and θ -300^0 respectively.

V. Simulation Results

Simulations were carried out in MATLAB/ SIMULINK on three-level Neutral Point Clamped Unified Power Quality Conditioner connected to a non-linear load employing Sinusoidal Pulse Width Modulation and Space Vector Pulse Width Modulation techniques and the results are presented below. FFT analysis is carried out in order to measure %THD in the load voltage and source current.

To study the performance of the UPQC, 5th and 7th harmonics are deliberately injected into the system and simulations were carried out to show the response of the UPQC.

a) Simulation results of 3level UPQC with SPWM

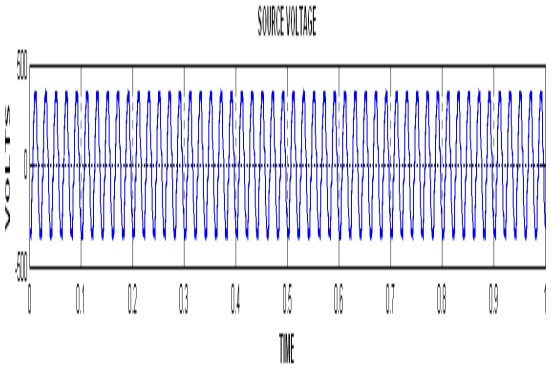

Fig.10 : Sourcevoltage

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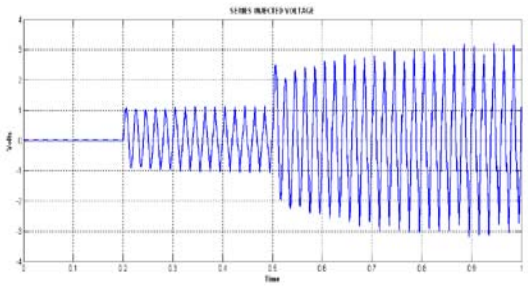


Fig.11 : Voltage injected by the series inverter

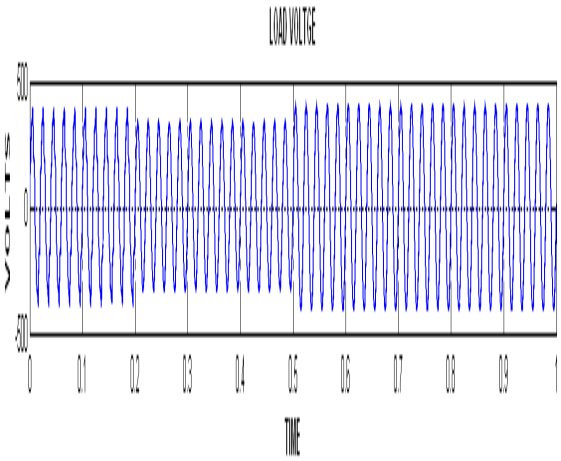


Fig.12 : Load voltage after connecting UPQC

Fig. 10 shows source voltage where 5th and 7th harmonics are deliberately injected to study the ability of the UPQC in reducing the harmonics. Fig.11 indicates the voltage injected by the series inverter and Fig.12 shows the load voltage after compensation. If we observe Fig. 10 and Fig.12, the load voltage is same as source voltage till 0.2 sec where series filter is 'ON' and harmonics are reduced after 0.5 sec when both shunt and series filters are 'ON'.

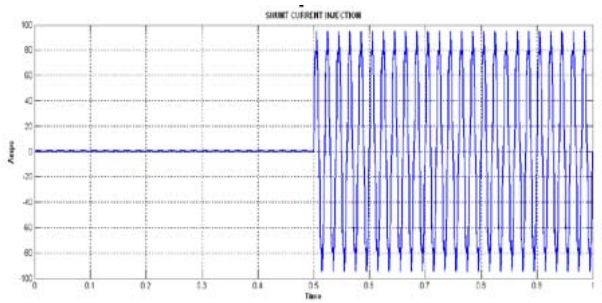


Fig.13 : Current injected by shunt inverter

The shunt inverter is switched on at 0.5sec and it started injecting current as shown in Fig.13.

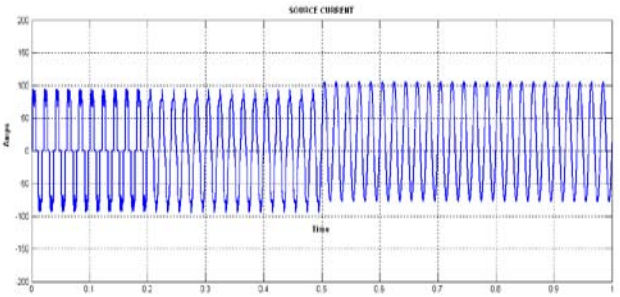
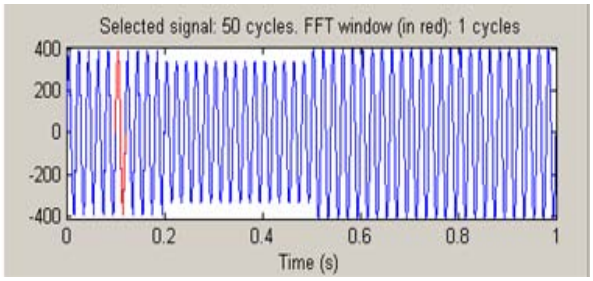
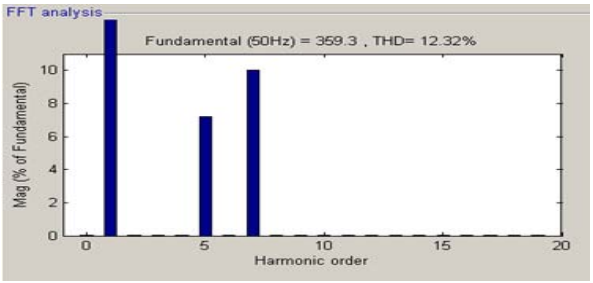


Fig.14 : Source current

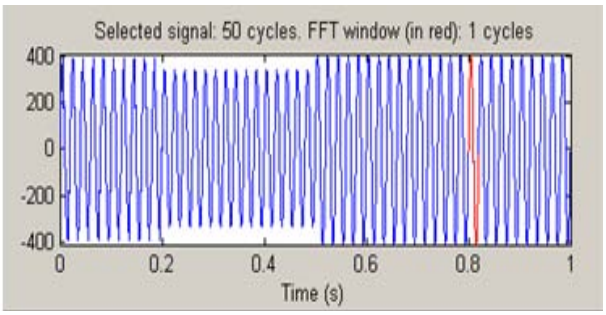
As it is seen in the above Fig.14, the source current harmonics are reduced from 0.5 sec when both filters started operating.

FFT analysis of load voltage





FFT analysis of load voltage before connecting UPQC



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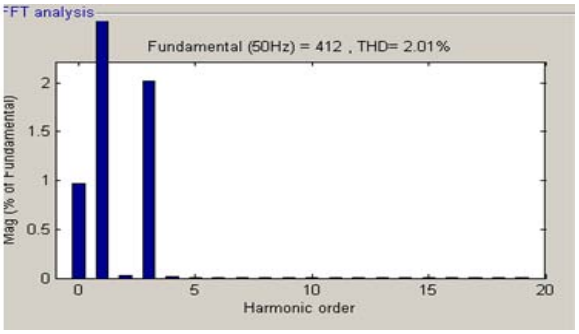
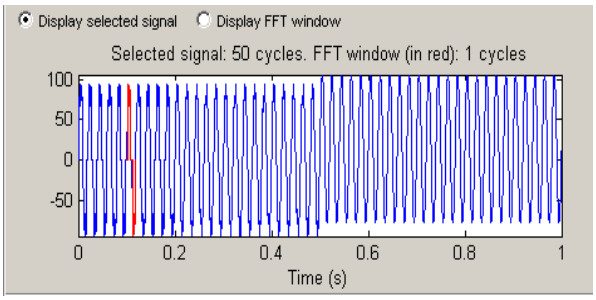
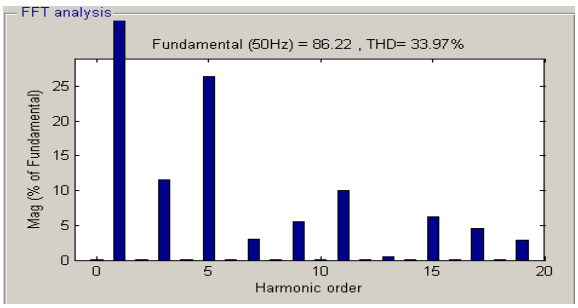


FFT analysis of load voltage after connecting UPQC

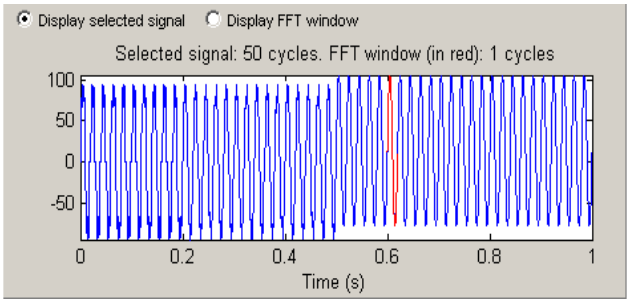
The series inverter is put into operation at 0.2sec and shunt inverter at 0.5sec.FFT analysis is carried out on the load voltage at 0.1sec and the THD is found to be 12.32%. In the second analysis, FFT is done at 0.8sec i.e. after connecting UPQC and THD is reduced to 2.01%



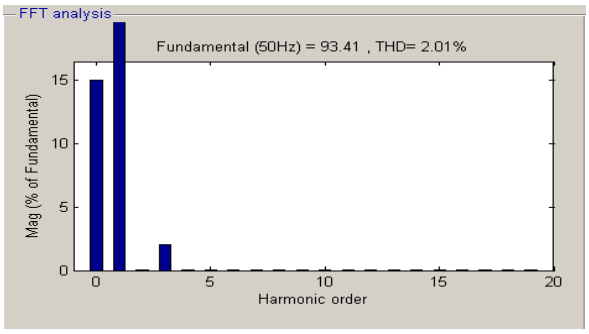
FFT analysis of source current



FFT analysis of source current before connecting UPQC



FFT analysis of source current after connecting UPQC



FFT analysis is carried out on the source current at 0.1sec before connecting UPQC and the THD is found to be 33.97%. In the second analysis, FFT is done at 0.6sec after connecting UPQC and THD is 2.01%

b) Simulation results of 3level UPQC with SVPWM

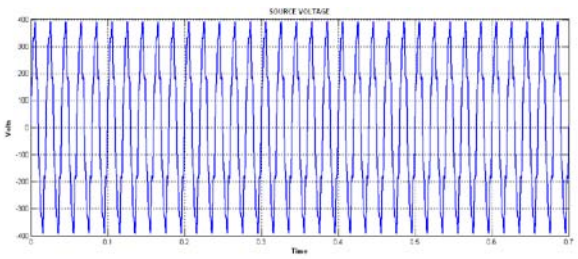


Fig.15 : Sourc Voltage

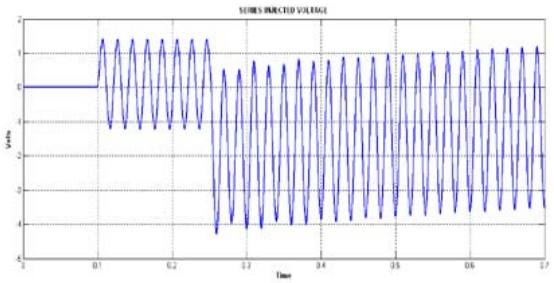


Fig.16 : Voltage injected by series inverter

The series filter is switched ON at 0.1 sec and it started injecting voltage.

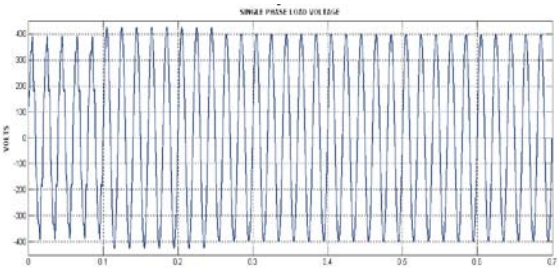


Fig.17 : Load voltage after connecting UPQC

Fig. 15 shows source voltage with 5th and 7th harmonic injection. Fig.16 indicates the voltage injected by the series inverter from 0.1 sec and Fig.17 shows the load voltage after compensation.

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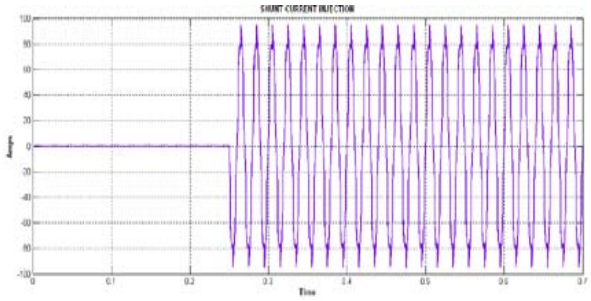


Fig.18 : Current injected by shunt inverter

The shunt filter is switched on at 0.25 sec and started injecting current

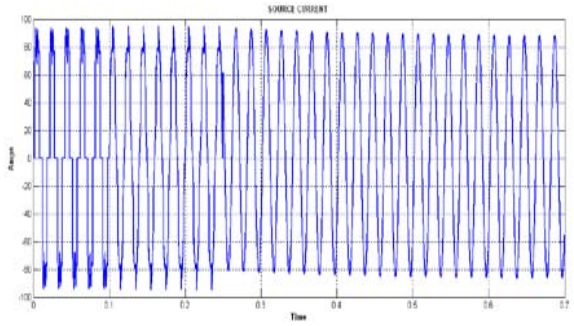
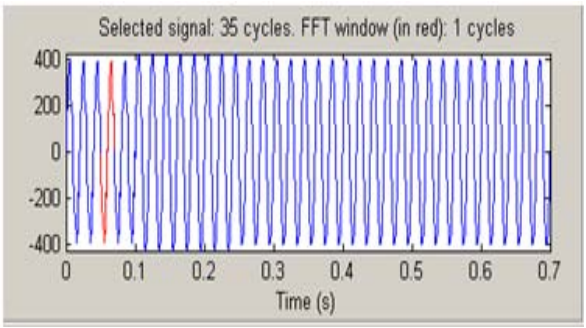
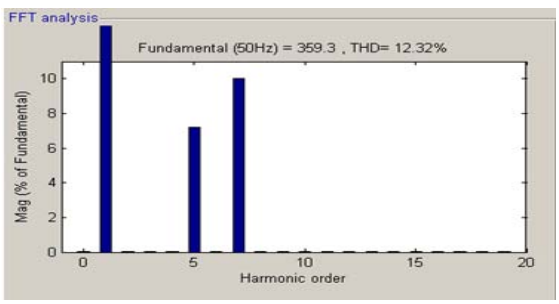


Fig.19 : Source current

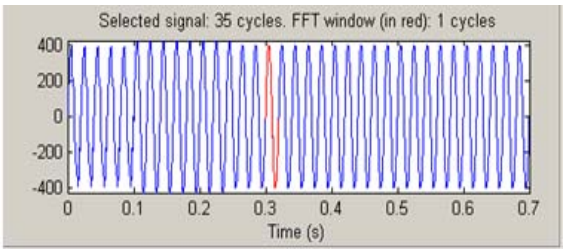
From Fig. 19, it is clear that the harmonics are reduced to some extent after 0.1 sec where series filter is switched ON and from 0.25sec onwards there is a considerable reduction in the harmonics as both filters are in operation.

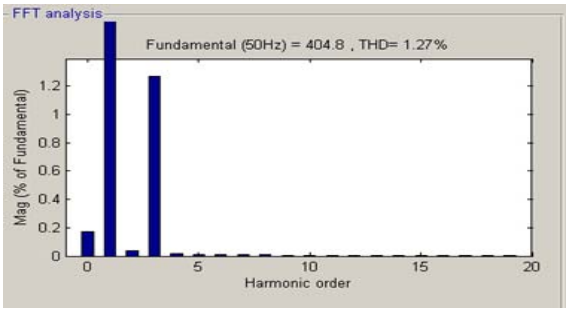
FFT analysis of load voltage





FFT analysis of load voltage before connecting UPQC

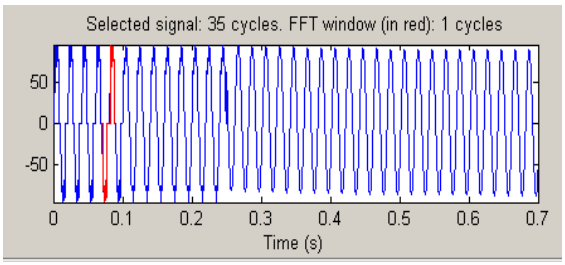


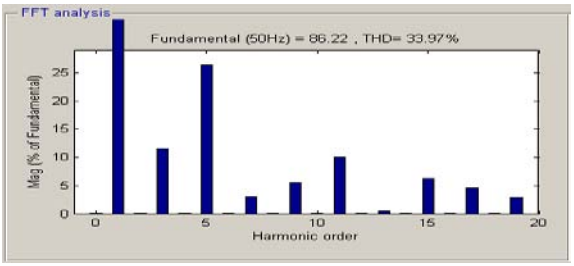


FFT analysis of load voltage after connecting UPQC

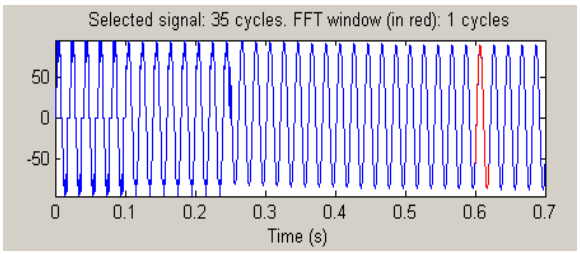
FFT analysis is carried out on the load voltage at 0.05sec before switching ON series and shunt inverters and the THD is found to be 12.32%. FFT analysis of load voltage again carried out at 0.3sec after connecting both series and shunt filters and THD is found to be 1.27%.

FFT analysis of source current





FFT analysis of source current before connecting UPQC



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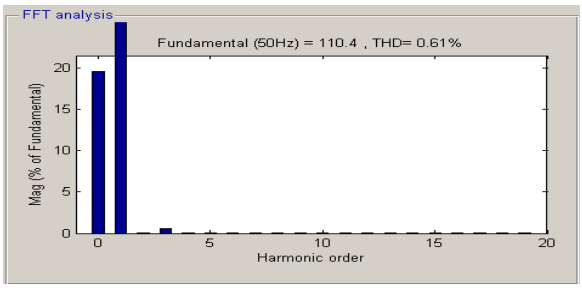


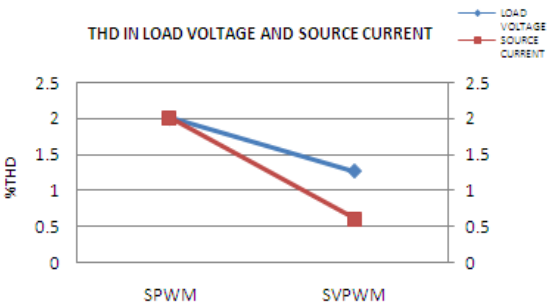
FFT analysis of source current after connecting UPQC

FFT analysis is carried out on the source current at 0.07sec before connecting UPQC and the THD is found to be 33.97%. In the second analysis, FFT is done at 0.6sec after connecting UPQC and measured THD is 0.61%

Table.II : Results of UPQC with SPWM and SVPWM

Control Scheme	Load voltage		Source current	
	%THD Before compensation	%THD After compensation	%THD Before compensation	%THD After compensation
SPWM	12.32	2.01	33.97	2.01
SVPWM	12.32	1.27	33.97	0.61

The above results are shown in the form of graphs for better understanding



The above table and graphs clearly show that the % THD of both load voltage and source current is less with SVPWM when compared to SPWM and within the prescribed limits of IEEE – 519.

VI. Conclusion

The performance of three level UPQC has been evaluated using Sinusoidal Pulse Width Modulation and Space Vector Pulse Width Modulation techniques. To prove the effective compensation by UPQC, harmonics are deliberately injected into the source voltage and the UPQC has successfully reduced harmonics from load voltage and source current. The %THD content in the load voltage and source current after compensation is very less and comply with IEEE-519. The simulation results show that the Total Harmonic Distortion of the load voltage after UPQC is put into operation is less in case of SVPWM compared to SPWM.

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