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FPGA Implementation of High Speed Radar Signal Processing

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Abstract- Electronic support measure (ESM) system or Electronic Warfare Support (ES), is the subdivision of EW involving actions tasked by, or under direct control of, an operational commander to search for, intercept, identify, and locate or localize sources of intentional and unintentional radiated electromagnetic (EM) energy for the purpose of immediate threat recognition, targeting, planning, and conduct of future operations. To test an ESM system field environment is created by using various equipment and design tools. Testing a system is important part of designing and manufacturing a system and it is necessary in any field. To test an ESM system, it is difficult to test it near the theater of war. Testing an ESM system in the theater of war may result in expose of our information to the opponent nations. Therefore, in order to test an ESM system an artificial environment is created by using various equipment and design tools.

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FPGA Implementation of High Speed Radar Signal Processing

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I. INTRODUCTION

The Real time threat environment in the battle field is different and dangerous. In the battle field to test an ESM system there are large number of Radars which monitor or surveillance the signals emitted by the enemies. These Radars identify or trace the signals and transmit to the large group of monitors and equipment. These equipment monitors the data and the Radar parameters such as pulse width, pulse repetition interval, direction of arrival, time of arrival, frequency, type of pulse repetition of time, angle of arrival, distance of the object, pulse repetition of the frequency.

These Radars parameters are identified by the ESM the system and convert into the form of pulse descriptor word format which is of 128 bits. To take the measures in order to protect from the enemy attacks the counter measures are taken with the help of Electronic Counter Measure (ECM) system. These system uses the data captured and create the counter pulses to attack the enemy Radar signal to protect the country. In order to protect from counter signals, the data is captured and transmitted to the advanced system called Electronic Counter Counter Measure (ECCM) System.

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II. MODELING OF THREAT

The field is created using Dielectric Resonator Oscillator (DRO) to generate various frequencies ranging from 1 GHz to 40 GHz. To generate higher frequencies, Voltage Control Oscillator (VCO) is used. These frequencies are given to mixer as an input. The mixer can be used as a switch to select the desired frequency by programming the FPGA control signal line. The inter pulse modulation generator is enabled using enable line to generate desired pulse. The desired frequency and pulse modulated signal is given to the programmable attenuator. The Antenna radiated pattern generated signal is also given to programmable attenuator. The output of programmable attenuator is desired signal, which is used to test the Electronic Support Measure (ESM) systems.

a) Generating Different types of Pulses

Radar system uses a Radio frequency electromagnetic signal reflected from a target to determine information about that target. In any Radar system, the signal transmitted and received will exhibit many of the characteristics Radars pulse signal parameters are pulse width, pulse repetition interval, Frequency, Direction of arrival (DOA), Time of arrival (TOA). The carrier is an RF signal, typically of microwave frequencies, which is usually modulated to allow the system to capture the required data. In simple ranging radars, the carrier will be pulse modulated and in continuous wave systems, such as Doppler Radar, modulation may not be required. Most systems use pulse modulation, with or without other supplementary modulating signals. Note that with pulse modulation, the carrier is simply switched on and off in sync with the pulses the modulating waveform does not actually exist in the transmitted signal and the envelope of the pulse waveform is extracted from the demodulated carrier in the receiver.

Although obvious when described, this point is often missed when pulse transmissions are first studied, leading to misunderstandings about the nature of the signal. The pulse width (T) of the transmitted signal is to ensure that the Radar emits sufficient energy to allow that the reflected pulse is detectable by its receiver. The amount of energy that can be delivered to a distant target is the product of two things; the output power of the transmitter, and the duration of the transmission.

Therefore, pulse width constrains the maximum detection range of a target.

It also determines the range discrimination that is the capacity of the radar to distinguish between two targets fairly close together. At any range, with similar azimuth and elevation angles and as viewed by a Radar with an un modulated pulse, the range discrimination is approximately equal in distance to half of the pulse duration. The pulse width of a signal is shown in Fig 2.1 it also determines the dead zone at close ranges. While the Radar transmitter is active, the receiver input is blanked to avoid the amplifiers being swamped or damaged.

All this means that the designer cannot simply increase the pulse width to get greater range without having an impact on other performance factors. As with everything else in a Radar system, compromises have to be made to a Radar systems design to provide the optimal performance for its role.

b) *Pulse Repetition Interval*

Pulse Repetition Interval is commonly known as PRI. It is the time difference between start time of pulse1 to start time of pulse2 . The difference gives the Pulse Repetition Interval (PRI) as shown in Fig 2.1.

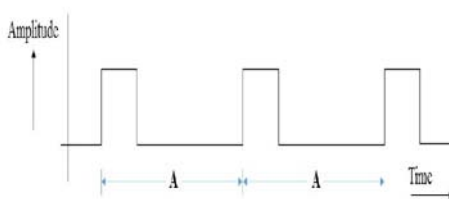


Fig. 2.1: Pulse Repetition Interval (PRI)

The pulse changes in PRI are less than plus or minus one present or measured jitter is believed to be incidental. Most nominally constant signals have less than plus or minus one μ second of Jitter. Desired measures are Mean PRI, Peak-to-peak incidental jitter, Basic Clock Interval Range and type of Count downs.

c) *Optimum PRI for Medium PRF Radar*

Fraction of targets Eclipsed in Range = PD/PRI
 Fraction of targets Eclipsed in Velocity = B_e/PRF
 Fraction of Range Velocity combinations visible = $[1 - PD/PRI] [1 - B_e/PRF]$

$$\frac{\partial (\text{fraction visible})}{\partial PRI} = PD/(PRI)^2 - B_e = 0$$

$$PRI = \sqrt{PD/B_e} \quad \text{optimum duty factor}$$

III. IMPLEMENTATION

The main objective of this paper is to create Radar like parameters to test an ESM system. For this we need a circuitry that generate such pulses and also a modulation mechanism which facilitates to introduce many variations in a continuous waveform. The circuitry which is mentioned for the aforementioned purpose is as shown in Fig 3.1

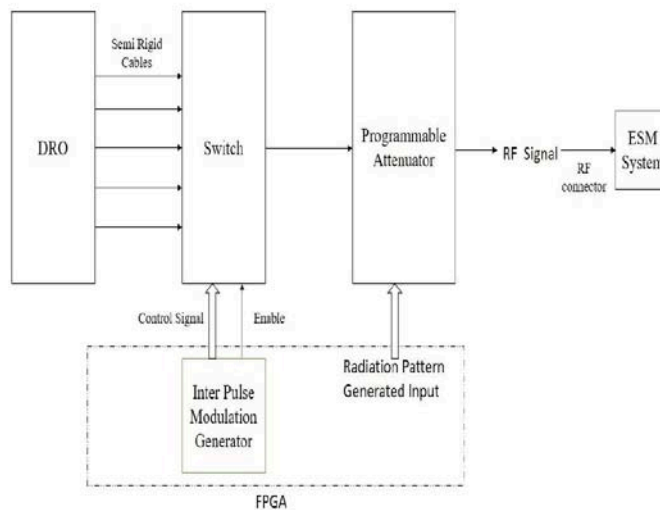


Fig. 3.1: Block Diagram of EW Threat Emulator

a) ESM System

The Radar like signal generated at the output of programmable attenuator is given to an electronic support measure system. The system measures the Radar parameters and show it on the display. Thus the accuracy of the generated Radar signal can be verified. The overlapping discipline, signals Intelligence (SIGINT) is the related process of analyzing and identifying the intercepted frequencies. The SIGINT is broken into three categories: ELINT, COMINT, and FISINT.

The Parameters of Intercepted Transmission are communication equipment Frequency, Bandwidth, Modulation, Polarization etc. The distinction between Intelligence and Electronic warfare support (ES) is

determined by tasks or controls the collection assets, what they are tasked to provide, and for what purpose they are tasked. Electronic warfare support is achieved by assets tasked or Controlled by an Operational commander. The purpose of ES tasking is immediate threat recognition, targeting, planning and conduct of future operations, and other tactical actions such as threat avoidance and Homing. However, the same assets and resources that are tasked with ES can Simultaneously collect Intelligence that meets other Collection Requirements. The ESM System is shown in Fig 3.2.



Fig. 3.2: ESM System

With the increase in Technology the Electronic Warfare has been more significant. Counter measuring and Counter Counter measuring has become very important for the security of a Nation and this has lead to various new techniques such that identifying the Radar parameters has become more and more complicated. This is generally done by using various Intra Modulating techniques on FPGA some of them are introducing a Stagger and Jitter levels and Dwell and Switch method.

b) Protocol & Equipment

The variations in the pulses such as constant, Stagger levels, Jitter and Dwell and Switch can be introduced in the Radar parameters by modulating the continuous wave output from the DRO with the generated pulse in the Inter pulse modulation block which is shown as below in Fig 3.3



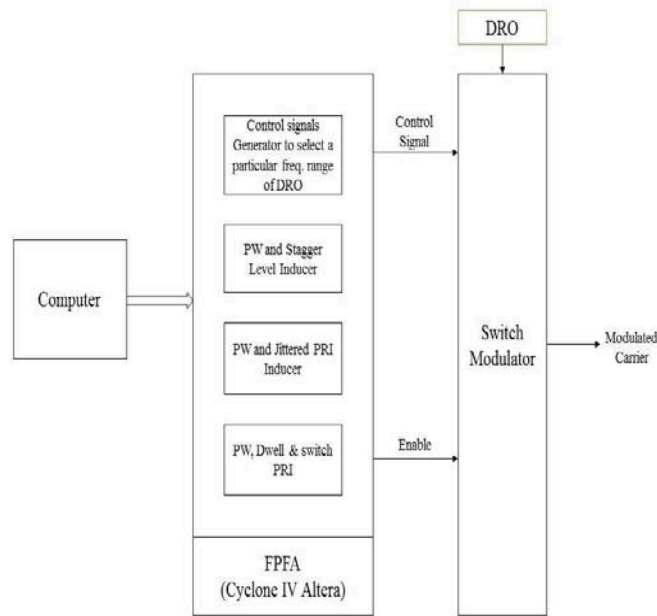


Fig. 3.3: Block Diagram of Inter Pulse Modulation

A computer with a LabVIEW and a Graphical User interface (GUI) is required which relates the inputs to the FPGA. LabVIEW panel has provision to specify the type of pulses and levels that are required and these inputs are sent to FPGA by ASCII sliding Window Protocol. Sliding window refers to an imaginary box that hold the Frames on both Sender and Receiver side. It provides the upper limit on the number of Frames that can be Transmitted before acquiring an acknowledgment. Frames may be acknowledged by Receiver at any point even when window is not full on Receiver side. Frames may be transmitted by source even when window is not yet full on Sender side. The windows have a specific size in which the Frames are

numbered modulo- N, which means they are numbered from 0 to N-1. For example if $N = 8$, the Frames are numbered 0, 1,2,3,4,5,6, 7, 0, 1,2,3,4,5,6, 7, 0, 1.

The size of window is N-1. For example in this case it is 7. Therefore, a maximum of N-1 Frames may be sent before an acknowledgment. When the Receiver sends an ACK, it includes the number of next Frame it expects to receive. For example, in order to acknowledge the group of Frames ending in Frame 4, the Receiver sends an ACK containing the number 5. When sender sees an ACK with number 5, it comes to know that all the Frames up to number 4 have been Received.

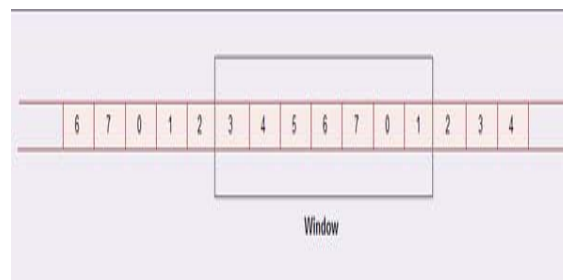


Fig. 3.4: Sliding Window

c) *Sliding Window on Sender Side*

At the beginning of a Transmission, the sender's window contains N-1 Frames as shown in Fig 3.5. As the Frames are sent by source, the left boundary of the window moves inward, shrinking the size of window. This means if window size is w, if four Frames are sent by source after the last acknowledgment, then the number of Frames left in window is (w-4). When the receiver sends an ACK, the source's window expands right boundary moves out words to allow in a number of

new Frames equal to the number of Frames acknowledged by that ACK. For example, if the window size is 7, if Frames 0 through 3 have been sent and no acknowledgment has been received, then the sender's window contains three frames - 4, 5, 6. Now, if an ACK numbered 3 is received by source, it means three frames (0, 1, 2) have been received by receiver and are undamaged.

The sender's window will now expand to include the next three Frames in its buffer. At this point the sender's window will contain six frames 4, 5, 6, 7, 0, 1

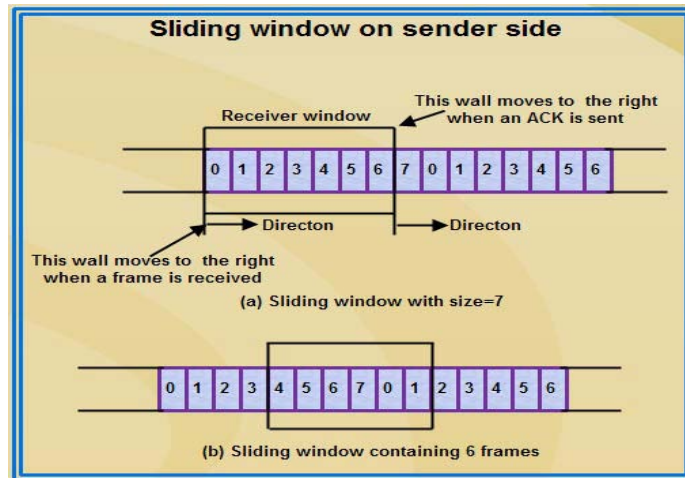


Fig. 3.5: Sliding Window on Sender Side

d) Sliding Window on Receiver Side

At the beginning of transmission, the receiver's window contains $n-1$ spaces for frame but not the frames as shown in Fig 3.12. As the new frames come in, the size of window shrinks. Therefore the receiver window represents not the number of frames received but the number of frames that may still be received without an acknowledgment ACK must be sent. Given a window of size w if three frames are received without an ACK being returned, the number of spaces in a window is $w-3$. As soon as acknowledgment is sent, window expands to include the number of frames equal to the number of frames acknowledged. For example, let the size of receiver's window is 7 as shown in diagram. It means window contains spaces for 7 frames.

With the arrival of the first frame, the receiving window shrinks, moving the boundary from space 0 to 1. Now, window has shrunk by one, so the receiver may accept six more frame before it is required to send an ACK. If frames 0 through 3 have arrived but have DOC been acknowledged, the window will contain three frame spaces. As receiver sends an ACK, the window of the receiver expands to include as many new placeholders as newly acknowledged Frames. The window expands to include a number of new frame spaces equal to the number of the most recently acknowledged frame minus the number of previously acknowledged frame. For example If window size is 7 and if prior ACK was for frame 2 & the current ACK is for Frame 5 the window expands by three $5-3=2$

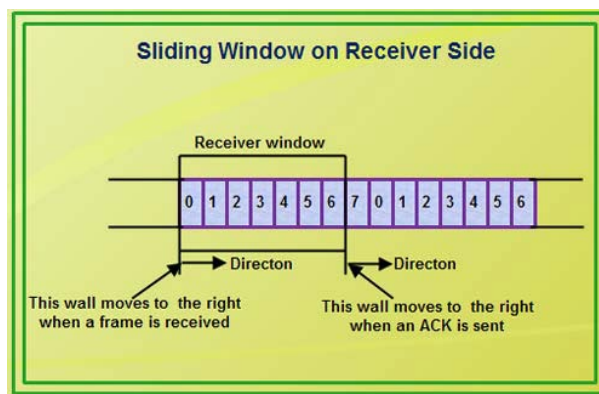


Fig. 3.6: Sliding Window on Receiver Side

Therefore, the sliding window of sender shrinks from left when frames of data are sending. The sliding window of the sender expands to right when acknowledgments are received. The sliding window of the receiver shrinks from left when Frames of data are Received. The sliding window of the receiver expands to the right when acknowledgement is sent.

In the ASCII sliding window protocol there are total 32 Frames. Again each frame is further divided into 7 frames. These seven frames are intended to perform seven different tasks namely Start of frame, Frame number, Data length, Command ID, Data width, Check sum, End of frame or Break of frame. If the command

ends in that frame, then End of frame comes into play. If the command still exists even after completion of the frame, then the command is passed on to the next frame through the Break of frame accordingly.

IV. ANALYSIS AND OUTPUT

Consider we have three segments Continuous Radar (CW) signals are generated by the DRO's as the input in the Range of Ghz. These high frequency signals are observed in the spectrum analyser. A certain Band of frequencies can be selected by either using a binary selector given to a control line or directly give the frequency in lab view software and GUI mode. As DRO's generate high frequency signals, they can be only sending through semi rigid cables with minimal loss of signal. The frequency received can be observed in the spectrum analyser. These received signals will be send to a switch which acts as input. Each DRO is powered with a 5V dc supply voltage.

Pulse generators are also sent into the switch which act as input they are namely Stagger, Jitter, constant and Dwell & switch. Only one kind of pulse generators can be sent at a time. Each different pulse generators have different pulse width (PW) and pulse repetitive index (PRI). Pulse width is width of pulse, generally measured in micro seconds (us) and pulse repetitive index (PRI) is the time duration between two consecutive pulses, generally measured in microseconds (mus). Each pulse generator has its own pulse width and PRI. These values can be manually

given by the user in the GUI interface of lab view Software. Now these pulse generators and CW radar signals from the DRO are inter pulse modulated inside switch. Enable pin determines the Ton and Toff of a pulse. Modulation occurs when enable pin is set to high.

Now arises the Hardware connections. The FPGA used in this is Cyclone 3. NIOS is the software used to program the pins of FPGA. Quartus is a software which is used as a Hardware programming language. It acts as medium between FPGA and Computer. These two devices are connected using JTAG USB cable. Quartus contains lots of tools in it, here we use Eclipse as tool for programming the FPGA. NIOS acts as processor of the system.

The Verilog code is dumped inside the FPGA as discussed earlier and executed. Once the code is executed the output is given to an attenuator .A programmable attenuator is used for attenuating the signal amplitude. The received signal is of very high frequency and it is difficult to identify the maximum amplitude of the signal. So to differentiate the signals a programmable attenuator is used. It is used in such a way that the first pulse is attenuated to its maximum and the next consecutive pulse is attenuated a little less, this continues until the pulse which has highest frequency. Once it reaches the pulse with a maximum frequency, it is very easy to identify the pulse which has the maximum frequency, as it has the minimum attenuation. A detector is used to convert the signal from frequency domain to time domain.



Fig. 4.1: EW Threat Emulation Kit



Fig.4.2: Oscilloscope Output [Carrier 5GHz]

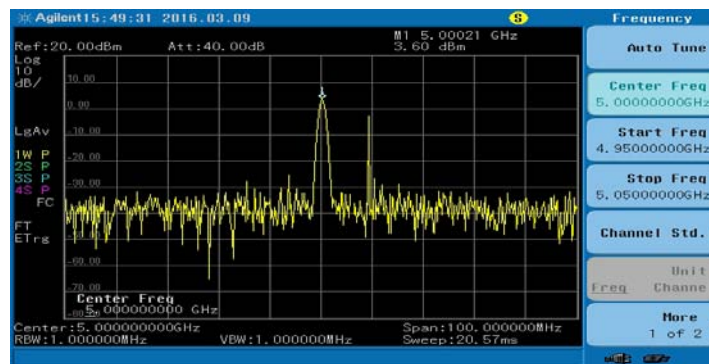


Fig.4.3: Staggered PRI

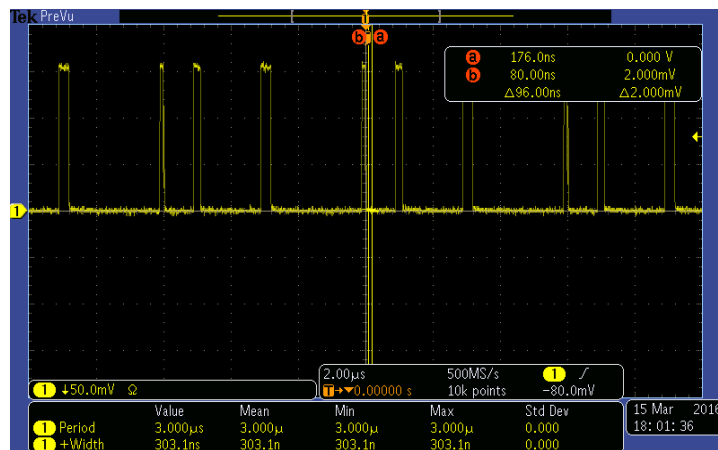


Fig.4.4: Oscilloscope Output [Carrier 8GHz]

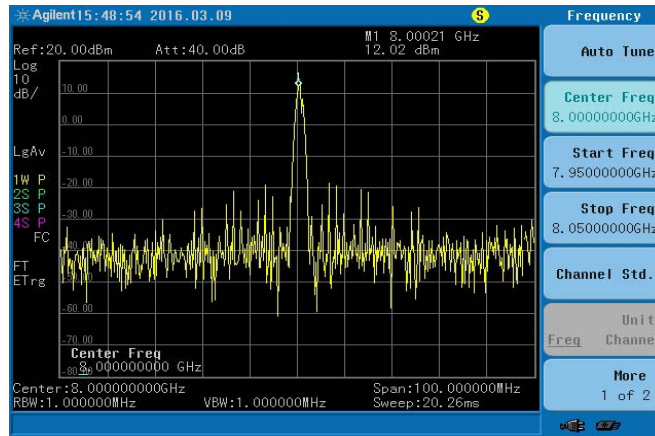


Fig.4.5: Dwell & Switch PRI

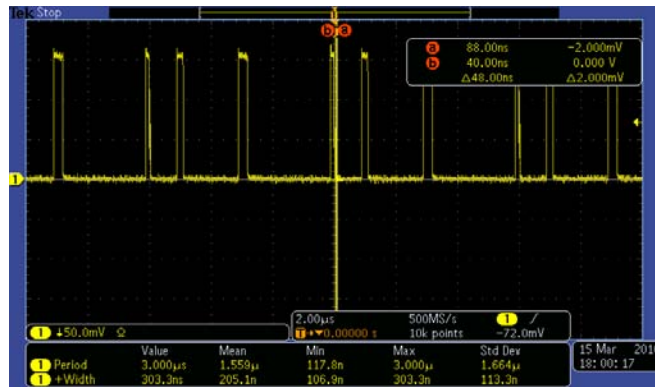


Fig.4.6: Oscilloscope Output [Carrier 8GHz]

Synthesis Report

S No	
Top-level Entity Name	Neo315_Qsys
Family	Cyclone III
Total logic elements	5,391
Total combinational functions	4,335
Dedicated logic registers	3,290
Total registers	3290
Total pins	116
Total virtual pins	0
Total memory bits	204,736
Embedded Multiplier 9-bit elements	4
Total PLLs	0

V. CONCLUSION & FUTURE SCOPE

Modern EW threat Emulation systems are combining advanced materials, SOPC'S, solid-state modules, digital signal processors, and complex A-D converters to give a better look to military and civilian users who need the best possible capability in small, compact, and efficient packages. Recent EW threat emulation systems often have imaging capability, can yield digitized signals quickly and easily for use with graphical overlays, can be networked together so the total system is greater than the sum of its parts, and can serve several different functions such as wide area

search, target tracking, fire control, and weather monitoring where previous generations of Radar technology required separate systems to do the same jobs.

Most important, however, is the relative ease and speed with which modern analog Radar signals can be converted to digital information. Not only does this open wide variety of signal processing options, but it also enables Radar information to be made available in Real time or near Real time on Internet type networks for inclusion in the digital battle field and Global Information Grid visions of the future. The Emulation

system developed in this paper is used to test the ESM Receiver with most of the mathematically defined signals. Two thousand levels of variation can be implemented in the case of Stagger and constant which is definitely an advancement which is possible using SOPC as implemented.

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