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I. Introduction

Fuel Cells (FC) are power sources that convert electrochemical energy into electrical energy with high efficiency, low emissions, and quiet operation. A basic proton exchange membrane (PEM) single-cell arrangement is capable of producing an unregulated voltage below 1V and consists of two electrodes (anode and cathode) linked by electrolyte [1]. The output current capability of a single cell depends on the electrode effective area, and several single cells are connected in series to form a FC stack. Due to the mechanical challenges associated with stacking several single cells, FC are typically low-voltage, high current power sources and can continuously run while reactant is fed into the system [2].

Several approaches to realize DC-DC isolated power conversion for FC power sources have been proposed based on full bridge, push–pull, and current-fed topologies. Some of the key contributions in the area include the study outlined in the following. An FC power converter based on a controlled voltage doubler was introduced, which uses phase-shift modulation to control the power flow through the transformer leakage inductance [3]. This interesting topology proved to be less efficient than other traditional topologies [4], but presents the advantage of the low component count. An FC inverter based on a traditional push–pull DC–DC converter was presented featuring low cost, low component count, and DSP control [5]. Based on the push–pull topology, a modular architecture was presented to enhance scalability and reliability [6]. An innovative current-fed version of the push–pull topology has been reported as part of a grid connected inverter system [7]. A similar current-fed push–pull topology was employed in a step-up resonant converter, presenting a high voltage-conversion ratio [8]. A full-bridge forward DC–DC converter with a full-bridge rectifier was presented [9]. This is a very robust topology when operated with zero-voltage switching (ZVS) technique and represents an industry standard in many applications, such as telecom power supplies (high input voltage). A three-phase version of the full-bridge forward converter was recently proposed [10], based on Δ-Y transformer connection and a clamp circuit to reduce the leakage inductance and circulating currents. A new family of phase-shift ZVS with adaptive energy storage was also proposed to increase soft switching operating range using auxiliary circuits [11]. As well, topologies based on current-fed full-bridge topologies were proposed featuring low-input ripple current and reduced stress on the input-side switches [12].

Successful power conditioning for FC systems requires dealing with poor voltage regulation, high input current, and a wide range of output loading conditions while maintaining high efficiency and low switching stress. When exposed to these stringent requirements, full-bridge ZVS, push–pull, and current fed topologies are confronted with several technical challenges. For example, maintaining ZVS (full-bridge) is difficult due to the poor voltage regulation of the FC and the wide range of loading conditions, which creates excessive conduction losses due to circulating current in the primary. The push–pull topology reduces transformer utilization (primary center tap), compromises magnetizing balance as the power rating increases (winding asymmetry and excitation imbalance), as well as limiting the possibilities for soft-switching operation. Current-fed-based topologies need bulky input inductors (high current), present oscillations produced by the interaction between parasite (leakage inductance, intra winding capacitance, and the input inductor), and could present excessive degrading high-frequency ripple current in the output capacitors due to the absence of filter inductor. While the trend for high-input-

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voltage converters (e.g., connected to the line) has been to minimize switching losses and deal with relatively small line regulation, FC power conversion presents the opposite scenario with low input voltage, poor regulation, and very high input current. Unlike applications with high input voltage, achieving ZVS with low voltage does not lead to substantial efficiency gains, given the small energy stored in the MOSFETs output capacitance (Coss). The power dissipated in a MOSFET due to the output capacitance during turn on is a function of the square of the FC voltage v_{fc}^2 . Since FC are low-voltage, high-current power sources, the relative importance of switching losses can be outweighed by conduction losses in the MOSFETs that are a function of i_{fc}^2 .

The ANFIS set theory is also used to solve uncertainty problems. The key benefit of ANFIS logic is that its knowledge representation is explicit, using simple "IF-THEN" relations. All situations that are not characterized by a simple and well defined deterministic mathematical model, can be more easily handled in terms of the ANFIS-set theory, in which simple rules and a number of simple membership functions are used to derive the correct result.

In general, ANFIS sets are efficient at various aspects of uncertain knowledge representation and are subjective and heuristic, while neural networks are capable of learning from examples, but have the shortcoming of implicit knowledge representation.

The ANFIS-logic system is inflected in three basic elements: fuzzification, ANFIS inference, and de fuzzification. Degrees of membership in the fuzzifier layer are calculated according to IF-THEN rules. They base their decisions on inputs in the form of a linguistic variable derived from membership functions

Which are formulas used to determine the ANFIS set to which a value belongs and the degree of membership in that set. The variables are then matched with the specific linguistic IF-THEN rules and the response of each rule is obtained through ANFIS implication. To perform compositional rule of inference, the response of each rule is weighted according to the impedance or degree of membership of its inputs and the centroid of the response is calculated to generate the appropriate output.

This paper addresses the challenges 1) to 5) by proposing a set of soft-switching techniques in a full-bridge forward topology. For this purpose, a special modulation sequence is developed to minimize conduction losses while maintaining soft switching characteristics in the MOSFETs and soft transitions in the output rectifiers. Auxiliary elements in the primary, such as series inductors and capacitors that are impractical to realize due the extreme input current are avoided by reflecting them to the secondary of the circuit to minimize circulating current and generate soft transitions in the switches. These variations are conceptually depicted in Fig. 1 indicating three major modifications suited for FC power conversion. The proposed combined techniques have the ability to maintain high efficiency in the entire operating range of the FC (wide input voltage) and under any loading condition. Detailed analysis of the techniques for efficiency gains is presented and a phase-shift ZVS topology is employed as a reference topology to highlight the mechanisms for performance enhancement and the advantages in the use of the special modulation. Experimental results of a 1-kW power converter are presented to validate the efficiency gains, illustrate the benefits of the special modulation, and demonstrate the soft-switching transitions.

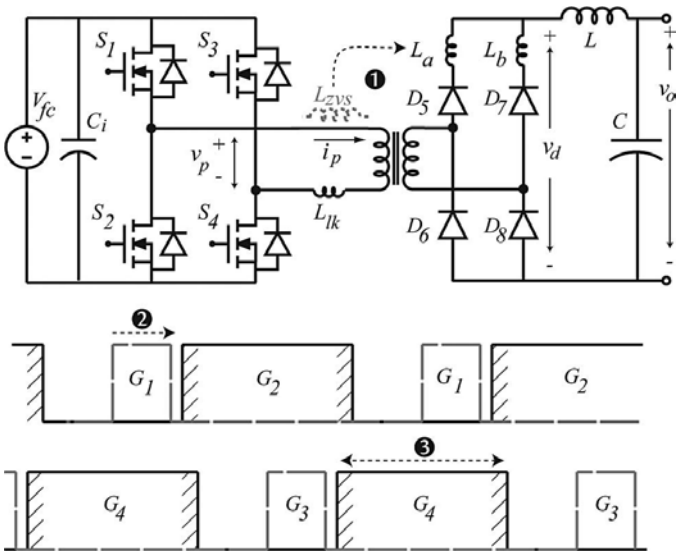

Fig.1, 2 & 3: Basic schematic for test system & pulse generation

II. Fc Voltage Regulation

This section briefly revisits the regulation characteristic of a polymer-electrolyte FC under different operating conditions, providing the basis for successful design of power conditioning stages. Both PEMFC and direct methanol FC (DMFC) belong to this category. The factors that mainly contribute to the output voltage behavior in a DMFC are fuel (methanol concentration), fuel flow rate (supplied to the anode), air/oxygen flow rate (supplied to the cathode), and operating temperature [1]. As well, the output current is a significant factor that affects the output voltage and, hence, its output power. It is interesting to note how the output voltage of this DMFC is greatly affected by its operating temperature and output current (fuel and oxygen flow rates are close to optimal in this case). This results in a significant change of the available output power, the area under the polarization curve. Therefore, in order to obtain a desired output power, it is first necessary to modify the operating conditions to increase the area under the polarization curve (for example, by increasing the operating temperature). It should be pointed out that the transition from a given polarization curve to another through variation in operating conditions is very slow. The main reasons for this behavior are the high heat capacity of the cell, and the slow mass transport processes in the flow fields and electrodes (fuel distribution in the flow channels and electrode assembly) [2], [23]. However, a fast dynamic response exists when the output current changes in fixed operating condition. As a result of this example, the poor voltage regulation, high current and low-voltage characteristics are highlighted. The same principle follows for larger electrode areas required to produce high currents, and a number of singles cells in series to conform a FC stack.

III. Right-Aligned Modulation and Primary Inductor Elimination in the Full-Bridge Topology

This section presents in a sequential and conceptual manner the steps taken to fulfill the requirements toward increasing the efficiency of the full-bridge forward converter in FC power conversion. A description of the power-loss mechanisms in the input stage is first presented, followed by the analysis of the output rectifier. Each design goal is addressed by the combined effects of the proposed soft-switching techniques.

a) *Full-Bridge Input Stage*

The conduction losses in the MOSFETs due to circulating current [design goal (a)] and the high-current bulky inductor in the primary are eliminated by removing the traditional *Lzvs* inductor in the primary and by forcing a right-aligned sequence of pulses in the upper switches as illustrated in Fig. 1 (modifications ① and ②). In order to illustrate the gains of the two changes with a practical example, Fig. 3 presents the conduction losses of a commercial MOSFET with low *R*dsON as a function of duty cycle for the voltage polarization curve of a commercial hydrogen FC. It can be seen that the total conduction losses un-der phase-shift ZVS (+ curve that includes circulating current) are considerably higher than losses only associated with power transferred to the secondary. The losses have been calculated using the rms value of the current through switch*M*1 and the MOSFET ON-resistance *R*dson , which is a function of the device temperature

$$P_{losscon} = R_{dson}\, i_{M1}^2 \qquad (1)$$

For example, the IRFB4110 has 3.7 mΩ at 25^0 C and 6 mΩ at 100^0 C (typical), resulting in 35 W conduction losses under 75 A rms at 100^0 C. When the switching losses are analyzed, the same power device experiences less than 6.5 W during the turn- ON transition due to its output capacitance *C*oss when switching at 40 kHz with *v*fc = 22 V as given in the following:

$$P_{losscoss} = \frac{1}{2} C_{oss} F_{sw} v_{fc}^2 \qquad (2)$$

Therefore, it can be inferred that in this particular low-voltage high-current application, the efficiency gain resulting from reducing circulating current in four switches outweighs those of switching losses, especially under heavy loading conditions. When the lower switches are considered, the scenario is even more favorable, as *M*2 and *M*4 not only benefit from lower conduction losses, but also operate in ZVS due to the modification ③in the modulation (+50% duty cycle). In addition, the reduction in the conduction interval also helps to reduce copper losses in the transformer windings and favors the use of planar magnetic with their inherent low leakage inductance to increase power transfer.

b) *Output Rectifier Stage*

The output rectifiers contribute to conversion losses due to conduction and reverse recovery. Since the output voltage of the power converter is high (i.e., 220 V to supply a single-phase inverter), the conduction current is typically a few amperes per kilowatt of output power (i.e., 4.54 A), making the reverse-recovery losses the dominant factor. Reverse-recovery charge is a function of the forward conduction current (*IF*) and the rate of change of current (*di*/*dt*), as well as operating temperature of the device. The reverse-recovery losses can be estimated by using the recovery charge, switching frequency (*F*sw), and reverse applied voltage (*VR*), including the peak ringing value as follows

$$P_{loss} = Q_{rr} V_R F_{sw} \qquad (3)$$

As a simple review of this combined effects, a conceptual relationship among *di*/*dt*, the *IF* , and *Q*rr in which the initial forward current is given by *IF* 3 > *IF* 2 > *IF* 1. As indicated in (3) the reverse-recovery losses can be reduced by means of controlling *di*/*dt* [design goal (c)] and by reducing the reverse peak voltage *VR* produced by transformer oscillations [design goal (d)]. For this purpose, the *L*zvs inductor is reflected to the secondary and placed at the output of each upper rectifier *D*5 and *D*7 (modification③). This technique limits the *di*/*dt* in the upper rectifiers, eliminates reverse recovery in the lower diodes *D*6 and *D*8, and reduces significantly the transformer oscillations by preventing a zero-voltage state at the secondary. As will be seen, the technique avoids simultaneous conduction of *D*5 , *D*6 , *D*7, and *D*8, thus reducing undesirable ringing that occurs when the primary current matches the inductor output current, which results in a severe voltage step in the secondary that creates ringing, and therefore, electromagnetic interference (EMI). In the following section, the operation of the full-bridge forward converter and the effect of the proposed modifications for efficiency improvements are presented in detail over the various switching intervals.

IV. Analysis of Anfis Controller

Proposed system consists of ANFIS to limit error in minimum range based on rules written and its membership functions. The proposed method is as shown in fig4. The simulation has been done on a DFIG system integrating the proposed FLCs for the vector control as shown in Fig. 4. The parameters of induction machine are influenced from Refs. [17] and are indexed in Tables 2 and 3.The vector control performance of proposed ANFIS controller is contrasted with a vector control utilizing fuzzy logic controllers. The wind speed is set at 6 m/s in accordance with a angular speed of 78 rad/s (Fig. 5(d)).

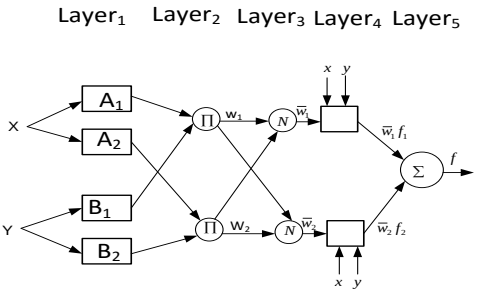

Fig. 4: The architecture of the ANFIS

V. Operation Intervals and Loss-Reduction Effects

The combination of the proposed techniques, *L*zvs inductor reflection to the output of the rectifier (①), right-aligned gate signals for the upper switches (②), and +50% duty cycle in the lower switches (③) are investigated in detail in this section. Fig. 5 shows the switching sequence for MOSFETs *M*1, *M*2, *M*3, and *M*4 along with the main waveforms for the techniques under study. Transition intervals have been exaggerated for clarity.

a) Detailed Analysis of the MOSFETs Waveforms

The waveforms for MOSFETs *M*1 and *M*4 and their respective body diodes *D*1 and *D*4 are shown in Fig. 7 during a full-cycle period, including the gate signals *G*1 and *G*4, drain to-source voltages *vM*1 and *vM*4 , currents for the MOSFETs n-channel *iM*1 and *iM*4 , and the body diodes *iD*1 and *iD*4.

As can be seen, unlike phase-shift ZVS or resonant converters, the proposed techniques prevent unnecessary circulating current in the transformer and through the MOSFETs, and allows power transfer during the conduction interval. This is a key requirement in low-voltage, high-current applications, where the conduction losses are substantial and outweigh switching losses at moderate switching frequencies. As well, the +50% duty-cycle modulation sequence ensures zero-voltage transitions in MOSFETs *M*2 and *M*4. The gains described in this section are further enhanced in the output rectifier as described in the following section.

b) Output Rectifier Waveforms

In order to complete the analysis of the waveforms and efficiency gains, the output rectifier should be investigated. The current and voltage waveforms for *D*7 (upper) and *D*8 (lower) diodes are presented in Fig. 8, where both conduction losses and reverse-recovery instants can be identified.

In summary, the waveforms for the proposed soft-switching techniques reveal the following improvements.

1. The auxiliary inductors *La* and *Lb* shape the current waveforms of *D*5 and *D*7 during reverse recovery. Therefore, the inductor values can be selected to achieve a desired *Q*rr in the upper diodes and, hence, control the total reverse recovery conversion losses.
2. Diodes *D*6 and *D*8 experience negligible reverse-recovery losses, unlike the phase-shift ZVS topology, which is ex plained by near-zero forward current when the reduced reverse voltage is applied.
3. The presence of *La* and *Lb* reduce oscillations and the peak reverse voltage applied to *D*6 and *D*8 that result from transformer ringing.

Transformer oscillation results in undesirable effect, such as high maximum reverse voltage rating for the diodes, EMI, over voltage between windings, and conversion losses in auxiliary snubber circuits. The concept of avoiding a zero-voltage condition on the transformer secondary is addressed by preventing simultaneous conduction of *D*5 , *D*6 , *D*7 , and *D*8 . As a

result, the turn-ON pulse is partially reflected to the secondary of the transformer as if the converter were operating in discontinuous conduction mode. Hence, the oscillations are reduced under any loading condition.

c) Frequency Response and Dynamic Behavior

The frequency response of the control-to-output characteristic of the full-bridge topology, which is a buck-derived topology, is dominated by the transfer function of the output filter (*L* and When the converter is operated in phase-shift ZVS, a series inductance is required to limit the current rate of change in the primary to generate soft transitions in the switches [24]. This limitation, reduces the effective duty cycle reflected to the secondary, therefore, affecting the control-to-output characteristic. As a result, an artificial dumping effect is created in the frequency response by the series inductance, which softens the control-to-output characteristic peak at the resonant frequency of the filter [25]. In closed-loop operation using traditional compensation (small signal), the artificial dumping does not have any noticeable effect in phase and gain margins. A similar behavior is experienced when the proposed techniques are employed using traditional compensators, therefore, showing a dynamic response similar to that of a phase-shift ZVS.

In this study, in order to facilitate the efficiency evaluation process, multiple measurements were performed with a closed loop controller (small-signal) in steady-state operation. The controller was realized with an inner current loop (inductor current) and an outer voltage loop. Validation of the waveforms and comparative efficiency measurements are presented in the following section.

VI. Simulation Results

Table 1: Converter Parameters

Parameters	Value limits
v_{fc}	18-40V
v_o	220V
L	1.33mH
D_a, L_b	10uH
C	680uF
C_i	4400Uf
F_{sw}	40-100kHz
T/f primary turns N_p	2
T/f secondary turns N_s	26

a) Validation of the Waveforms

A complete switching cycle in *M*1, *M*4, *D*7, and *D*8 was measured under medium loading condition to validate the waveforms. In order to facilitate the visualization, the switching frequency was set to 40 kHz. Fig. 9 shows the waveforms of MOSFET *M*1, including gate and drain-to-source voltages, and the secondary transformer current. It can be seen that the MOSFET current starts at zero (ZCS) at the beginning of *T*1 and slowly ramps up until it reaches the current level of the output-filter inductor at the beginning of *T*2. The MOSFET turns off during *T*3, limiting the conduction interval to *T*1–*T*2. The body diode *D*1 conduction interval can be seen in *T*11, which returns the energy of the leakage inductance to the input dc bus and avoids circulating current in the primary. The small energy in the leakage is absorbed and clamped by the input capacitors of the converter. The lowerMOSFET*M*4 waveforms are shown in Fig. 10, where the zero-voltage transition during turn-ON can be seen at the beginning of *T*11. Thereafter, at the beginning of *T*4, *M*4 turns off. As well, *D*4 has a soft-switching transition during *T*5. The conduction interval in *M*4 is similar to that of *M*1, showing reduced conduction losses.

In order to evaluate the converter operation under phase shift ZVS, the inductor *L*zvt was included and *La* and *Lb* were removed. Fig. 11 shows MOSFET *M*1 drain-to-source voltage (Ch1) and gate-to-source (Ch2) signals along with the secondary current waveform *is* (Ch4). It can be seen that the turn-ON transition occurs during (*T*1) interval and the conduction is extended until the end of (*T*6). As described by the analysis of conduction losses, the conduction interval presents unnecessary circulating current. MOSFET *M*4 (lower side switch) presents a similar behavior with circulating current.

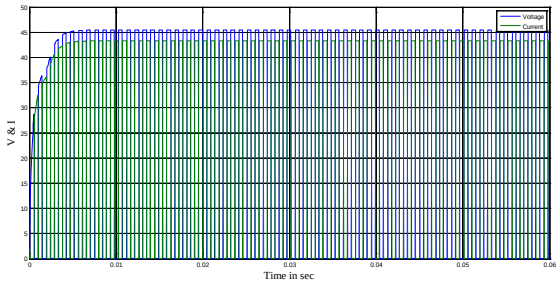

Fig. 5: Upper MOSFET Voltage and Current

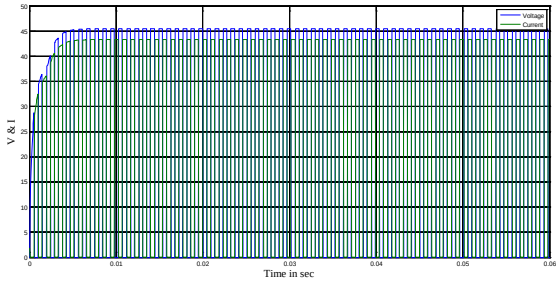

Fig.6 : Lower MOSFET Voltage and Current

Focusing on the rectifier stage, the upper output-rectifier *D*7 waveforms with the proposed techniques are shown in Fig. 12. The turn-OFF transition from forward-biased to blocking is illustrated in interval

*T*1. The effect of *Lb* and *L*lk can be seen in the current transition, resulting in moderate reverse-recovery losses at the beginning of *T*2. The end of the interval *T*7 corresponds to the instant when the current in *Lb* matches the current in the output-filter inductor *L*. During *T*8 , the slope of *iD*7 is mainly due to *L*. The conduction interval is defined from *T*7 to *T*1 of the next switching cycle. As can be seen, the transformer oscillation are small and experience a fast damping beginning at *T*2 (no snubber have been included in the prototype). Only an initial peak is experienced due to the effect of the stray inductance in the current path (hall effect sensor measurement path) and *Lb*. This provides a clear indication that the proposed arrangement only requires a small local snubber connected from *D*7 cathode to *L* input terminal, as opposed to the well-known bulky snubber circuit in ZVS circuits.

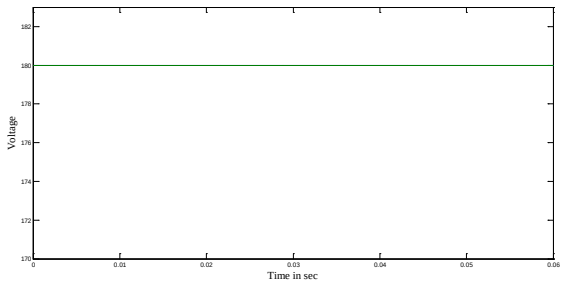

Fig. 7: Upper side diode Voltage Medium Loading.

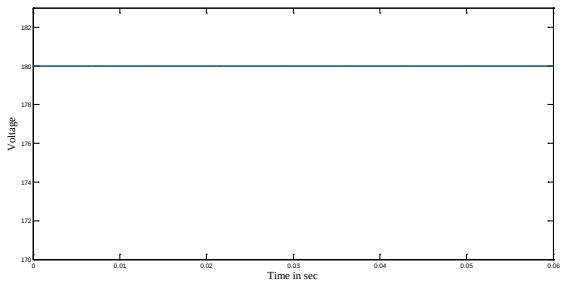

Fig. 8: Upper diode voltage under proposed controller

The improvement that results from the proposed modifications is better appreciated in the experimental waveforms for *D*8 depicted in Fig. 13. Due to the interleaving effect of *La* and *Lb* during *T*3–*T*5 interval, diode*D*8 experiences a fast transition from high conduction current to near-zero current. At the beginning of *T*7, the converter input voltage is partially reflected to the secondary and blocks *D*8 immediately with a transition that produces negligible reverse-recovery losses in *D*8. As well, the blocking transition presents moderate ringing at the beginning of *T*7 while the upper diode current *iD*7 ramps up.

When this is compared to the behavior under phase-shift ZVS, which is presented in Fig. 14, diode *D*8 presents undesirable reverse-recovery losses at the beginning of interval *T*8, where a small negative-current peak can be seen due to the effect of *Q*rr . As predicted by the analysis, the ringing peak voltage in *D*8 is high, increasing the reverse-recovery losses and requiring a bulky snubber.

Finally, in order to verify that the input current is positive, a fundamental requirement in FC power conversion, Fig. 15 presents the input current of the converter and the transformer input voltage operating under medium loading condition. As predicted by the analysis, the current remains positive during all the switching intervals.

b) Comparative Efficiency Measurements

The combined switching and conduction losses for the proposed soft-switching techniques are presented in this section. A phase-shift ZVS is employed as a reference topology for comparative evaluation. The same power devices, power transformer, drivers, dead-time insertion, heat sink and fan, and output filter were employed in both cases to ensure a fair comparison (see Table I). Note that the objective of the experimental efficiency measurements is to illustrate the efficiency gains with the proposed modifications rather than performing an absolute measurement of the converter efficiency. The efficiency measurement accounts for the power switches, printed circuit board, connections, and magnetic parts and does not include losses in the controller and drivers. For ZVS operation, the auxiliary *L*zvt inductor and snubbers were included, while removing *La* and *Lb*. Several tests were performed for various input voltages *v*fc = 18, 25, and 30 V under variable loading conditions (50–1000 W range) for both power converters. The results are shown in Fig. 16, illustrating the efficiency as a function of output power and input voltage in a 3-D plot. It is important to highlight that even though efficiency characterization in power converters is traditionally performed using fixed input voltage, FC power conversion requires the use of a polarization curve (variable input) to account for the lax voltage regulation that is characteristic in these power sources. Therefore, a surface efficiency measurement provides a better means for comparison, as presented in Fig. 16. The efficiency profile achieved with the proposed soft-switching techniques, referred to as Modified in the figure is depicted with circle markers, while the phase-shift ZVS is illustrated with star markers. It can be seen that the proposed modifications present a significant efficiency gain under any operating condition. For example, an efficiency gain of 3%–4% in a power converter with an overall efficiency of 90% provides an improvement close to 30%–40% in the thermal management of the power stage and allows the use of lower cost power semiconductors/ Heat sinks. This can be considered as an excellent improvement toward power density and cost of the power conversion stage, while maintaining the simplicity of a full-bridge topology. As well, the efficiency gains result in

cumulative fuel savings (i.e., hydrogen or methanol) under any operating condition (light, medium, and heavy) by employing the proposed soft-switching techniques.

VII. Conclusion

The ANFIS based new control topology will reduces the power conversion losses. The transformer utilized conversion network can minimizes stresses on power electronic devices used for conversion. stress less devices can give better performance gives to reduces the losses. The ANFIS based controller can works fast and accurately in pulse generation compared to conventional Fuzzy Logic controller.

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